# TRAVEO™ T2G event generator

## Customer Training Workshop

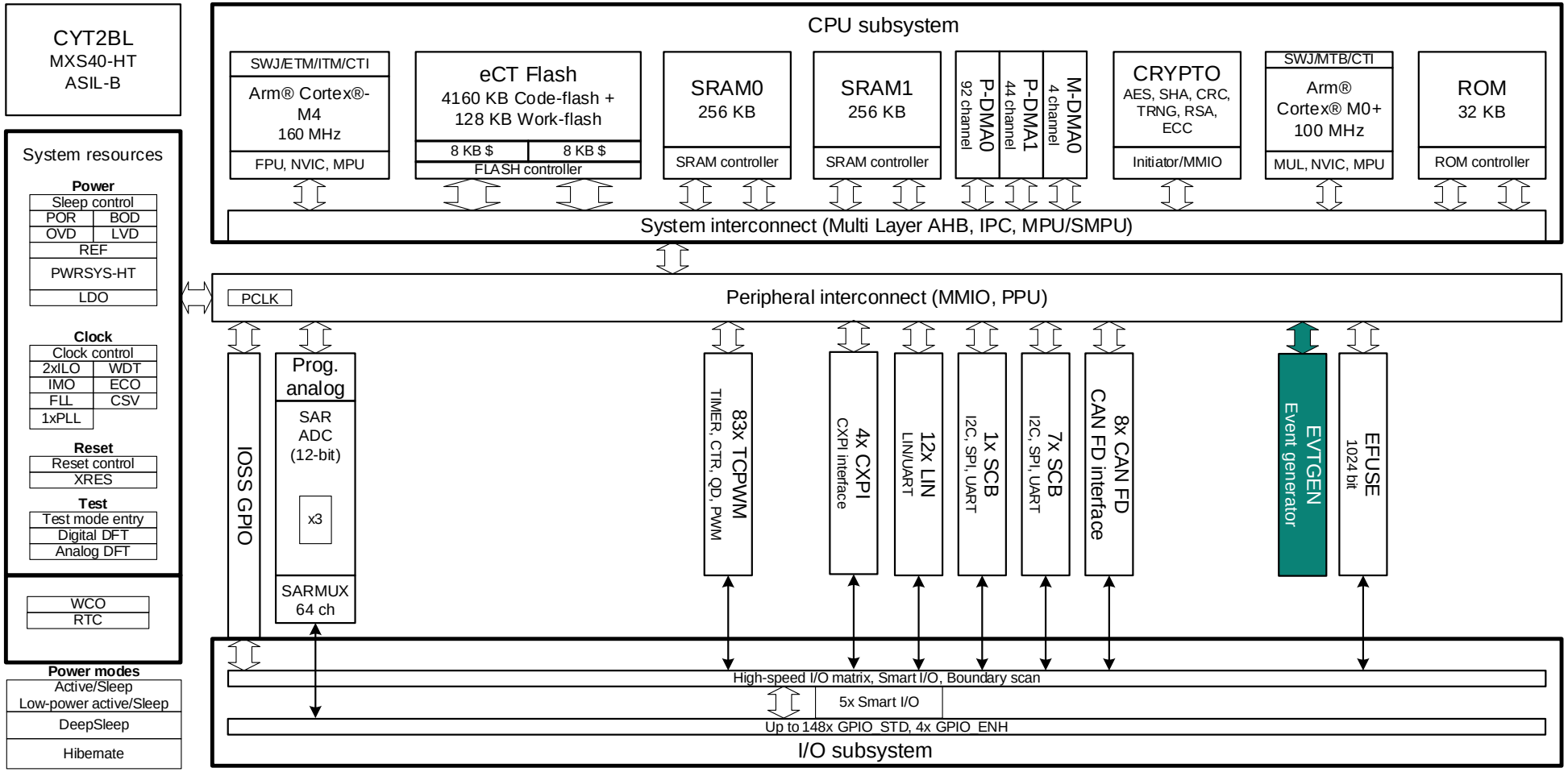
# Target products

Target product list for this training material:

| Family category | Series | Code flash memory size |
|---|---|---|
| TRAVEO™ T2G Automotive body controller entry | CYT2B6 | Up to 576 KB |
| TRAVEO™ T2G Automotive body controller entry | CYT2B7 | Up to 1088 KB |
| TRAVEO™ T2G Automotive body controller entry | CYT2B9 | Up to 2112 KB |
| TRAVEO™ T2G Automotive body controller entry | CYT2BL | Up to 4160 KB |
| TRAVEO™ T2G Automotive body controller high | CYT3BB/4BB | Up to 4160 KB |
| TRAVEO™ T2G Automotive body controller high | CYT4BF | Up to 8384 KB |
| TRAVEO™ T2G Automotive body controller high | CYT6BJ | Up to 16768 KB |
| TRAVEO™ T2G Automotive cluster entry | CYT2CL | Up to 4160 KB |
| TRAVEO™ T2G Automotive cluster 2D | CYT3DL | Up to 4160 KB |
| TRAVEO™ T2G Automotive cluster 2D | CYT4DN | Up to 6336 KB |

# Introduction to TRAVEO™ T2G body controller entry

Event generator (EVTGEN) is a part of peripheral blocks.

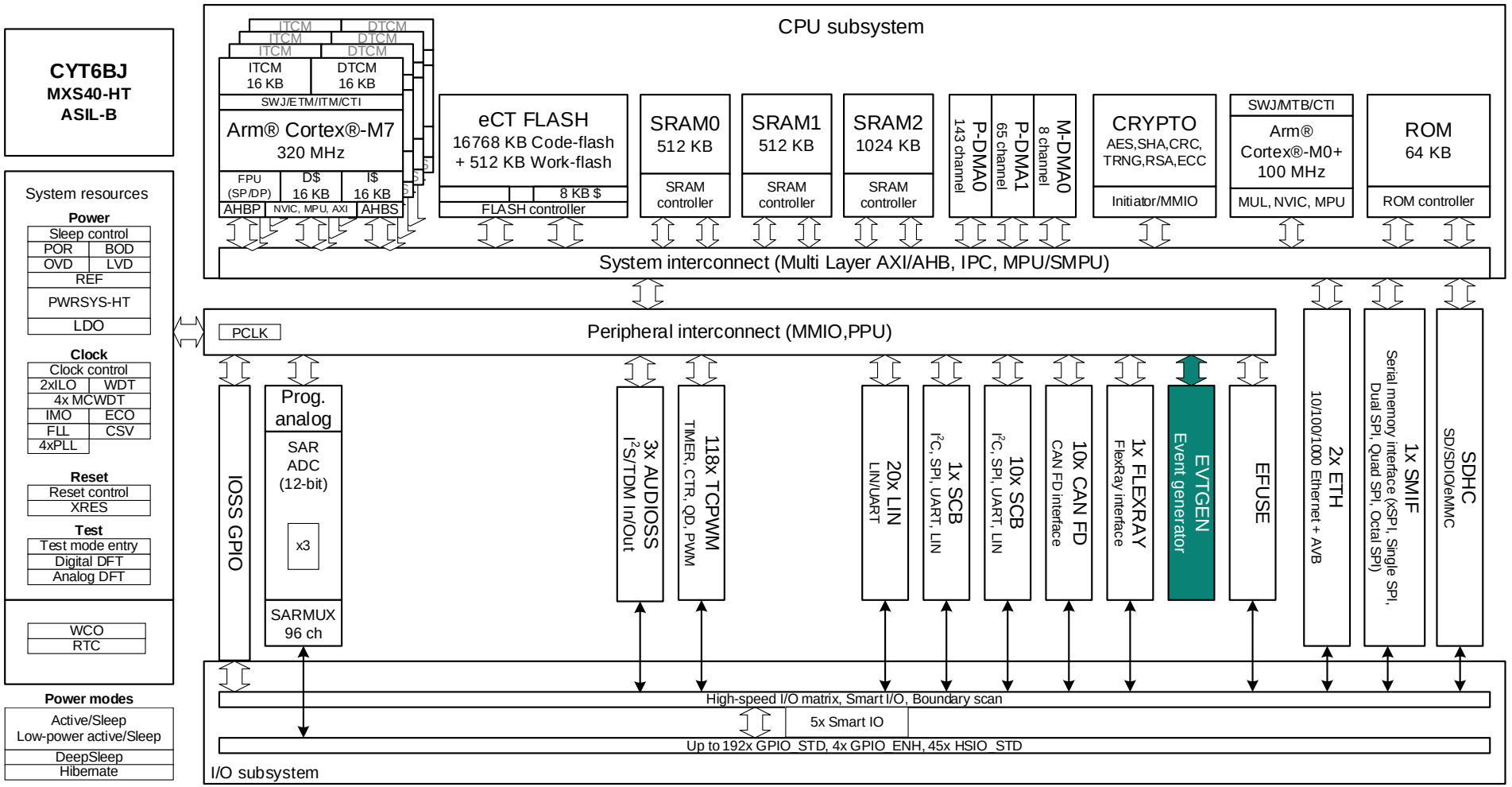



**Hint bar**

See the Event generator (Chapter 28) in the TRAVEO™ T2G architecture technical reference manual for additional details.

# Introduction to TRAVEO™ T2G body controller high

Event generator (EVTGEN) is a part of peripheral blocks.

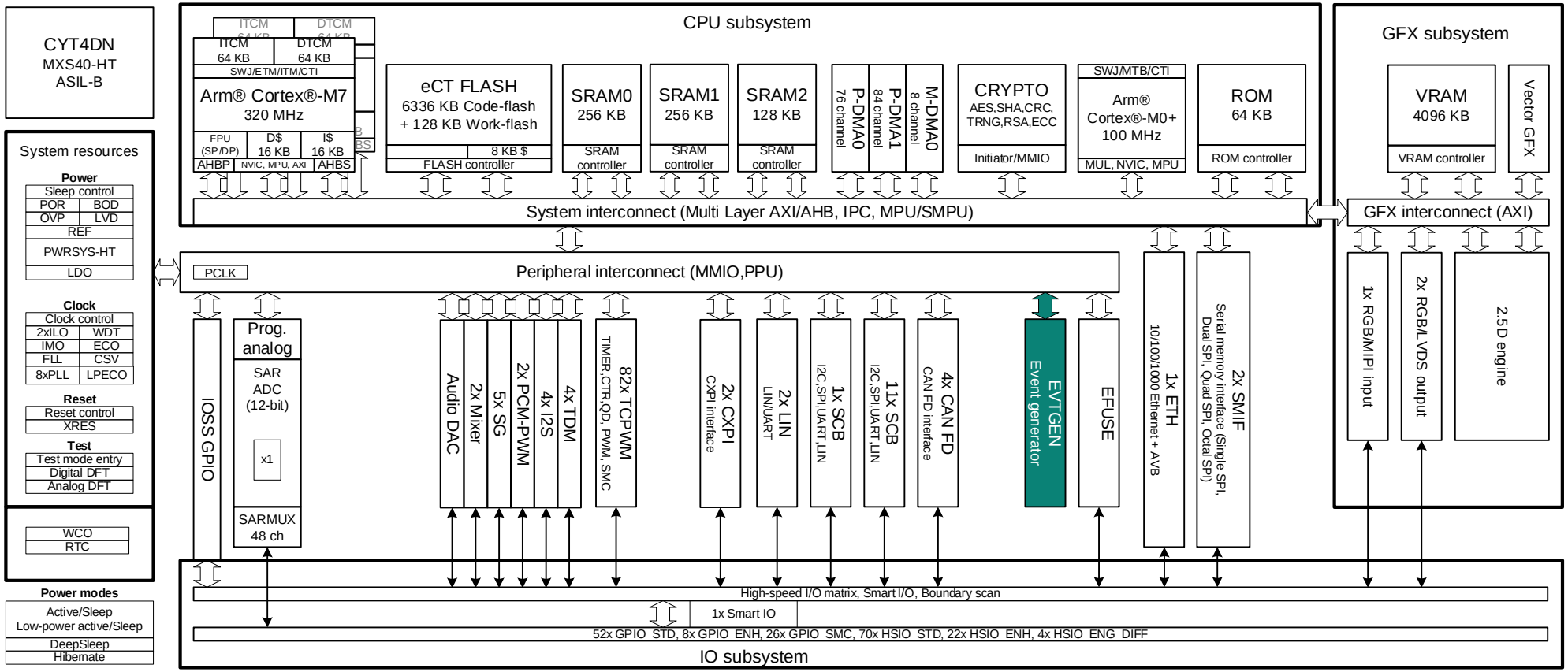



**Hint bar**

See the Event generator (Chapter 28) in the TRAVEO™ T2G architecture technical reference manual for additional details.

# Introduction to TRAVEO™ T2G cluster

Event generator (EVTGEN) is a part of peripheral blocks.

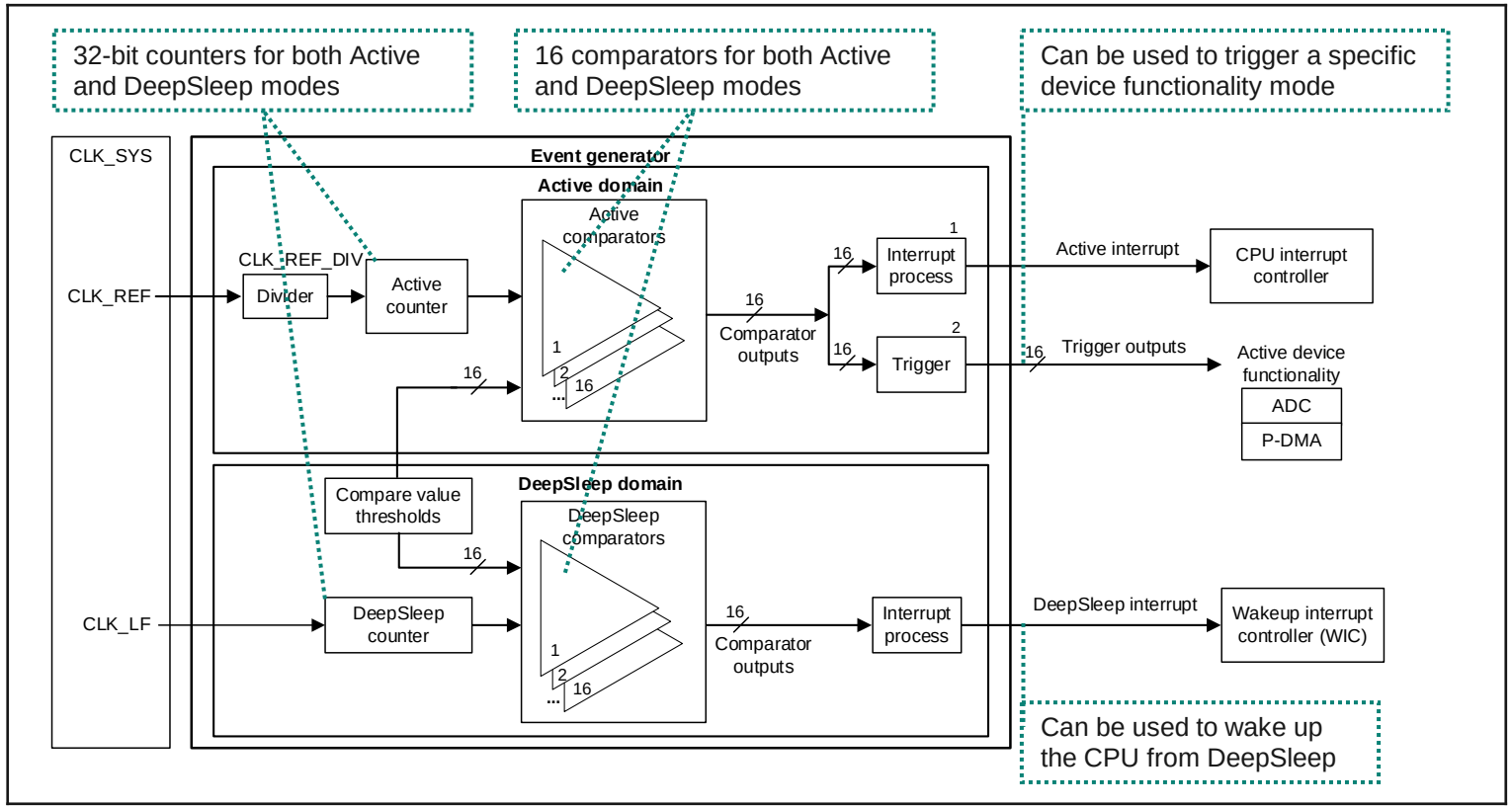



**Hint bar**

See the Event generator (Chapter 28) in the TRAVEO™ T2G architecture technical reference manual for additional details.

# Event generator (EVTGEN) overview

- 32-bit counters, one each for DeepSleep and Active power modes
- Interval range:
  - 10 ns to 76 hours (Active mode)
  - 31 µs to 36 hours (SSleep mode)
- Generates interrupts or triggers



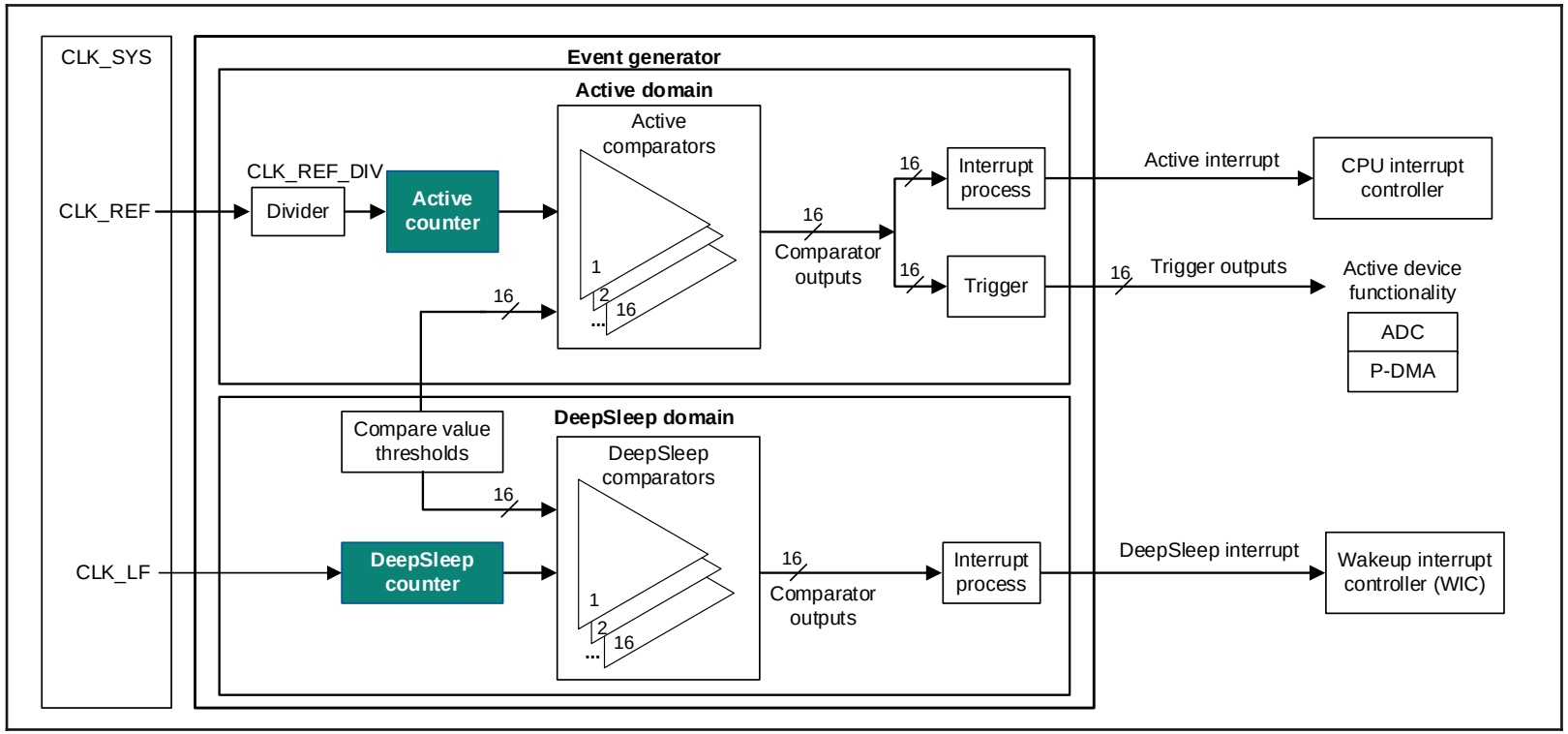

[1] This interrupt can be used like a normal interval timer.
[2] This trigger activates ADC.

**Hint bar**

- See the Event generator (Chapter 28) in the TRAVEO™ T2G architecture technical reference manual for additional details.
- See the Trigger multiplexer (Chapter 29) in the TRAVEO™ T2G architecture technical reference manual for additional trigger details.
- See the Interrupts (Chapter 12) in the TRAVEO™ T2G architecture technical reference manual for additional interrupt details.

# Counters

- Active counter
  - Works on the divided CLK_REF_DIV[1] (CLK_HF1[2])
  - Restarts from ‘0’ after overflow
  - Enables read by software in Active mode
  - Not retained in DeepSleep power mode
- DeepSleep counter
  - Works on the CLK_LF[3] (ILO[4] or WCO[5])
  - Cannot be read by software in Active or DeepSleep mode



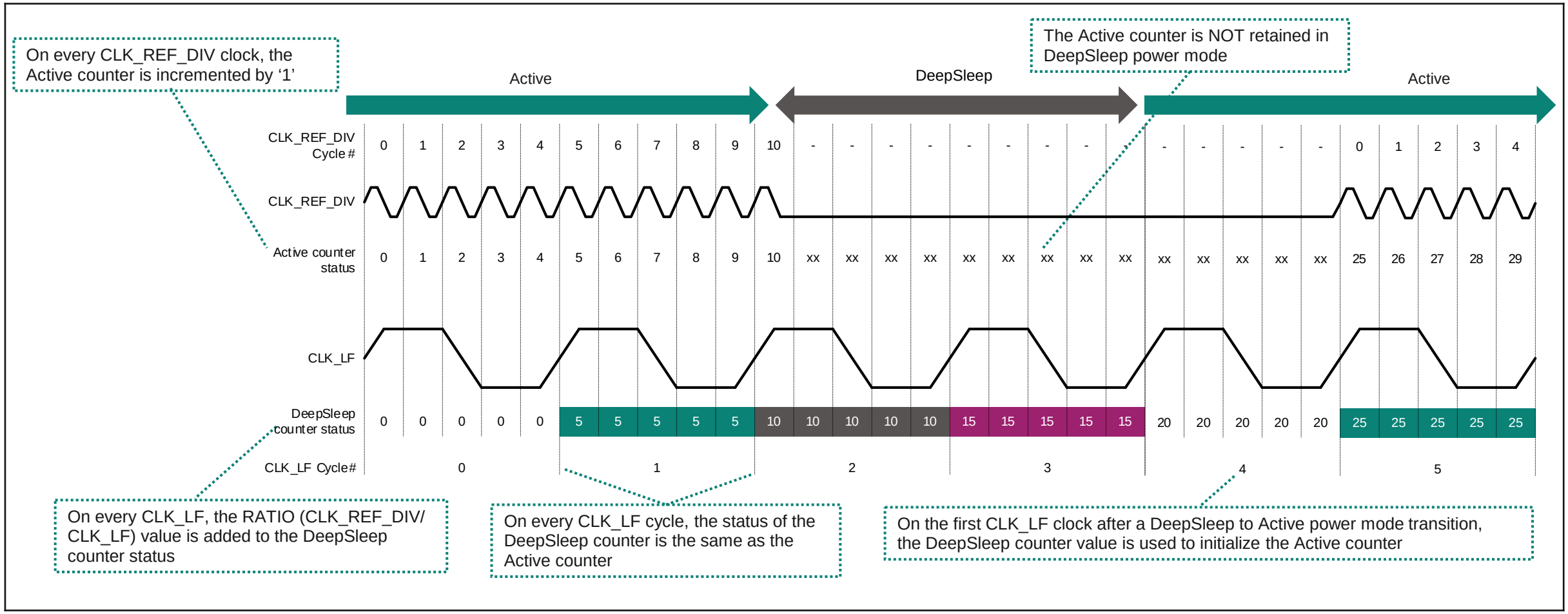

[1] Reference clock
[2] High-frequency clock (max. 100 MHz)
[3] Low-frequency clock
[4] ILO: Internal low-speed oscillator
[5] WCO: Watch crystal oscillator

**Hint bar**

- See the Block diagram (Chapter 28.2) in the TRAVEO™ T2G architecture technical reference manual for additional details
- See the Clocking system (Chapter 18) in the TRAVEO™ T2G architecture technical reference manual for additional clock details
- See the respective device datasheet for each clock frequency

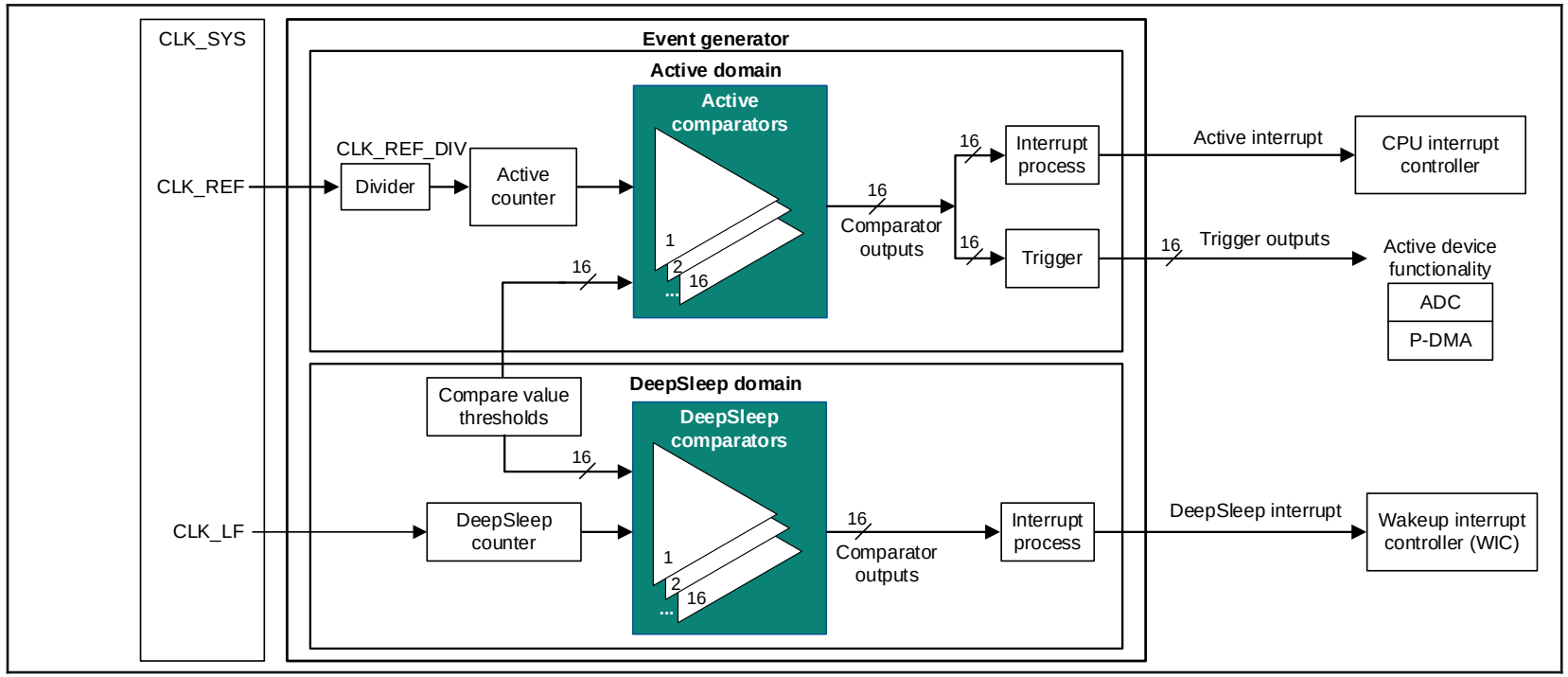
# Relation of Active and DeepSleep counter

- Active and DeepSleep counter status with RATIO = 5 (CLK_REF_DIV is 5 times as fast as CLK_LF)
  - Active and DeepSleep counters are always in sync



# Comparators

| Specification | Active comparators: COMP0 [31:0] | DeepSleep comparators: COMP1 [31:0] |
|---|---|---|
| Maximum number of comparator | 16 | 16 |
| Minimum count time | 10 ns (CLK_HF1: 100 MHz) | 31 µs (minimum); ILO: 32 kHz |
| Maximum count time | 76 hours (CLK_HF1: 4 MHz/256[1]) | 36 hours (maximum); ILO: 32 kHz |
| Target counter to compare | Active counter | DeepSleep counter |
| Outputs | Trigger / Interrupt | Wakeup interrupt |



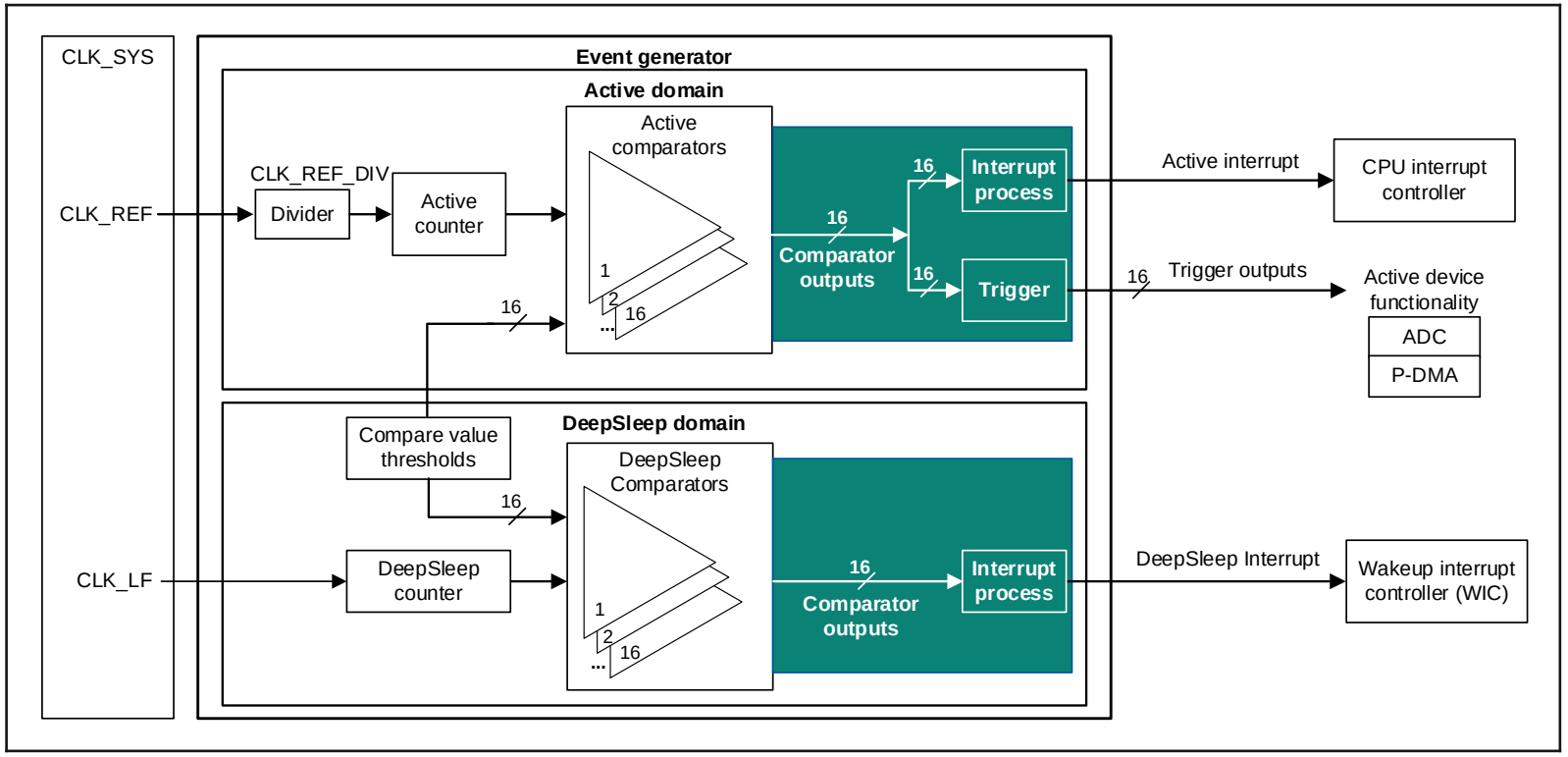

[1] CLK_REF_DIV range is 1 to 256

## Hint Bar

- See the register reference manual and architecture reference manual section 28.2.5 for additional details
- See the respective device datasheet for each clock frequency

# Comparator outputs

- Interrupts
  - An Active interrupt is generated when the Active counter is ≥ COMP0
    - Use case: Periodic task management
  - DeepSleep interrupt occurs when the DeepSleep counter is ≥ COMP1
    - Use case: Wake up from DeepSleep mode
- Trigger
  - Available only in Active power mode
  - Generated when the Active counter is ≥ COMP0
    - Use case: Periodic task management

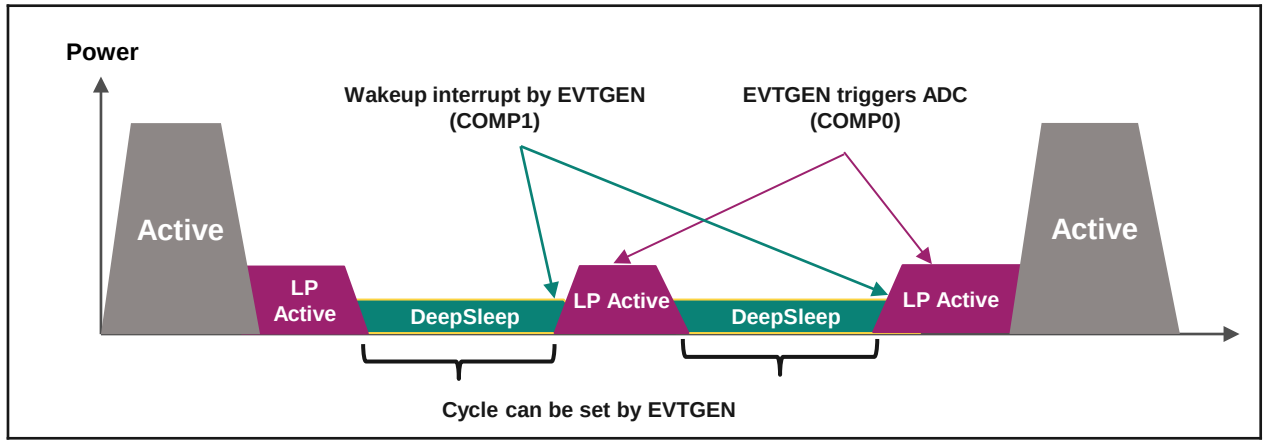



**Hint bar**

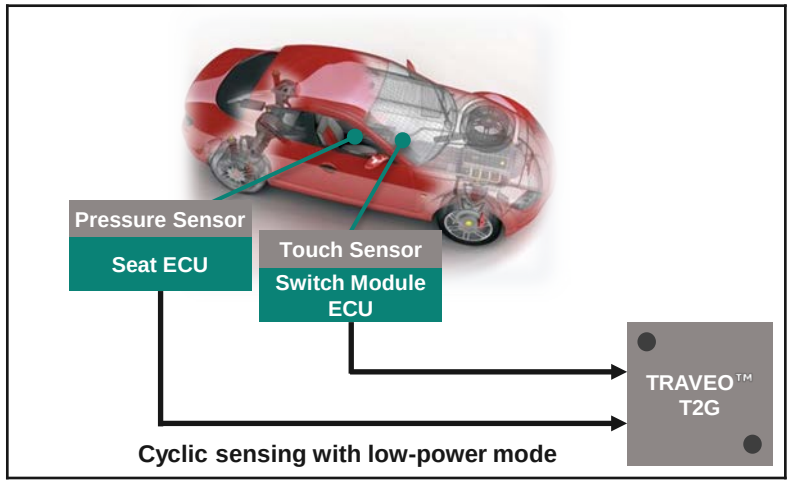
- See the Comparator structure (Chapter 28.2.5) in the TRAVEO™ T2G architecture technical reference manual for additional details.
- See the Trigger multiplexer (Chapter 29) in the TRAVEO™ T2G architecture technical reference manual for additional trigger details.

# Cyclic wakeup operation by EVTGEN

- Enables periodic ADC sensing with low-power
- Periodic wakeup from DeepSleep mode by using the DeepSleep comparator (using COMP1)
- After CM0+ or CM4/CM7 wakes up (in LP Active mode), EVTGEN can generate trigger for ADC (using COMP0)




- Use case
  - Cyclic touch detection on switch module ECU
  - Cyclic pressure sensing on seat ECU

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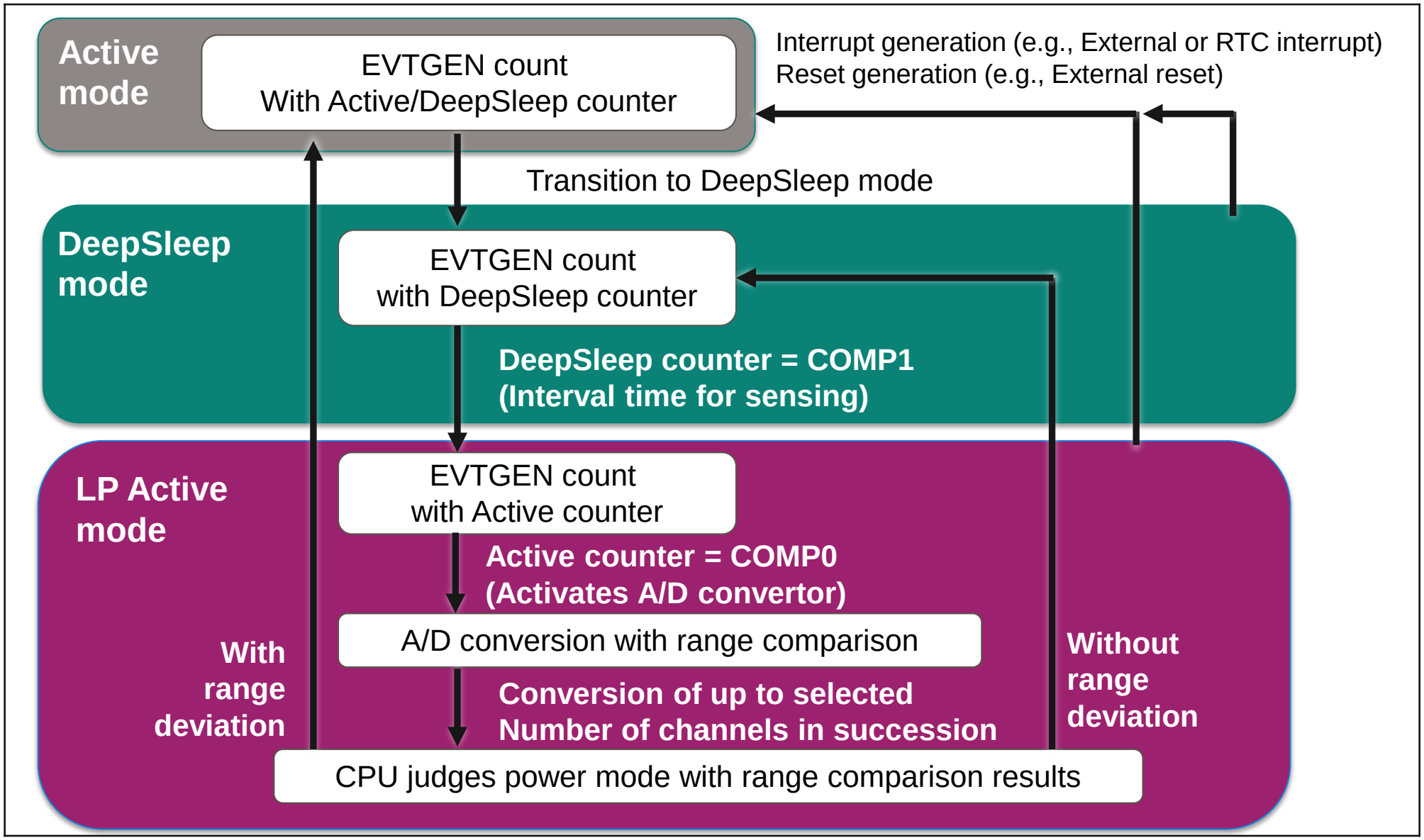
- See the Use case (Chapter 28.2.9) in the TRAVEO™ T2G architecture technical reference manual for additional details.
- See the Device power modes (Chapter 17) in the TRAVEO™ T2G architecture technical reference manual for additional low-power details.
- See the Trigger multiplexer (Chapter 29) in the TRAVEO™ T2G architecture technical reference manual for additional trigger details.
- See the Cyclic Wakeup Sequence for Sensing by ADC section for additional cyclic wakeup sequence details.

# Cyclic wakeup sequence for sensing by ADC



# Revision history

| Revision | ECN | Submission date | Description of change |
|---|---|---|---|
| ** | 6140813 | 04/25/2018 | Initial release |
| *A | 6354961 | 10/18/2018 | Added slides 2, 4, 5 and note descriptions in all slides.<br>Updated slides 3, 9, 10 and 11. |
| *B | 6599849 | 06/13/2019 | Updated slides 2, 3, 4, 9 and 10.<br>Added slide 5. |
| *C | 7032177 | 11/27/2020 | Updated slides 2 to 13. |
| *D | 7065149 | 01/07/2021 | Updated slides 1, 2, 7, 10 and 13. |
| *E | 8113591 | 03/14/2025 | Updated slides 2 to 7 and 9. |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