CIF
Camera and ADC interface
The Camera and ADC Interface Module (CIF) provides a 16-bit wide parallel read interface that can be used to connect camera sensors and external Analog to Digital Converters (ADCs).

- Throughput up to 96 Mpixel/s
- Multiple cropping units with tracking optimized parameters

**Key Features**

- Flexible Data Format Conversion
- JPEG encoder
- Security Watchdog

**Customer Benefits**

- Wide range of sensors supported, compression enabled
- Image compression
- Detection of irregularities or interruptions in the data stream
The Video Image Signal Processing (ISP) unit is the interface to the attached sensor device.

It accepts multiple data types such as: ITU-R BT.601 YCbCr, RAW RGB Bayer, ITU-R BT.656 YCbCr. Additionally, a so-called “data mode” is supported which accepts non-line or frame organized data.

The input part of the ISP is fully programmable in terms of signal polarities, active video data positions and luminance/chrominance order.

The ISP can be configured to generate interrupts for multiple different conditions. To be noted that all interrupts are mapped to the single physical request line ISP_INT.
The baseline JPEG encoder module consists of a JPEG encoder pipeline, which is controlled by a register interface that is accessed via handshake interface.

The encoding process starts with a raster to block (R2B) conversion of the YCbCr 4:2:2 pixel data provided by an imaging device, where the pixel data is reordered into 8x8 pixel blocks.

Every 8x8 block undergoes a baseline Discrete Cosine Transform (DCT), a ZigZag (ZZ) reordering, a quantization (Q) and a variable length encoding (VLE), based on Huffman algorithm.

The last step is the generation of the JFIF 1.02 compliant data stream by inserting markers and tables.

The JPEG encoder can be configured to generate interrupts for several error conditions, which are routed to MJPEG_INT.
The Security Watchdog unit is used to monitor the incoming image data.

In order to do so, the horizontal and vertical synchronization signals in the input formatter unit are observed and are compared to programmable time-out frames.

When a time-out frame gets breached, an interrupt is generated to immediately report the event (through the ISP_INT).

The timing information is retrieved via two separate 16 bit counters used to measure horizontal and vertical timeframes in parallel.

The timing unit granularity is controlled via a predivider and it ranges from $1 \times T_{CIF_CLK}$ to $216 \times T_{CIF_CLK}$.
CIF
System integration

- The CIF is a Back Bone Bus (BBB) master with 6 integrated DMA channels with burst capabilities.
- The DMA channel are ensuring the transfer of data without overhead to the LMU RAM.
- Additionally, the CIF is capable of communicating errors and events to the Interrupt Router.
Application example
Video capturing/encoding

› The CIF provides a sensor/camera interface for a wide range of video application and it is optimized for high speed data transmission with low power consumption.

› The CIF requires fast system memory for image storage.

› The integrated JPEG encoding engine is able to generate a full JFIF 1.02 compliant JPEG file that can be displayed directly by any image viewer.
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