WTU
Watchdog Timer Unit

AURIX™ TC4xx Microcontroller

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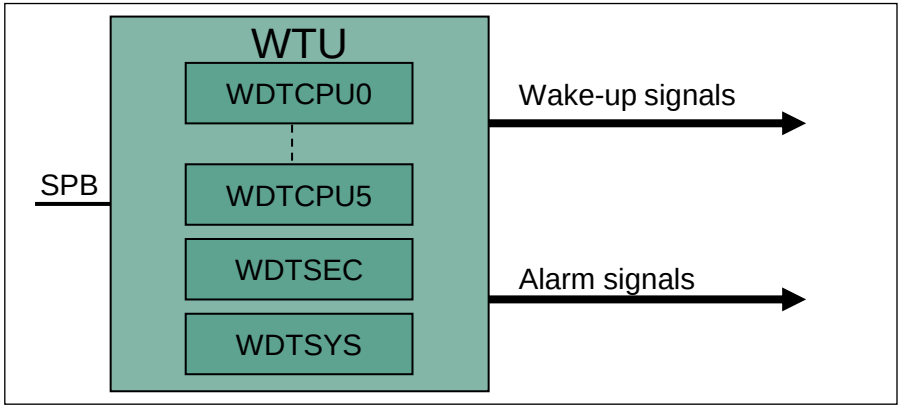


Highlights

- The Watchdog Timer Unit (WTU) provides several independent watchdog timers (WDTs)
- The main system use is Program Flow Monitoring (PFM), which tracks if the software is executed in the correct order
- Up to 8 independent WDTs

Key Features

Programmable 16-bit timer-base (reload) value with password

Independent WDT per core and a WDT for system

Alarm triggering for violations

Customer Benefits

- Temporal and logical supervision with protection against unintended changes
- Independent monitoring of cores without SW coordination
- Implementation of safety mechanisms

WTU
Independent WDT per core and WDT per system

- The Watchdog Timer Unit consists of a Universal Bus Slave (UBS) and a total of up to 8 independent Watchdog Timers (WDT) modules:
  - One watchdog timer per lock-stepped CPU: WDTCPU0-5
  - One watchdog timer for CSRM security CPU – WDTSEC
  - One system watchdog timer – WDTSYS
- For CPUs implemented with Hardware Virtualization Support, the WDT can be assigned to one or multiple of its Virtual Machines (VMs). In the case where multiple VMs run on a single CPU, to achieve freedom from interference, the respective WDT should be assigned to only one of the VMs
- The individual CPU watchdog timer functions enable the monitoring of separate CPU execution threads without the need for SW to coordinate the shared use of a common system watchdog. Periodic servicing of a CPU-WDT and providing the correct password confirm that the corresponding CPU is executing the SW sequence as expected
- Similar to the CPU watchdog, the WDTSEC is monitoring the temporal and logical code execution of the core inside CSRM
- The system watchdog, unlike CSRM security CPU and CPUs WDTs, is not fixed to a certain CPU and is freely configurable

WTU
Programmable 16-bit timer-base (reload) value with password

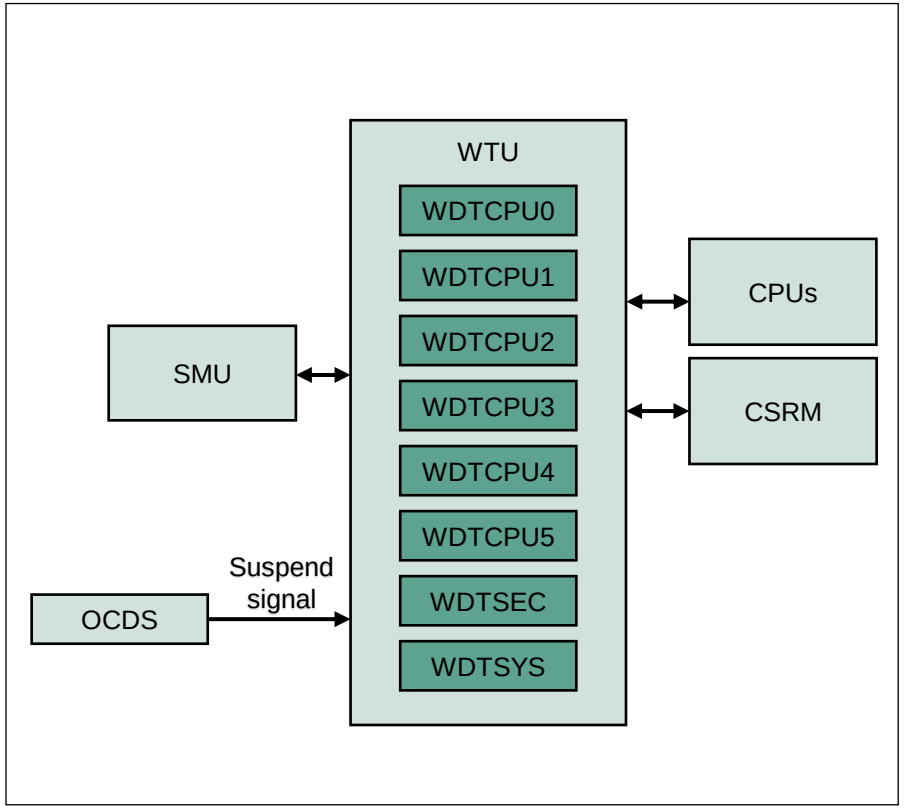
- The main function of each WDT is Program Flow Monitoring (PFM), which is split in two types of checks:
  - Temporal supervision: check if the software finishes the tasks in a defined time-frame (for example not hanging in an infinite loop)
  - Logical supervision: check if the software tasks are executed in the expected order
- WDT is a 16-bit up-counting timer with configurable input frequency
- WDT has a password protection mechanism with a 15-bit user-definable password and configurable auto-sequencing:
  - This password can be used to monitor the logical flow of the SW (for example to detect unexpected SW loops)
  - Using automatic password sequencing means that the password automatically changes after each password check. The expected next password follows a pseudo-random sequence

WTU
Alarm triggering for violations

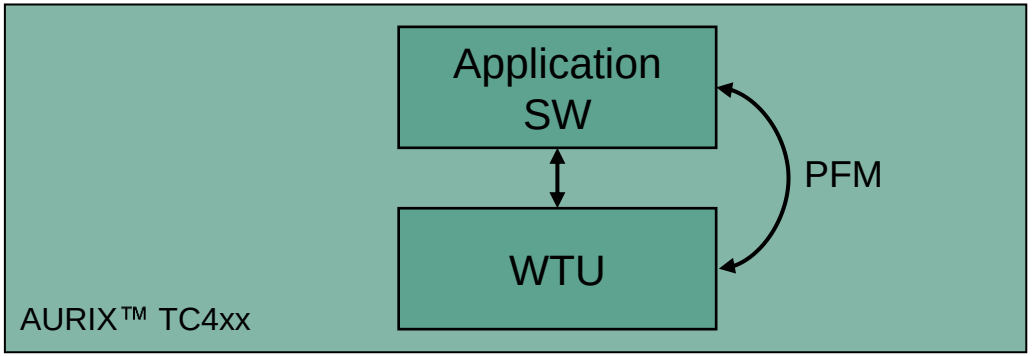
- Each WDT provides a dedicated register interface, password, timer logic and alarm signal going to the Safety Management Unit (SMU)
- Alarms are triggered when:
  - Temporal supervision: the application software is unable to service its WDT before a certain time deadline or inside a certain time window
  - Logical supervision: the WDT access password is configured to auto-increment after each access. If the wrong password is provided, an alarm is signaled
- There is also an alarm output which represents the logical “OR” combined alarm output of the WDTCPU0-5, WDTSEC and WDTSYS
- Each WDT supports options to check code execution sequence and intermediate code execution time

WTU
System integration

- The WTU uses programmable 16-bit timers to monitor the temporal and logical behavior of the cores or of the system
- In case of deviations from the expected behavior, alarms are triggered. These alarms can have different configured reactions (for example a reset)
- In the cases of debugging and testing of the application, the On-Chip Debug System can suspend the watchdogs' functions



Application example
Program Flow Monitoring



Overview

- For real-time systems, especially safety relevant ones, both the time and logical behavior are important
- PFM enables the check of the application software against misbehaviors like entering an infinite loop or going to the wrong branch

Advantages

- Ensure that the application SW is executing in the right order, and it is not stuck in a specific operation like an unexpected loop
- Establish the required corrections of the application SW or the reactions (via safety mechanisms) to such misbehaviors

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