AURIX™
System Architecture

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06

Please read the Important Notice and Warnings at the end of this document
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System Architecture

Security & Safety: SMU, HSM
Timers: STM, GTP
Communication Interfaces: MCMCAN, Gigabit Ethernet MAC, SPI, UART, I2C, ...

Memories: RAM, Flash EEEPROM
Peripherals: DMA, ADC, GTM, CCU6

Up to 6 TriCores

AURIX™ TC3xx

Highlights
› Multicore Microcontroller with embedded Flash
› TriCore™ (DSP processor) @300 MHz
› Up to 16 MB Flash, more than 6 MB RAM
› DMA, HW-FFT, ADC, Gigabit Ethernet MAC,...

Key Features
Embedded flash platform for real time applications
Up to 6 TriCore™ with DSP instructions
Rich peripheral set and large RAMs

Customer Benefits
› Embedded flash allows compact design and fast code execution
› Enables heavy processing tasks like radar or signal processing applications
› Reduces the need for external components for cost competitive BOMs
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Embedded flash platform for real time applications

- All the flash memory is divided in banks (PF0-6 & DF0-1), which are concurrently readable.
- Each bank has its own Shared Resource Interconnect (SRI) ports, Error Correction Code (ECC) decoders and pre-fetch logic.
- In case of ECC errors, the Safety Management Unit (SMU) and theInterrupt Router (IR) can be configured to generate errors, respectively interrupts.
- This embedded flash platform offers a high performance code storage and flexible memory selection, controlled by safety mechanisms.

Note: This is the general description of the Flash memory structure on AURIX™ TC3xx. This depends on the device. Please refer to the according User Manual.
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Up to 6 TriCore™ with DSP instructions

› The TriCore™ architecture combines three powerful concepts:
  – Microcontroller
  – RISC processor
  – DSP (Digital Signal Processor)

› TC 1.6.2P:
  – High performance architecture
    – Superscalar Harvard
  – 6 pipeline stages for up to 300 MHz
  – 2.3 DMIPS/MHz
  – Instruction and data cache

› 32bit Floating Point Unit in all CPUs:
  – Single precision according to IEEE-754
  – 2 FLOPs per cycle (pipelined)
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Rich peripheral set and large RAMs

› Peripherals:
  - ADC: Analog-Digital Convertor – 12-bit up to 1 MSPS
  - GTM, GPT12 and CCU6: Signal Capture / Compare and PWM generation
  - FFT engine: Fourier Transform acceleration
  - STM: Timer Module
  - DMA: Direct Memory Access Module
  - Advanced On – Chip Debug System (OCDS)

› Communication Interfaces:
  - QSPI: Advanced SPI interface (Serial Peripheral Interface)
  - MCMCAN: CAN Interface
  - ASCLIN: Lin and UART
  - Gigabit Ethernet MAC: Ethernet 1000 Mbit/s interface
  - I2C: Inter-Integrated Circuit Bus
  - EBU: External Bus Unit (32-bit Data, 24-bit Address)

› On-Chip Memories:
  - More than 6 MB integrated RAM including CPUs tightly coupled Scratch-Pad RAM
  - Up to 16 MB integrated Flash memory with EEPROM Emulation
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Rich Peripheral set and large RAMs

AURIX™ Multi-CPU architecture contains:

› Distributed Scratch-Pad RAMs for data (DSPR) and program (PSPR)
  – Can be accessed by all CPUs
› CPUs execute code from cached PFlash modules
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System integration

› AURIX™ TC3xx combines three powerful technologies within one silicon die, improving power consumption, speed and reducing the costs for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

› AURIX™ TC3xx devices are designed to meet the needs of embedded control systems applications, where real-time responsiveness, computational power and data bandwidth are key design elements.
Overview

Car systems like airbag and engine management need to operate in a safe and secure way:

› Safe: Airbag must not trigger under regular driving conditions

› Secure: Unauthorized persons must not be able to hack the car’s systems

Advantages

Beside AURIX™ TC3xx versatile set of on-chip peripherals connected to TriCore™ CPUs, the AURIX™ family also offers safety and security modules to deal with critical embedded applications.
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