IR
Interrupt Router

Key Features
Mapping Service Requests to Service Providers
Assign a priority for each Service Request

Highlights
› Schedules the Service Requests (SRs) from external resources, internal resources and Software to the CPUs and the DMA module (Service Providers).
› SR cleared automatically on HW acknowledge by Interrupt Service Providers (ISP)
› Software Interrupts: 8 SW Service Requests per CPU
› Low latency arbitration around 50 ns

Customer Benefits
› Each interrupt could be configured to triggered one Service Provider (CPUx, DMA)
› Arbitration for pending Service Requests mapped to the same ISP
Each service request must be configured to be serviced by one of the service provider:

- Type of Service (TOS)
  - CPUx \((x=0..5)\): The service request is executed by the selected CPU
  - DMA: The service request triggers a DMA channel transfer

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**Diagram:**

- **Interrupt Router**
  - Interrupt from module 1: TOS = CPU1 → CPU0
  - Interrupt from module 2: TOS = CPU3 → CPU1
  - Interrupt from module 3: TOS = DMA → CPU2
  - Interrupt from module 4: TOS = CPU4 → CPU3
  - Interrupt from module 5: TOS = CPU2 → CPU4
  - Interrupt from module 6: TOS = CPU5 → CPU5
  - Interrupt from module 7: TOS = CPU0 → DMA
Assign a priority for each service request

- A Service Request Priority Number (SRPN) from 0 to 255 must be assigned to each service request:
  - Depending on the selected Service Provider (TOS) the SRPN presents the following:
    - CPUx: The interrupt priority of the related Service request (SRPN 0 is neutral)
    - DMA: The number of the DMA channel to be triggered.

- **Arbitration**: For each ISPx, IR arbitrates among the group of pending Service Requests mapped to this ISPx. Winner of an arbitration round is the pending SR with the highest priority (SRPN number).
IR
System integration

- Each peripheral interrupt has a dedicated Service Request Node (SRN)
  - TOS and SRPN configuration, Interrupt Overflow, SW Interrupt Set/Clear
- Each Service Provider has a dedicated Interrupt Control Unit (ICU)
  - Parallel and independent arbitration for pending service requests mapped to different ISPs

Interrupt Trigger signals from:
- Peripherals
- External
- SW
Application example
DMA transfer

In this example data is transferred from the QSPI FIFO registers to internal memory without any CPU intervention.

1. Rx Data Available Interrupt
2. Trigger DMA Channel 1 Transfer
3. DMA transfer: Copy Data from QSPI Rx FIFO to RAM
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