## STM System Timer

### Highlights

- The System Timer STM is used to generate a time base e.g. for an OS, as well as to generate trigger events.
- There are as many STM modules as there are CPUs in the system. Thus each CPU can use one STM for its time base.

### Key Features

- Free-running 64-bit counter
- Flexible interrupt service request generation

### Customer Benefits

- Fits perfectly the generation of OS time base and triggering events
- Indication of events with assigned priority for highest flexibility

---

[Image of STM block diagram]

STM

\[ f_{STM} \]

Clock

64-bit Counter

Compare-0

Interrupt-0

Compare-1

Interrupt-1

Copyright © Infineon Technologies AG 2019. All rights reserved.
STM
Free-running 64-bit counter

The STM has a 64-bit counter which is clocked by $f_{STM}$ from the CCU (Clock Control Unit).

The system timer value can be read via 7 registers, each selecting a 32-bit range of the system timer value.

Each of these can be used as counters with different resolution and range.

Due to the 64-bit width, the entire counter needs to be read with two load instructions. The timer will continue counting between the load operations, therefore there is a chance that the read values will not match. In order to enable synchronous and consistent reading of the STM content, a capture register was implemented.

This capture register holds the upper value of the timer why the lower part is read. Therefore the second load operation will read the content of the capture register.
The STM counter can be compared against the values in two comparison registers.

If the values match, a compare match event is generated from either of the comparisons.

Two parameters are programmable for the compare operations:

- **START**: First bit (LSB) location to be taken for the compare operation.
- **SIZE**: Number of bits to be compared (starting from zero).

Using the START and SIZE configuration, it is even possible to check for single bit transitions (setting the size to 0 and the start to the bit of interest.

In the right side figure – the following parameters are assumed to be configured:

- \( \text{SIZE0} = 17; \ \text{START0} = 10 \)
- \( \text{SIZE1} = 7; \ \text{START1} = 7 \)
Clock to the STM ($f_{STM}$) is generated from the CCU

- This is generated from the system PLL after it is enabled
- The clock divider should be configured in both modules: CCU and STM

It must be ensured that the $f_{STM}$ is on an integer to the System Peripheral Bus (SPB) clock ($f_{SPB}$)

- If the integer ratio is not ensured, then the counter value can be wrong
Application example
Operating system time base generation

Overview
STM can be used to generate the time base for a Real-Time Operating System (RTOS), for example as a base for the scheduler.

Advantages
› Different rates of timer interrupt can be configured
› In a multicore system, each CPU can have its own time base
IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.