

# SCU

## System Control Units

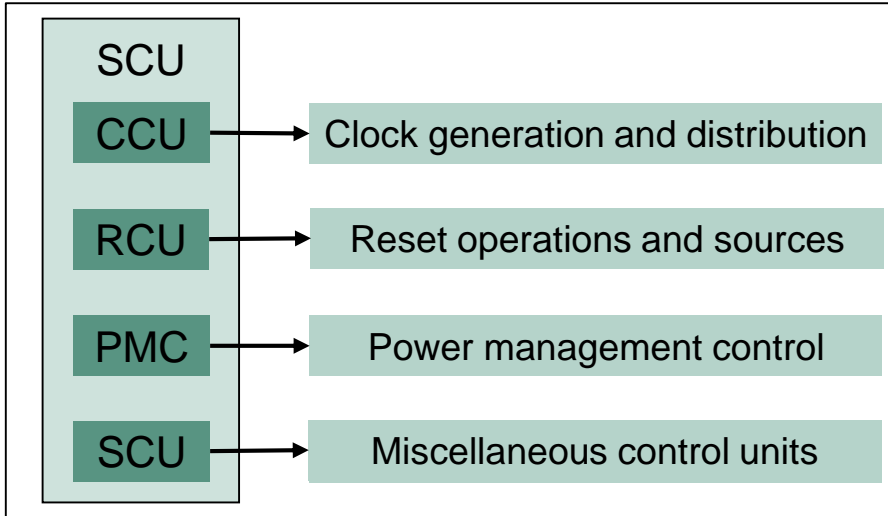
AURIX™ Microcontroller Training  
V1.0



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# SCU

## System Control Units



### Highlights

- › The SCU comprises various units, which handle clock generation for all modules, reset operations (incl. effects and triggers), power management control (e.g. reducing power consumption) and many other miscellaneous submodules such as watchdogs.

### Key Features

Clock generation and distribution

Reset operations and sources

Power management control

Miscellaneous control units

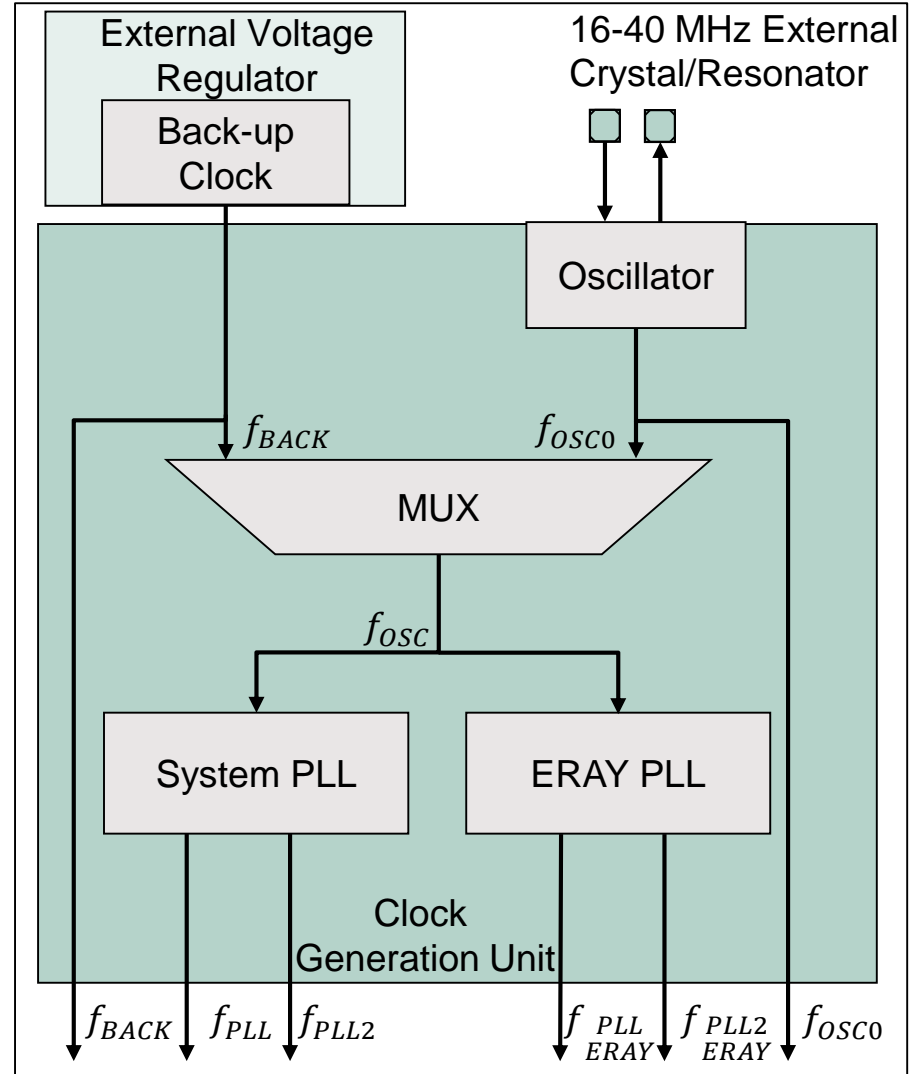
### Customer Benefits

- › Flexible clock configuration according to application needs
- › Scalable reset concept based on different triggers
- › Minimize power use during operation
- › Ensure safe operation

# SCU

## CCU – Clock Speed Upscaling

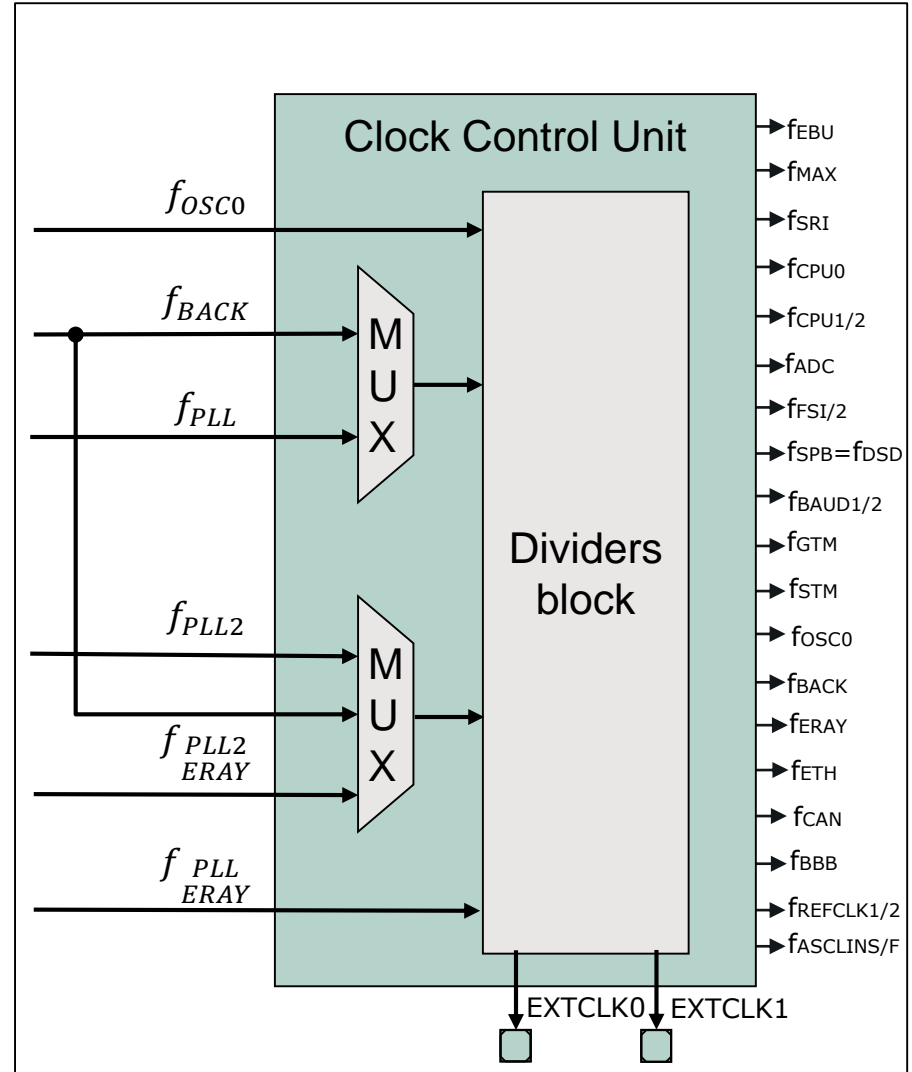
- Aside from the pure clock generation options, there are several support functions which aim to enable an easier and more convenient control
- Generally, the CPU operating speed is about 10 times higher than the speed of the crystal used as clock source
- Therefore 2 Phase Lock Loops (PLLs) are provided for upscaling the clock frequency
- The role of the PLL is to convert a low-frequency external clock signal into a high-speed internal clock in order to maximize the performance
- The PLLs from AURIX™ also have fail-safe logic that detects degenerated external clock behaviors such as abnormal frequency deviations or total loss of the external clock
- In these cases, emergency actions can be defined and implemented



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## CCU – Clock distribution

- › Based on the clock source and the clock speed upscaling, different clocks are defined and, furthermore, they need to be distributed through the system to the single peripherals and CPUs in a way that enables these modules to operate in the best way in terms of performance and power consumption
- › For the clock distribution, the system is split into several sub-clock domains where the clock speed could be configured individually (with the intrinsic restrictions established by the internal interfaces)
- › The clock distribution is done via the Clock Control Unit (CCU), which receives the clocks created by the 2 PLLs, the back-up clock and the oscillator clock. These clocks are either forwarded directly or divided in order to supply the sub-clock domains
- › This approach increases the flexibility of the system by enabling the user to configure the clock individually for the different modules



## RCU – Reset types and effects

- › AURIX™ has a scalable reset concept, where different types of reset are encapsulated one into the other. The **Cold Power-On Reset** is the highest reset type, where the Embedded Voltage Regulator (EVR), internal clocks and RAMs are reset, additionally to the modules affected by the **Application Reset**, **System Reset** and **Warm Power-On Reset**
- › SW Module Reset and Debug Reset enable the user to directly trigger a reset of the connected modules

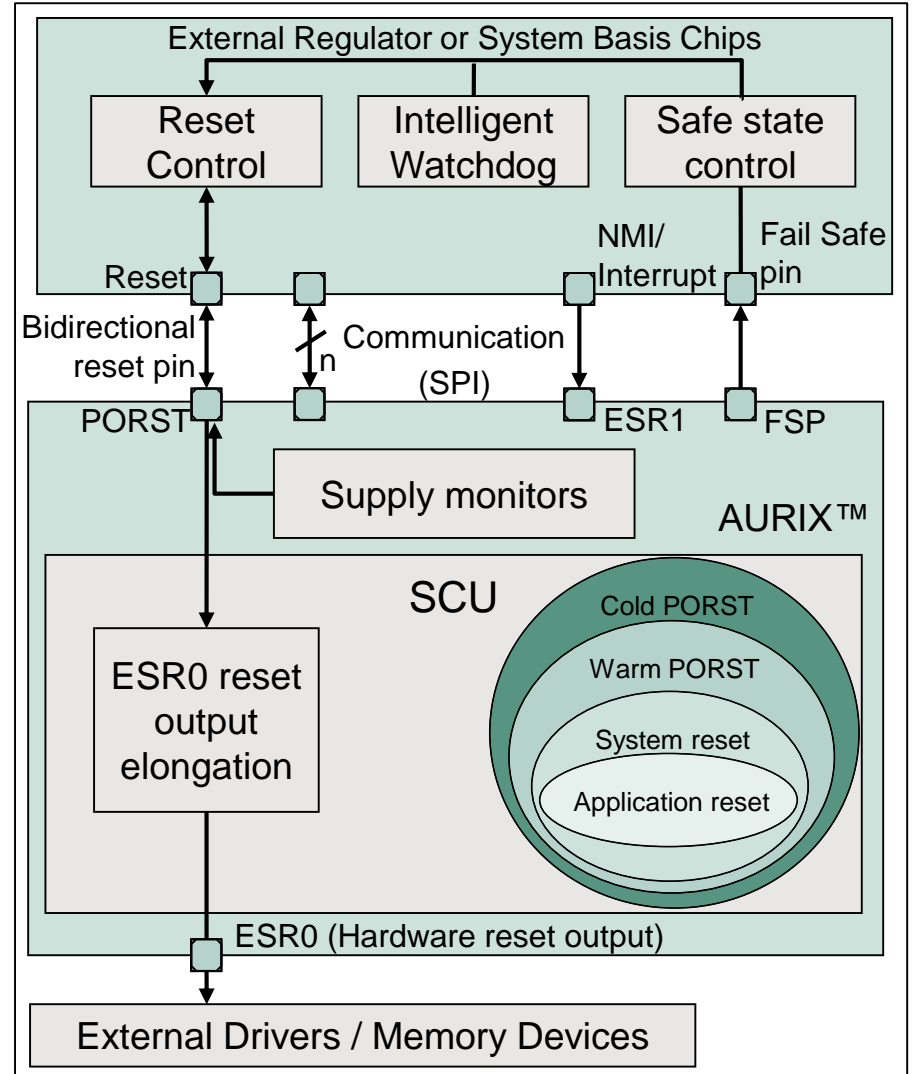
Reset Type	Additional Modules affected by <b>Cold Power-On Reset</b>	Additional Modules affected by <b>Warm Power-On Reset</b>	Additional Modules affected by <b>System Reset</b>	Modules affected by <b>Application Reset</b>
<b>Cold Power-On Reset</b>	<ul style="list-style-type: none"> <li>› Embedded Voltage Regulator</li> <li>› Internal clocks</li> <li>› RAMs:                             <ul style="list-style-type: none"> <li>- DSPRs/PSPRs</li> <li>- LMU/BMU</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>› JTAG interface</li> <li>› OCDS</li> <li>› MCDS</li> <li>› SMU – Fault Signaling Protocol Pin</li> </ul>	<ul style="list-style-type: none"> <li>› Flash memory</li> <li>› Clock source</li> <li>› PLL</li> <li>› External Service Requests pins</li> </ul>	<ul style="list-style-type: none"> <li>› All CPUs</li> <li>› All Peripherals</li> <li>› SCU</li> <li>› Port pins in reset</li> <li>› RAMs:                             <ul style="list-style-type: none"> <li>- Dcache invalid</li> <li>- Pcache invalid</li> </ul> </li> </ul>
<b>Warm Power-On Reset</b>				
<b>System Reset</b>				
<b>Application Reset</b>				
SW Module Reset	Available for all CPUs, DMA channel, QSPI, CAN, ASCLIN, Ethernet, GTM, SENT, ADC, HSSL, CCU6...			
Debug Reset	OCDS and MCDS reset, all CPUs and peripherals (except SCU) are put into reset			

*A higher reset encapsulates a lower reset*

# SCU

## RCU – Reset types and sources

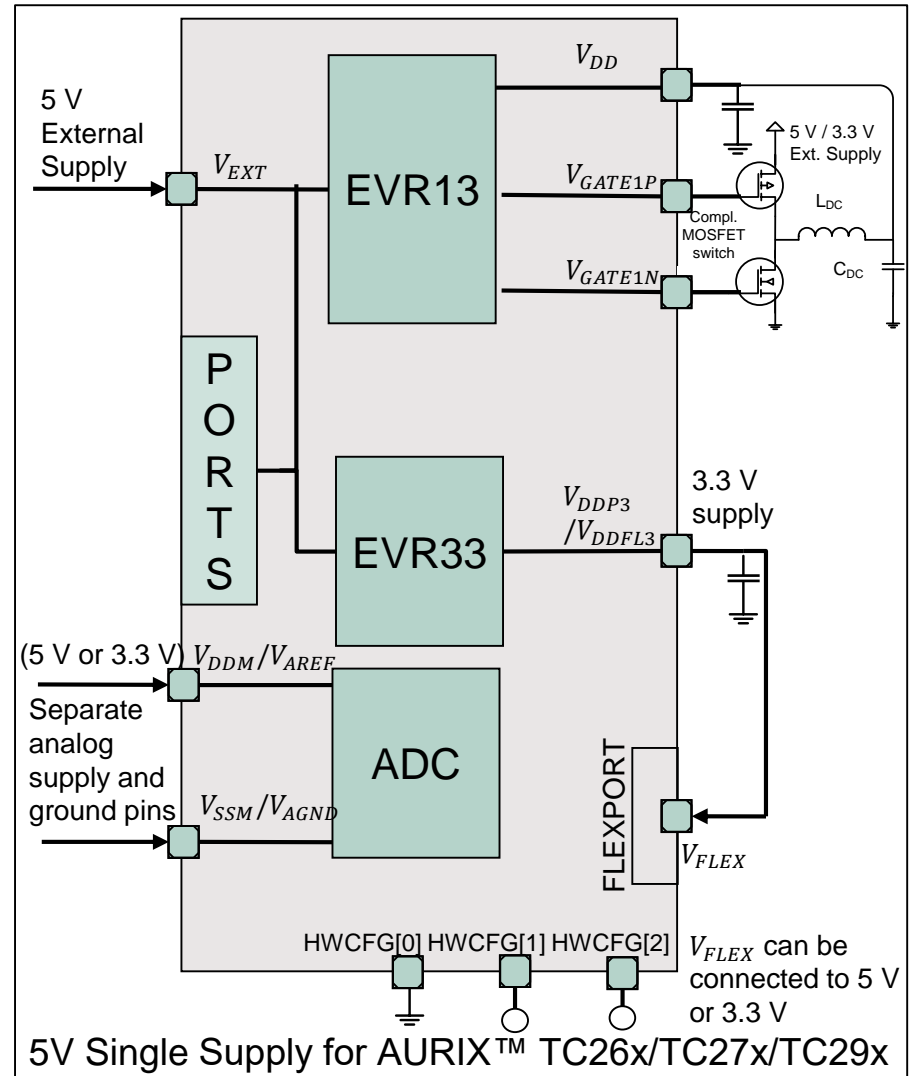
Reset Type	Source of reset
<b>Cold Power-on Reset</b>	<ul style="list-style-type: none"> <li>&gt; Startup</li> <li>&gt; Temporary power fail on any of the 3 supplies (Ext. Supply &lt; 3.0 V; EVR33 &lt; 3.0V; EVR13 &lt; 1.17 V)</li> </ul>
<b>Warm Power-on Reset</b>	<ul style="list-style-type: none"> <li>&gt; PORST pad asserted</li> </ul>
<b>System Reset</b>	<ul style="list-style-type: none"> <li>&gt; ESR0/ESR1</li> <li>&gt; SMU</li> <li>&gt; STMx</li> <li>&gt; Watchdog (SMU)</li> <li>&gt; Software reset</li> </ul>
<b>Application Reset</b>	<ul style="list-style-type: none"> <li>&gt; ESR0/ESR1</li> <li>&gt; SMU</li> <li>&gt; STMx</li> <li>&gt; Software reset</li> <li>&gt; Tuning protection</li> </ul>
<b>SW Module Reset</b>	<ul style="list-style-type: none"> <li>&gt; Configurable by registers</li> </ul>
<b>Debug Reset</b>	<ul style="list-style-type: none"> <li>&gt; OCDS request trigger</li> <li>&gt; JTAG reset</li> </ul>



## PMC – Single source power supply concept

- > AURIX devices support different supply modes:
  - Single 5 V source supply
  - Single 3.3 V source supply
  - Legacy tri-supply mode (for backward compatibility)
  - Dual supply modes
- > AURIX™ contains 2 separate parallel Embedded Voltage Regulators (EVR33 and EVR13) generating 3.3 V and 1.3 V supply voltages from the external supply
- > All supply and generated voltages are monitored internally against overshoot and brownout conditions based on programmable thresholds
- > The reaction to these situations is triggering either a cold Power-On Reset or an alarm
- > This approach reduces the complexity of the system, since additional regulators are not needed to obtain the 3.3 V or 1.3 V voltages

1.3 V supply



## PMC – Idle, Sleep & Standby modes

- › The power management scheme allows activation of power down modes so that the system operates with the minimum required power for the corresponding application state
- › A progressive reduction in power consumption is achieved by invoking Idle, Sleep or Standby modes
- › The Idle mode is specific to each individual CPU, while the Sleep and Standby modes influence the complete system

Mode/Current	Description	Entry/Exit
<b>CPUx Run</b>	Normal operation	-
<b>CPUx Idle</b> 20-65 mA /CPU	The CPU clock is disabled. All peripherals remain active.	Entry: via Software, SMU Exit: on CPUx Interrupt, Trap, Reset
<b>System Sleep</b> >15 mA @ T = 85°C	Peripheral clocks are gated if configured by control registers. All CPUs are set to IDLE	Entry: via Software Exit: on CPUx Interrupt, Trap, Reset
<b>System Standby</b> 150 mA @ T = 25°C	Main domain is powered off. Standby RAM may be active	Entry: via Software, NMI Exit: on edge detection on NMI/pins, PORST assertion In case of separate standby supply pin: entry & exit are done on the VEXT supply ramp-down, respectively ramp-up



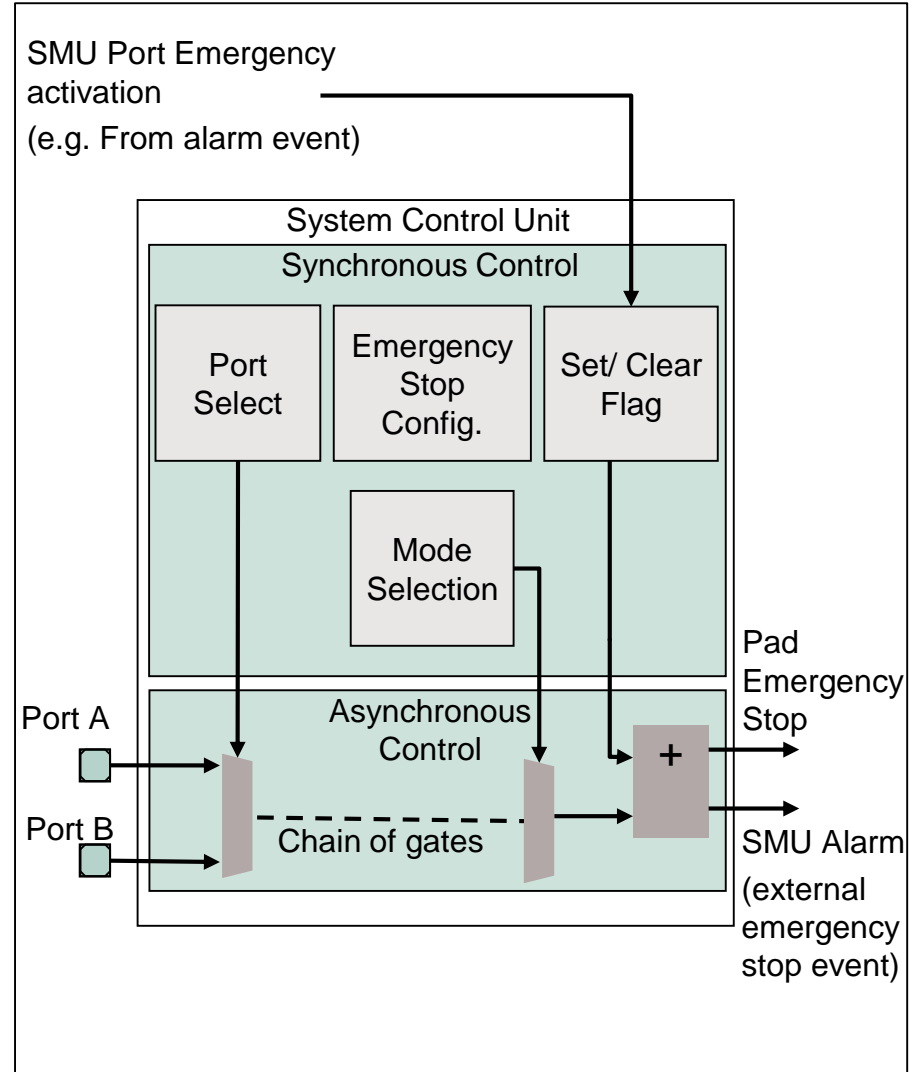
## SCU – Watchdog Timers

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- › The WatchDog Timers (WDTs) provide a highly reliable and secure way of detecting and recovering from software or hardware failure
- › They can be used to abort any accidental malfunction of a CPU or internal module within a user-specified time period
- › Additionally, each of the WDTs incorporates an End-of-Initialization (ENDINIT) feature which protects the critical registers from unintended writes
- › To protect these functions a sophisticated scheme is implemented that requires a password and guard bits during the accesses to the WDT control registers. Any write access that does not provide the correct values for the password and guard bits is regarded as malfunction and results in an alarm
- › On top of the general WDTs, a Safety Watchdog Timer is provided. It is independent from the CPU watchdogs and it also provides temporal protection against unintended writes to critical system registers which could impact the safety-critical systems
- › These feature ensures that the system runs in a robust and safe manner (e.g. Trigger an alarm, a reset or stopping the CPU in case of malfunction)

# SCU – Emergency Stop Output Control

- › The emergency stop feature provides a fast reaction to an emergency event without the intervention of the software. As reaction to the emergency event, selected output ports can be immediately placed into a defined state (e.g. bring the actuators in a known state)
- › An emergency stop can be triggered by the following:
  - A transition on the port which is configured as the Emergency Stop input
  - An alarm event or command from the Safety Management Unit that is configured to generate a port emergency stop
- › The emergency stop control logic for the ports operates in two modes:
  - Synchronous mode (default): the emergency case is activated by hardware and released by software
  - Asynchronous mode: both the activation and releasing of the emergency case are done by hardware



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