AURIX™
System Architecture

AURIX™ TC2xx Microcontroller Training
V1.0 2019-03

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AURIX™
System Architecture

**Key Features**
- Embedded flash platform for real time applications
- Up to 3 TriCore™ with DSP instructions
- Rich peripheral set and large RAMs

**Highlights**
- Multicore Microcontroller with embedded Flash
- TriCore™ (DSP processor) @300 MHz
- Up to 8 MB Flash, more than 2 MB RAM
- DMA, HW-FFT, ADC, Ethernet MAC,...

**Customer Benefits**
- Embedded flash allows compact design and fast code execution
- Enables heavy processing tasks like radar or signal processing applications
- Reduces the need for external components for cost competitive BOMs

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Embedded flash platform for real time applications

› All the flash memory is divided in banks (PF0-3 & DF0-1), which are concurrently readable.
› Each bank has its own Shared Resource Interconnect (SRI) ports, Error Correction Code (ECC) decoders and pre-fetch logic.
› In case of ECC errors, the Safety Management Unit (SMU) and the Interrupt Router (IR) can be configured to generate errors, respectively interrupts.
› This embedded flash platform offers a high performance code storage and flexible memory selection, controlled by safety mechanisms.

Note: This is the Flash memory structure of AURIX™ TC29x. For all the other devices, consult the User Manual.
The TriCore™ architecture combines three powerful concepts:
- Microcontroller
- RISC processor
- DSP (Digital Signal Processor)

**TC 1.6Efficiency (TC 1.6E):**
- High efficiency / low power architecture
  - Scalar Harvard
  - 4 pipeline stages for up to 200 MHz
- Identical instruction set as TC1.6P
- 1.4 DMIPS/MHz
- Instruction cache

**TC 1.6Performance (TC 1.6P):**
- High performance architecture
  - Superscalar Harvard
  - 6 pipeline stages for up to 300 MHz
- Identical instruction set as TC1.6E
- 1.6 DMIPS/MHz
- Instruction and data cache

**32bit Floating Point Unit in all CPUs:**
- Single precision according to IEEE-754
- 2 FLOPs per cycle (pipelined)
Rich peripheral set and large RAMs

**Peripherals:**
- ADC: Analog-Digital Convertor – 12-bit up to 1 MSPS
- GTM, GPT12 and CCU6: Signal Capture / Compare and PWM generation
- FFT engine: Fourier Transform acceleration
- STM: Timer Module
- DMA: Direct Memory Access Module
- Advanced On – Chip Debug System (OCDS)

**Communication Interfaces:**
- QSPI: Advanced SPI interface (Serial Peripheral Interface)
- CAN: Controller Area Network
- Ethernet MAC: Ethernet 100 Mbit/s interface
- I2C: Inter-Integrated Circuit Bus
- EBU: External Bus Unit (32-bit Data, 24-bit Address)

**On-Chip Memories:**
- More than 2 MB integrated RAM including CPUs tightly coupled Scratch-Pad RAM
- Up to 8 MB integrated Flash memory with EEPROM Emulation
AURIX™ Multi-CPU architecture contains:

- Distributed Scratch-Pad RAMs for data (DSPR) and program (PSPR)
  - Can be accessed by all CPUs
- CPUs execute code from cached PFlash modules
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System integration

› AURIX™ TC2xx combines three powerful technologies within one silicon die, improving power consumption, speed and reducing the costs for embedded applications:
  - Reduced Instruction Set Computing (RISC) processor architecture
  - Digital Signal Processing (DSP) operations and addressing modes
  - On-chip memories and peripherals

› AURIX™ TC2xx devices are designed to meet the needs of embedded control systems applications, where real-time responsiveness, computational power and data bandwidth are key design elements

AURIX TC29x Block diagram
## Overview

Car systems like airbag and engine management need to operate in a safe and secure way:

- **Safe**: Airbag must not trigger under regular driving conditions
- **Secure**: Unauthorized persons must not be able to hack the car’s systems

## Advantages

Beside AURIX™ TC2xx versatile set of on-chip peripherals connected to TriCore™ CPUs, the AURIX™ family also offers safety and security modules to deal with critical embedded applications.
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