SPI_DMA_1
for KIT_AURIX_TC397_TFT
SPI data communication via DMA

AURIX™ TC3xx Microcontroller Training
V1.0.0

Scope of work

QSPI is used to conduct SPI Master Slave communication using the DMA module.

This example implements an SPI full duplex communication.
QSPI2 is configured as an SPI master and QSPI3 is configured as an SPI slave. Both master and slave exchange eight bytes of data.
Four DMA channels are used to enable data transfer between RAM and QSPI FIFOs without CPU intervention:

- DMA channel 1 is configured as SPI master Tx
- DMA channel 2 is configured as SPI master Rx
- DMA channel 3 is configured as SPI slave Tx
- DMA channel 4 is configured as SPI slave Rx

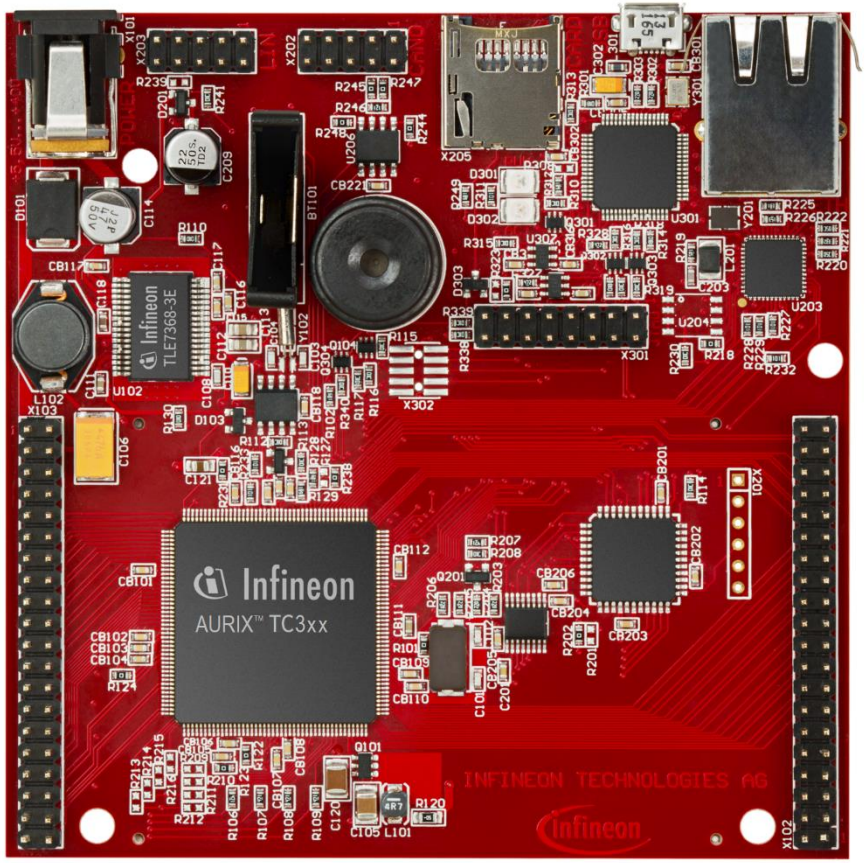
An LED is used to signal the successful data communication.

Introduction

- The **Q**ueued **S**ynchronous **P**eripheral **I**nterface (QSPI) enables any synchronous serial communication with external devices based on the standardized SPI-bus signals: clock, data-in, data-out and slave select.
- The QSPI works in full duplex mode either as Master or Slave with up to 50 Mbit/s.
- The DMA module channels can be configured to transfer data from/to QSPI FIFOs to/from internal RAM Memory without any CPU intervention.
- This example is based on the Infineon Low Level Drivers to demonstrate SPI Master Slave Communication with minimum CPU intervention.

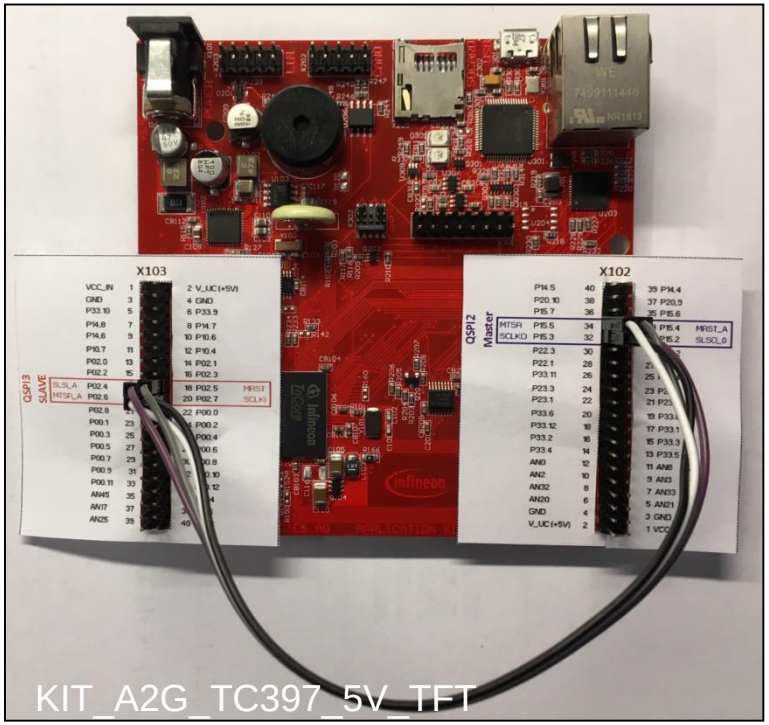
Hardware setup

This code example has been developed for the board KIT_A2G_TC397_5V_TFT.



Hardware Setup

X103			
VCC_IN	1	2	V_UC
GND	3	4	GND
P21.2	5	6	P21.3
P14.8	7	8	P14.7
P14.6	9	10	P20.0
P21.4	11	12	P21.5
P02.0	13	14	P02.1
P02.2	15	16	P02.3
P02.4	17	18	P02.5
P02.6	19	20	P02.7
P02.8	21	22	P00.0
P00.1	23	24	P00.2
P00.3	25	26	P00.4
P00.5	27	28	P00.6
P00.7	29	30	P00.8
P00.9	31	32	P00.10
P00.11	33	34	P00.12
AN19	35	36	AN18
AN17	37	38	AN16
AN25	39	40	AN24



X102			
P14.5	40	39	P14.4
P33.10	38	37	P20.9
P15.7	36	35	P15.6
P15.5	34	33	P15.4
P15.3	32	31	P15.2
P22.3	30	29	P22.2
P22.1	28	27	P22.0
P33.11	26	25	P23.4
P23.3	24	23	P23.2
P23.1	22	21	P23.0
P33.6	20	19	P33.8
P33.12	18	17	P33.1
P33.2	16	15	P33.3
P33.4	14	13	P33.5
AN0	12	11	AN8
AN2	10	9	AN3
AN11	8	7	AN13
AN20	6	5	AN21
GND	4	3	GND
V_UC	2	1	VCC_IN

› Use the stencils as illustrated.

› Connect following pins as described and illustrated using wires.

X103 : QSPI3 (Slave)	WIRE	X102 : QSPI2 (Master)
P02.7 : 20 : SCLKI	←→	P15.3 : 32 : SCLKO
P02.4 : 17 : SLSI_A	←→	P15.2 : 31 : SLSO_0
P02.5 : 18 : MRST	←→	P15.4 : 33 : MRST_A
P02.6 : 19 : MTSR_A	←→	P15.5 : 34 : MTSR

Implementation

Configuring the SPI communication

The configuration of the SPI communication is done through the function ***initQSPI()*** in two different steps:

- QSPI Slave initialization
- QSPI Master initialization

QSPI Slave initialization

- The initialization of the QSPI slave module is done by defining an instance of the ***IfxQspi_SpiSlave_Config*** structure
- The structure is filled with default values by the function ***IfxQspi_SpiSlave_initModuleConfig()***
- Afterwards, the following parameters are modified to enable the DMA usage, set its channels, interrupt priorities and IO port pins:
  - DMA configuration: ***dma.useDma***, ***dma.txDmaChannelId***, ***dma.rxDmaChannelId***
  - Interrupts configuration: ***base.txPriority***, ***base.rxPriority***, ***base.erPriority***, ***base.isrProvider***
  - Pins configuration: ***pins***

Implementation

QSPI Slave initialization (Cont.)

- The function ***IfxQspi_SpiSlave_initModule()*** is used to initialize the QSPI slave module
- Finally, the buffers used by the QSPI slave are initialized

The functions needed to initialize the QSPI Slave can be found in the iLLD header ***IfxQspi_SpiSlave.h***.

QSPI Master initialization

- The initialization of the QSPI master module is done by defining an instance of the ***IfxQspi_SpiMaster_Config*** structure
- The structure is filled with default values by the function ***IfxQspi_SpiMaster_initModuleConfig()***
- Afterwards, the following parameters are modified to enable the DMA usage, set its channels, interrupt priorities and IO port pins:
  - DMA configuration: ***dma.useDma***, ***dma.txDmaChannelId***, ***dma.rxDmaChannelId***
  - Interrupts configuration: ***base.txPriority***, ***base.rxPriority***, ***base.erPriority***, ***base.isrProvider***
  - Pins configuration: ***pins***

Implementation

QSPI Master initialization (Cont.)

- The function ***IfxQspi_SpiMaster_initModule()*** is used to initialize the QSPI master module
- A QSPI module controls 16 communication channels, which are individually programmable. In this example, the function ***initQSPI2MasterChannel()*** initializes the channel zero using an instance of the structure ***IfxQspi_SpiMaster_ChannelConfig***. Afterwards, the slave select channel number is set through the parameter ***sls.output*** and the baud rate is modified via the parameter ***base.baudrate***
- The function ***IfxQspi_SpiMaster_initChannel()*** is used to initialize the QSPI master channel
- Finally, the buffers used by the QSPI master are initialized

The functions needed to initialize the QSPI Master can be found in the iLLD header ***IfxQspi_SpiMaster.h***.

Implementation

Interrupt Service Routines (ISR):

- The following ISRs are implemented to ensure a proper SPI communication in DMA mode:
  - SPI Master error interrupt ***QSPI2ErrorISR()*** ISR calls the function:
    - ***IfxQspi_SpiMaster_isrError()***
  - SPI Slave error interrupt ***QSPI3ErrorISR()*** ISR calls the function:
    - ***IfxQspi_SpiSlave_isrError()***
  - SPI Master transmit interrupt ***DMAChn1ISR()*** ISR calls the function:
    - ***IfxQspi_SpiMaster_isrDmaTransmit()***
  - SPI Master receive interrupt ***DMAChn2ISR()*** ISR calls the function:
    - ***IfxQspi_SpiMaster_isrDmaReceive()***
  - SPI Slave transmit interrupt ***DMAChn3ISR()*** ISR calls the function:
    - ***IfxQspi_SpiSlave_isrDmaTransmit()***
  - SPI Slave receive interrupt ***DMAChn4ISR()*** ISR calls the function:
    - ***IfxQspi_SpiSlave_isrDmaReceive()***

- The functions listed above can be found in the iLLD headers ***IfxQspi_SpiMaster.h*** and ***IfxQspi_SpiSlave.h***

Implementation

SPI Master - Slave Communication:

The SPI Master Slave communication is established through the following steps:

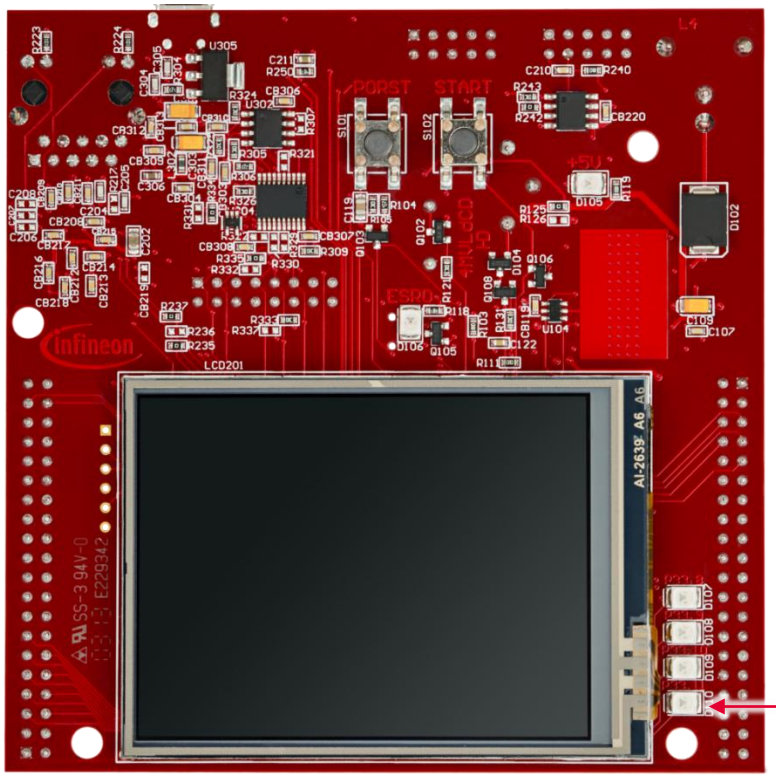
- Enable SPI Slave for data communication using the function: ***IfxQspi_SpiSlave_exchange()***
- Enable and Start SPI Master data communication using the function: ***IfxQspi_SpiMaster_exchange()***
- Poll for SPI slave data reception using the function: ***IfxQspi_SpiSlave_getStatus()***
- The received and transmitted data are compared byte by byte and the number of errors are counted

Run and Test

After code compilation and flashing the device, perform the following steps:

- Run the project and check if the LED D110 is on.
  - Data transmitted without errors

- Additionally, using the debugger, the behavior can be checked:
  - Add ***g_qspiDma*** to Watch window
  - Check if ***g_qspiDma.qspiBuffer.spiSlaveRxBuffer*** and ***g_qspiDma.qspiBuffer.spiMasterRxBuffer*** are the same as ***g_qspiDma.qspiBuffer.spiMasterTxBuffer*** and, respectively, ***g_qspiDma.qspiBuffer.spiSlaveTxBuffer***



References

- AURIX™ Development Studio is available online:
- https://www.infineon.com/aurixdevelopmentstudio
- Use the *„Import...“* function to get access to more code examples.

- More code examples can be found on the GIT repository:
- https://github.com/Infineon/AURIX_code_examples

- For additional trainings, visit our webpage:
- https://www.infineon.com/aurix-expert-training

- For questions and support, use the AURIX™ Forum:
- https://www.infineonforums.com/forums/13-Aurix-Forum

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