SPI_DMA_1
for KIT_AURIX_TC297_TFT
SPI data communication via DMA
Scope of work

QSPI is used to conduct SPI Master Slave communication using the DMA module.

This example implements an SPI full duplex communication. QSPI2 is configured as an SPI master and QSPI3 is configured as an SPI slave. Both master and slave exchange eight bytes of data. Four DMA channels are used to enable data transfer between RAM and QSPI FIFOs without CPU intervention:

- DMA channel 1 is configured as SPI master Tx
- DMA channel 2 is configured as SPI master Rx
- DMA channel 3 is configured as SPI slave Tx
- DMA channel 4 is configured as SPI slave Rx

An LED is used to signal the successful data communication.
Introduction

- The **Queued Synchronous Peripheral Interface (QSPI)** enables any synchronous serial communication with external devices based on the standardized SPI-bus signals: clock, data-in, data-out and slave select.

- The QSPI works in full duplex mode either as Master or Slave with up to 50 Mbit/s.

- The DMA module channels can be configured to transfer data from/to QSPI FIFOs to/from internal RAM Memory without any CPU intervention.

- This example is based on the Infineon Low Level Drivers to demonstrate SPI Master Slave Communication with minimum CPU intervention.
Hardware setup

This code example has been developed for the board KIT_AURIX_TC297_TFT_BC-Step.
Hardware Setup

› Use the stencils as illustrated.

› Connect following pins as described and illustrated using wires.

<table>
<thead>
<tr>
<th>X103 : QSPI3 (Slave)</th>
<th>WIRE</th>
<th>X102 : QSPI2 (Master)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P02.7 : 20 : SCLKI</td>
<td></td>
<td>P15.3 : 32 : SCLKO</td>
</tr>
<tr>
<td>P02.4 : 17 : SLSI_A</td>
<td></td>
<td>P15.2 : 31 : SLSO_0</td>
</tr>
<tr>
<td>P02.5 : 18 : MRST</td>
<td></td>
<td>P15.4 : 33 : MRST_A</td>
</tr>
<tr>
<td>P02.6 : 19 : MTSR_A</td>
<td></td>
<td>P15.5 : 34 : MTSR</td>
</tr>
</tbody>
</table>
Implementation

Configuring the SPI communication

The configuration of the SPI communication is done through the function `initQSPI()` in two different steps:

› QSPI Slave initialization
› QSPI Master initialization

QSPI Slave initialization

› The initialization of the QSPI slave module is done by defining an instance of the `IfxQspi_SpiSlave_Config` structure
› The structure is filled with default values by the function `IfxQspi_SpiSlave_initModuleConfig()`
› Afterwards, the following parameters are modified to enable the DMA usage, set its channels, interrupt priorities and IO port pins:
  - DMA configuration: `dma.useDma`, `dma.txDmaChannelId`, `dma.rxDmaChannelId`
  - Interrupts configuration: `base.txPriority`, `base.rxPriority`, `base.errPriority`, `base_isrProvider`
  - Pins configuration: `pins`
Implementation

QSPI Slave initialization (Cont.)

› The function `IfxQspi_SpiSlave_initModule()` is used to initialize the QSPI slave module
› Finally, the buffers used by the QSPI slave are initialized

The functions needed to initialize the QSPI Slave can be found in the iLLD header `IfxQspi_SpiSlave.h`.

QSPI Master initialization

› The initialization of the QSPI master module is done by defining an instance of the `IfxQspi_SpiMaster_Config` structure
› The structure is filled with default values by the function `IfxQspi_SpiMaster_initModuleConfig()`
› Afterwards, the following parameters are modified to enable the DMA usage, set its channels, interrupt priorities and IO port pins:
  – DMA configuration: `dma.useDma`, `dma.txDmaChannelId`, `dma.rxDmaChannelId`
  – Interrupts configuration: `base.txPriority`, `base.rxPriority`, `base.erPriority`, `base.isrProvider`
  – Pins configuration: `pins`
Implementation

QSPI Master initialization (Cont.)

› The function `IfxQspi_SpiMaster_initModule()` is used to initialize the QSPI master module
› A QSPI module controls 16 communication channels, which are individually programmable. In this example, the function `initQSPI2MasterChannel()` initializes the channel zero using an instance of the structure `IfxQspi_SpiMaster_ChannelConfig`. Afterwards, the slave select channel number is set through the parameter `sls.output` and the baud rate is modified via the parameter `base.baudrate`
› The function `IfxQspi_SpiMaster_initChannel()` is used to initialize the QSPI master channel
› Finally, the buffers used by the QSPI master are initialized

The functions needed to initialize the QSPI Master can be found in the iLLD header `IfxQspi_SpiMaster.h`. 
Implementation

Interrupt Service Routines (ISR):

› The following ISRs are implemented to ensure a proper SPI communication in DMA mode:
  – SPI Master error interrupt `QSPI2ErrorISR()` ISR calls the function:
    – `IfxQspi_SpiMaster_isrError()`
  – SPI Slave error interrupt `QSPI3ErrorISR()` ISR calls the function:
    – `IfxQspi_SpiSlave_isrError()`
  – SPI Master transmit interrupt `DMACHn1ISR()` ISR calls the function:
    – `IfxQspi_SpiMaster_isrDmaTransmit()`
  – SPI Master receive interrupt `DMACHn2ISR()` ISR calls the function:
    – `IfxQspi_SpiMaster_isrDmaReceive()`
  – SPI Slave transmit interrupt `DMACHn3ISR()` ISR calls the function:
    – `IfxQspi_SpiSlave_isrDmaTransmit()`
  – SPI Slave receive interrupt `DMACHn4ISR()` ISR calls the function:
    – `IfxQspi_SpiSlave_isrDmaReceive()`

› The functions listed above can be found in the iLLD headers `IfxQspi_SpiMaster.h` and `IfxQspi_SpiSlave.h`
Implementation

SPI Master Slave Communication:

The SPI Master Slave communication is established through the following steps:

› Enable SPI Slave for data communication using the function: 
  `ifxQspi_SpiSlave_exchange()`

› Enable and Start SPI Master data communication using the function: 
  `ifxQspi_SpiMaster_exchange()`

› Poll for SPI slave data reception using the function: 
  `ifxQspi_SpiSlave_getStatus()`

› The received and transmitted data are compared byte by byte and the number of errors are counted
Run and Test

After code compilation and flashing the device, perform the following steps:

› Run the project and check if the LED D110 is on.
  - Data transmitted without errors

› Additionally, using the debugger, the behavior can be checked:
  - Add `g_qspiDma` to Watch window
  - Check if
    `g_qspiDma.qspiBuffer.spiSlaveRxBuffer` and
    `g_qspiDma.qspiBuffer.spiMasterRxBuffer`
    are the same as
    `g_qspiDma.qspiBuffer.spiMasterTxBuffer` and, respectively,
    `g_qspiDma.qspiBuffer.spiSlaveTxBuffer`
References

› **AURIX™ Development Studio** is available online:
  › [https://www.infineon.com/aurixdevelopmentstudio](https://www.infineon.com/aurixdevelopmentstudio)
  › Use the „Import...“ function to get access to more code examples.

› More code examples can be found on the GIT repository:
  › [https://github.com/Infineon/AURIX_code_examples](https://github.com/Infineon/AURIX_code_examples)

› For additional trainings, visit our webpage:
  › [https://www.infineon.com/aurix-expert-training](https://www.infineon.com/aurix-expert-training)

› For questions and support, use the AURIX™ Forum:
<table>
<thead>
<tr>
<th>Revision</th>
<th>Description of change</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.0.1</td>
<td>Update of version to be in line with the code example’s version</td>
</tr>
<tr>
<td>V1.0.0</td>
<td>Initial version</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.