MSC Micro Second Channel

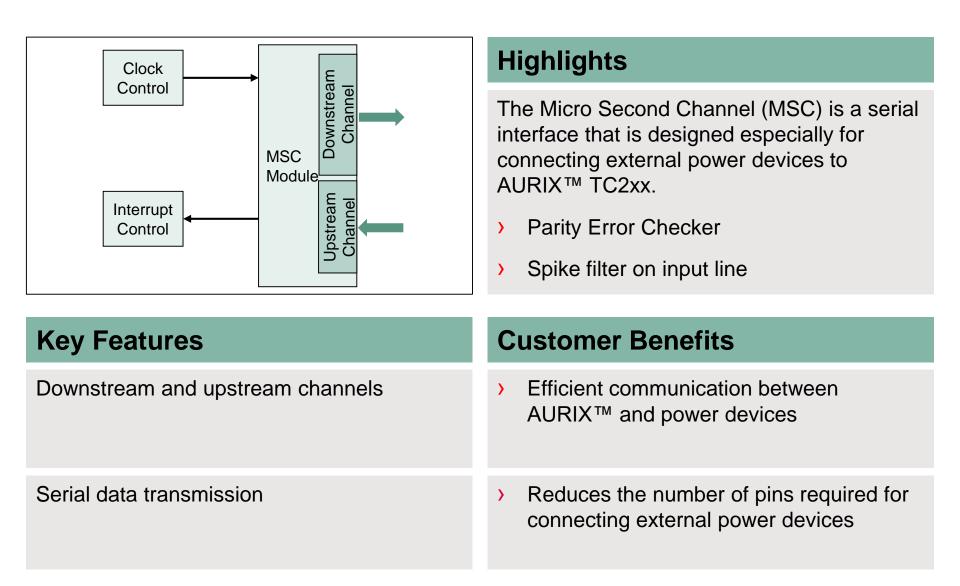
AURIX[™] TC2xx Microcontroller Training V1.0 2019-03



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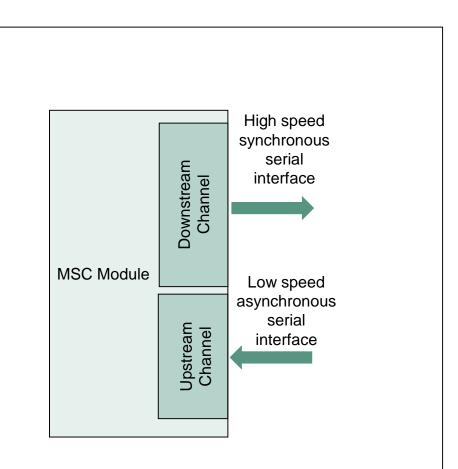




MSC Downstream and upstream channels



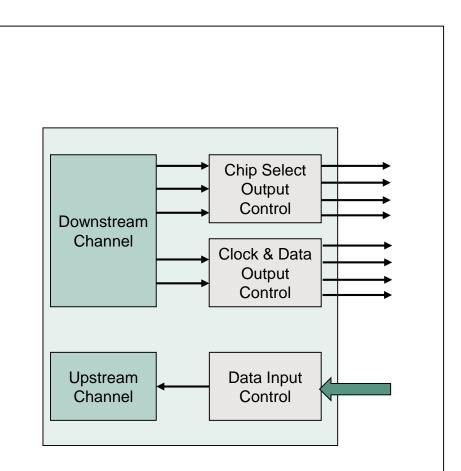
- The data is sent to the power device via the downstream channel (high speed synchronous serial data stream) and the status information is received on AURIX[™] side via the upstream channel (low speed asynchronous serial data stream)
- > Downstream channel:
 - Serial output clock frequency up to 100 MHz
 - Fractional clock divider for precise frequency control
 - Start of serial frame: software-controlled, timer-controlled or free-running
- > Upstream channel:
 - Programmable upstream data frame length (16 or 12 bits)
 - Parity error checker
 - Built-in spike filter on SDI lines



MSC Serial data transmission

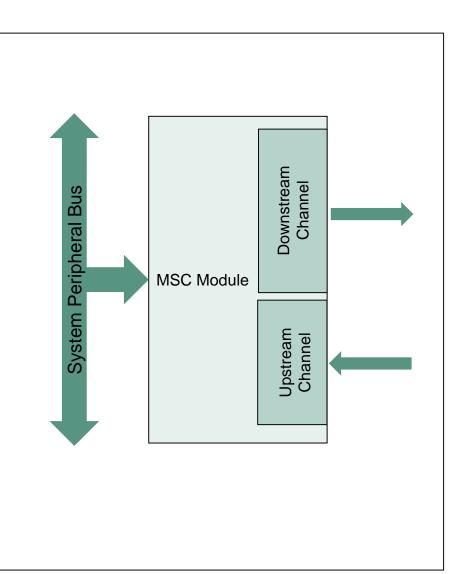


- Serial data transmission:
 - Low-speed asynchronous reception
 - High-speed synchronous transmission
- Serial data transmission reduces the number of pins required for communication with external devices
- > The pin types of the downstream channel interface are selectable:
 - Four LVDS differential output drivers
 - Four digital GPIO pins
- The downstream channel generates five output signals that control eight MSC module output (4 chip select outputs, 2 clock outputs, 2 serial data outputs)
- The upstream channel has one input signal



MSC System integration

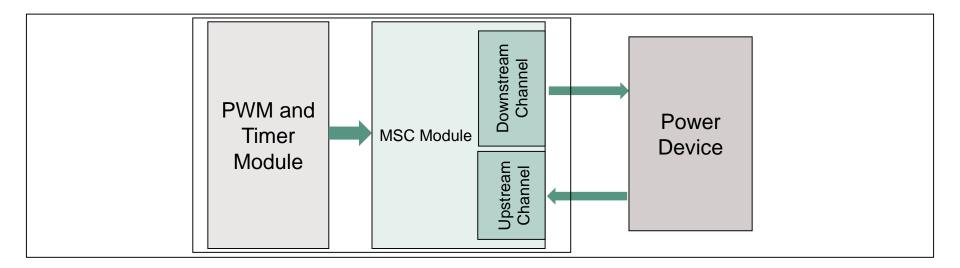
- As in the case of most of the AURIX modules, MSC is connected on the System Peripheral Bus (SPB)
- Parallel requests from on chip bus masters to MSC module are executed sequentially via the on chip bus system
- Read-modify-write feature provides an atomic read/write sequence, which ensures that no other master can access the module in between





Application example Control of an external power switching unit





Overview

 The MSC module supports two MSC slaves. Each interface can send command and data frames to the power device

Advantages

 Downstream channel can be used to send information to the power device.
Data frames can be sent out in repetition mode with one passive frame in between, reducing the number of pins and the CPU overhead

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