MEMMAP

Memory Maps

AURIX™ Microcontroller Training
V1.0 2019-03

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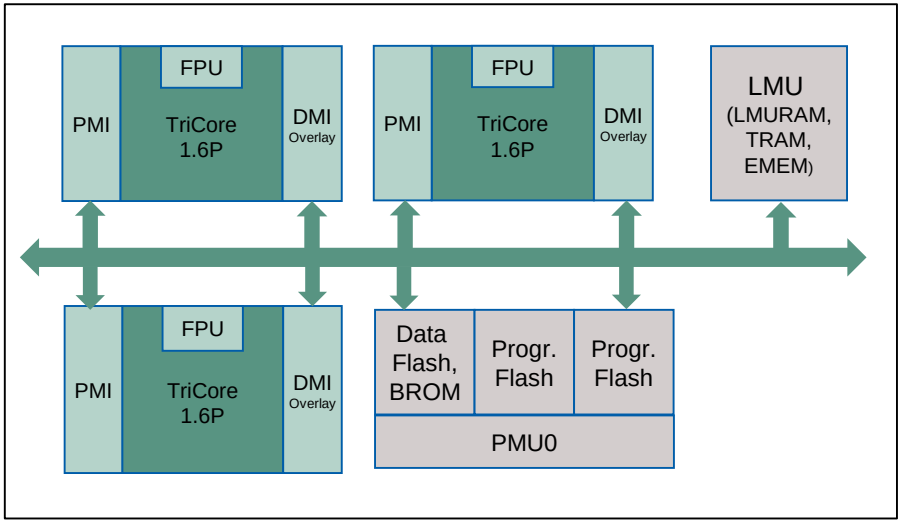

Highlights

- Multicore Microcontroller with embedded Flash
- Scratch-Pad RAM (PSPR and DSPR) closely coupled to TriCore™
- Flash memories accessible via PMU
- Up to 8 MB Flash, up to 2 MB RAM
- Contiguous Memory maps

Key Features

Compatible address maps across family

Versatile addressing modes

Customer Benefits

- Memory hierarchy allows optimal code performance & application portability
- Easy handling of cacheable and peripheral address space

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Compatible address maps across family

- AURIX™ TC2xx has the following memories:
  - Program and Data Flash Memory (PFlash/DFlash): Flash memory is used for information that does not change in time (e.g. the program running on the microcontroller)
  - User Configuration Blocks (UCB): This is an area in DFlash, where protection data is stored (e.g. unique chip identifier, trimming data, etc.)
  - BootROM (BROM): It is a part of the PMU and it is a read-only memory. A fixed piece of code is placed in the BootROM. The microcontroller start-up code is executed out of the BootROM and its content is not user readable (security feature)
  - Program & Data Scratch-Pad RAM (PSPR/DSPR): Allows the CPU to access code/data faster compared to the other RAMs and Flashes
  - Program & Data Cache (PCACHE/DCACHE): Cache memory is high-speed RAM. This area of the memory is used for repeatable reads and writes, where fast access to the data/code is needed
  - LMU: SRI peripheral providing access to volatile memory resources
    - LMURAM: Local memory for general purpose usage
    - TRAM: Trace RAM used for tracing
    - EMEM: Emulation and debug memory (available only in the Emulation Devices)

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Compatible address maps across family

- TriCore™ 4 GB addressable memory map is organized into segments of 256 MB
- A Segment is identified by the A[31:28] bits of the system address
- Each segment allows access to a specific area and it is used to define cacheable and non-cacheable areas
- This structure ensures the portability of applications across the devices of the family (considering that all needed modules are included in the device)
- A good understanding of the memory structure enables the user to optimize the code in order to achieve optimal run-time performance

Segment	Memory
Segments 0-7	Multiprocessor space (e.g. CPUs Scratch-Pad RAM)
Segment 8	Cached PFlash, BROM and EBU (if available)
Segment 9	Cached LMURAM (if available) and EMEM (if available)
Segment 10	Non-cached PFlash, DFlash, BROM and EBU (if available)
Segment 11	Non-cached LMURAM (if available) and EMEM (if available)
Segment 12-13	Reserved
Segment 14	Peripheral Space
Segment 15	Peripheral Space

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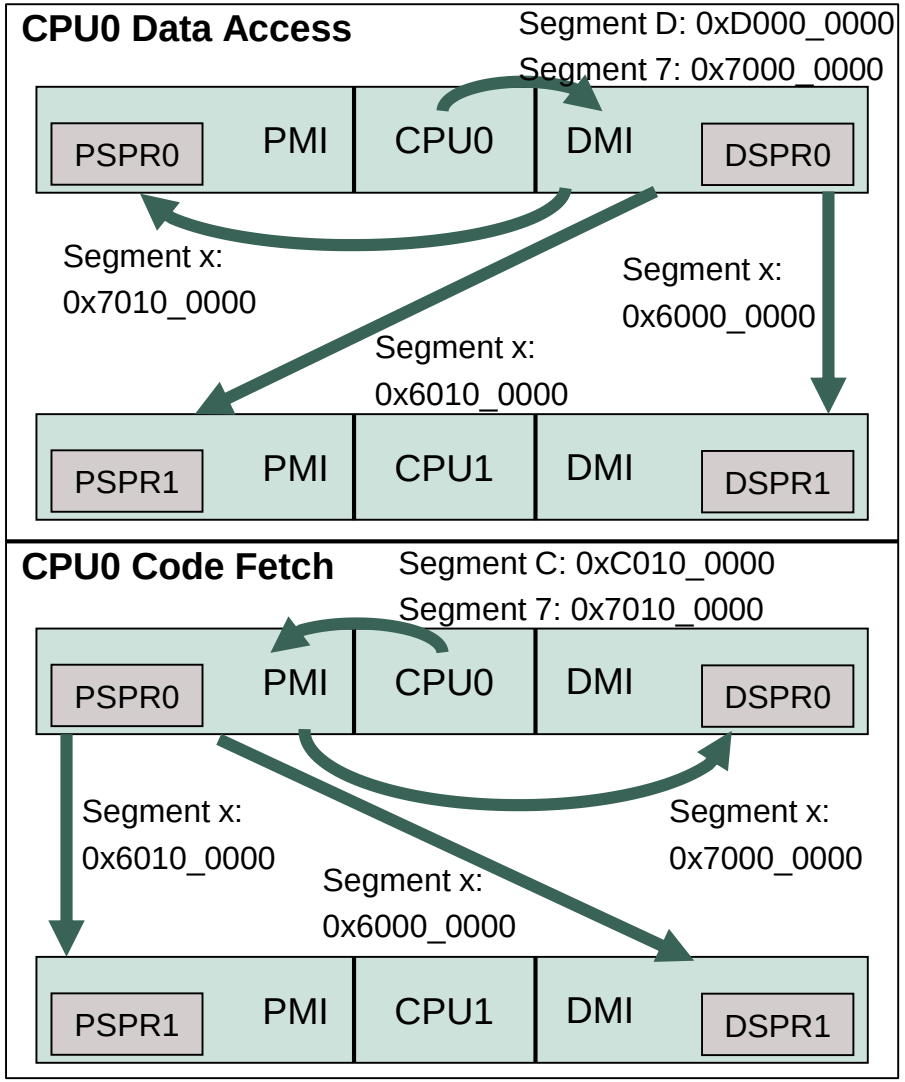
Versatile addressing modes

- Each CPU has access to
  - its own memory or other CPUs' memories via its global segment (0-7)
  - its own DSPR at offset 0 via the local address (0xD000_0000)
  - its own PSPR at offset 0x0010_0000 (1MB) via the local address (0xC000_0000)
- This provides
  - the best usage of TriCore™ addressing modes for optimum code-density (single instruction access)
  - unique address for CPU Scratch-Pad RAMs in the system



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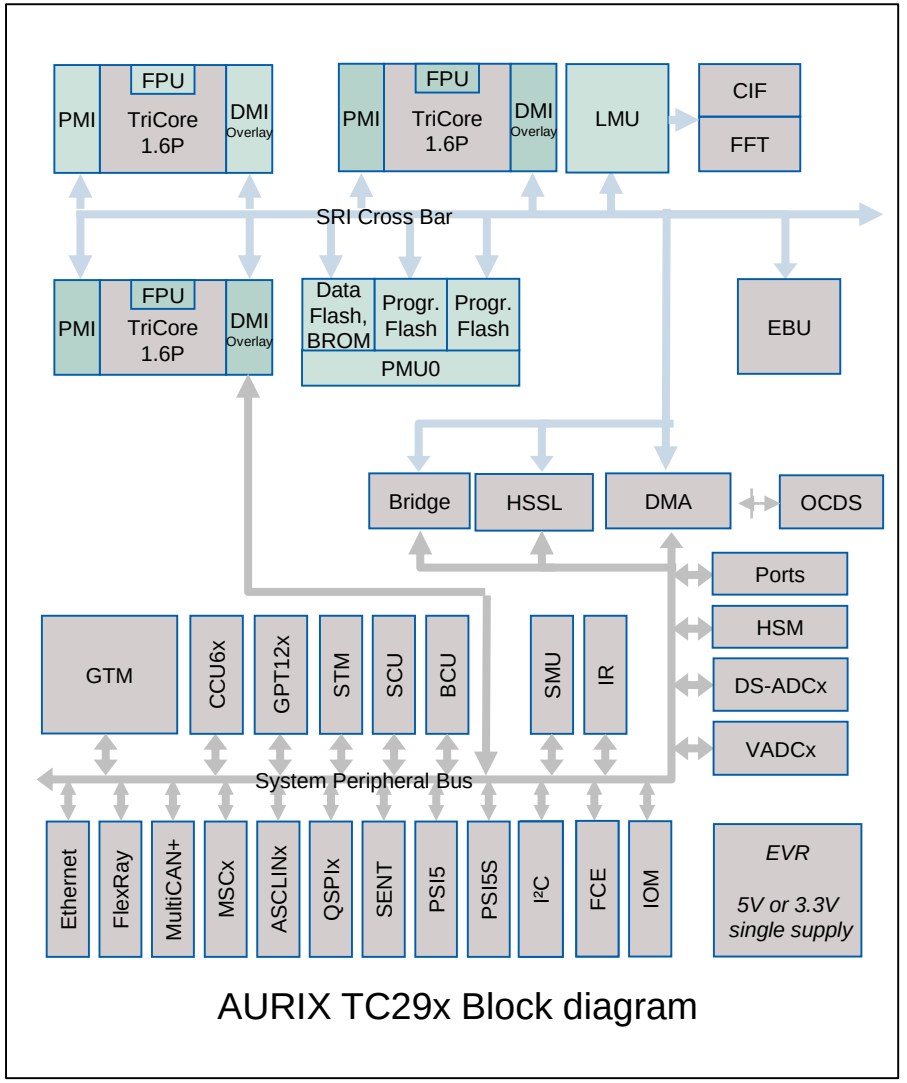
System integration

- Each segment of the memory is either peripheral space or cached/non-cached memory
- In the TriCore™ Architecture, different segments have different access characteristics
- Access to a segment outside the implemented memory size will result in a trap



AURIX TC29x Block diagram

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