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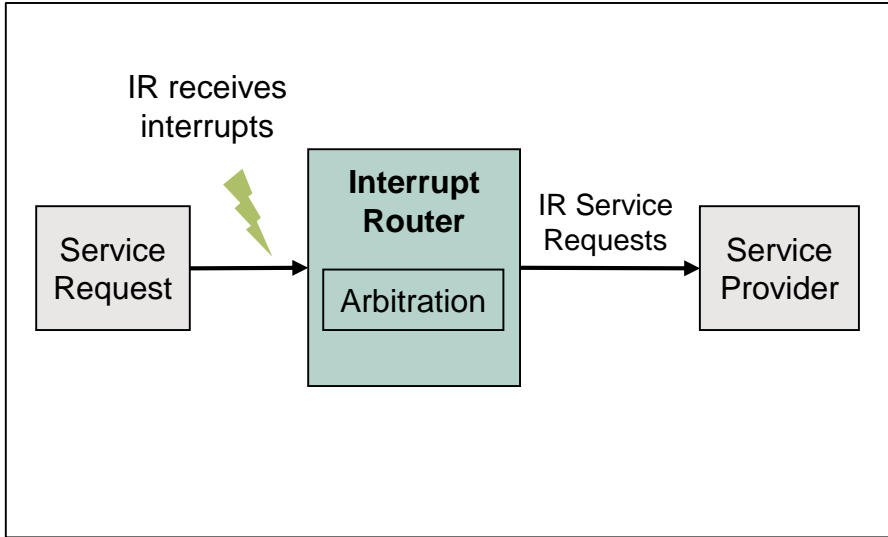
Interrupt Router

AURIX™ Microcontroller Training
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Interrupt Router



Highlights

- > Schedules the Service Requests (SRs) from external resources, internal resources and Software to the CPU and the DMA module (Service Providers).
- > SR cleared automatically on HW acknowledge by Interrupt Service Providers (ISP)
- > Software Interrupts: 8 SW Service Requests per CPU
- > Low latency arbitration around 50 ns

Key Features

Mapping Service Requests to Service Providers

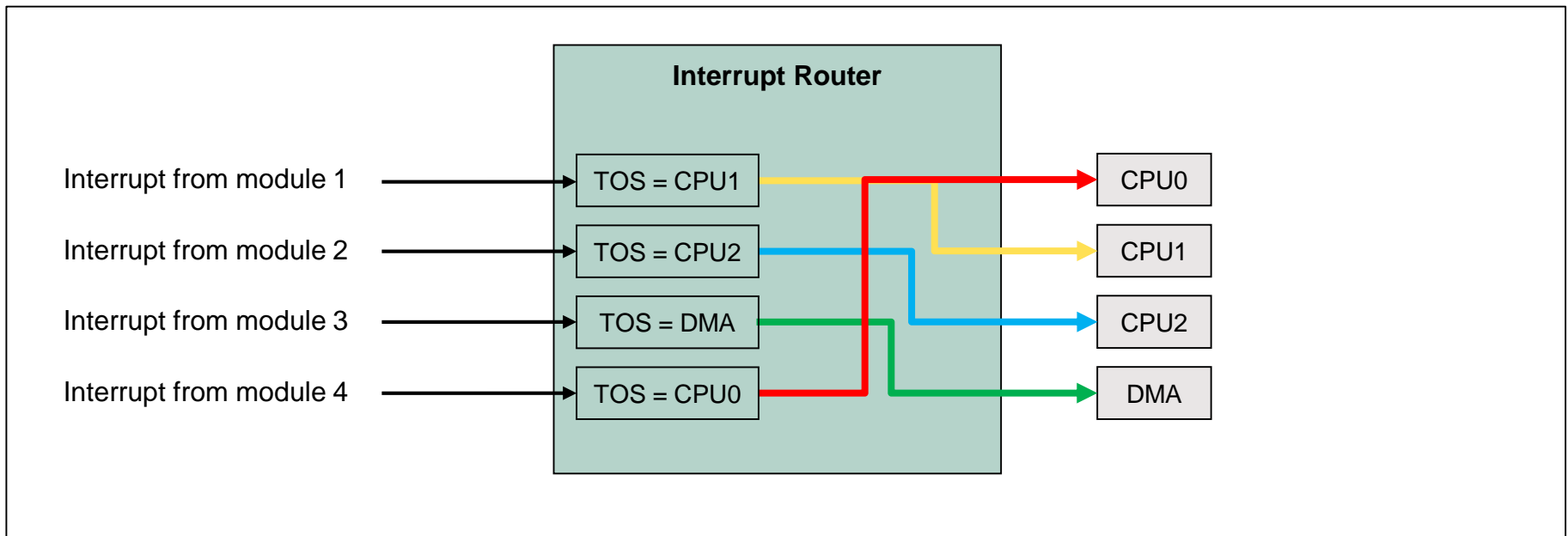
Assign a priority for each Service Request

Customer Benefits

- > Each interrupt could be configured to triggered one Service Provider (CPUx, DMA)
- > Arbitration for pending Service Requests mapped to the same ISP

Mapping service requests to service providers

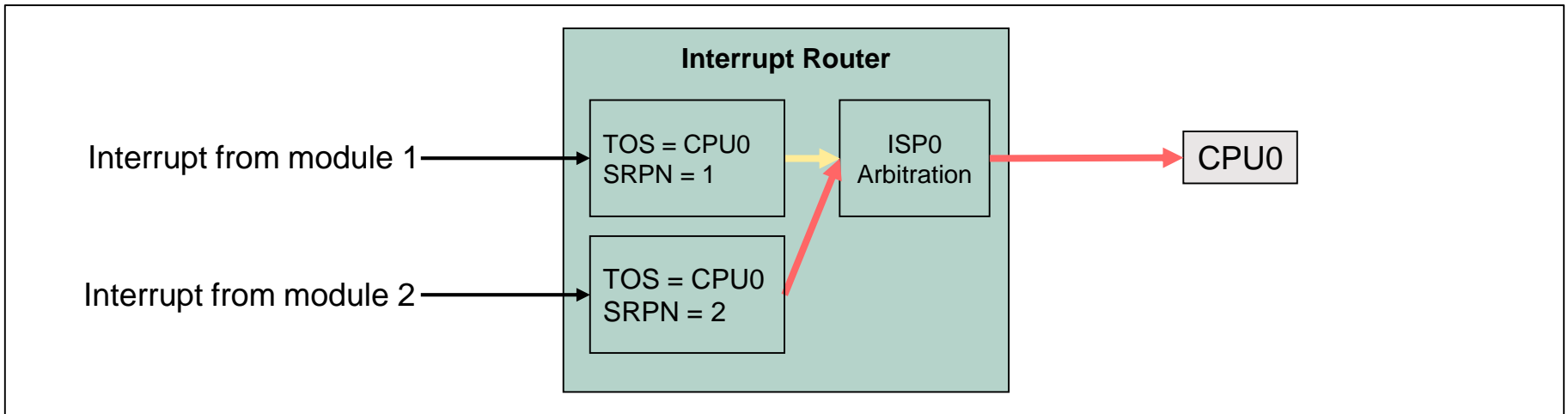
- › Each service request must be configured to be serviced by one of the service provider:
 - Type of Service (TOS)
 - CPU_x (x=0..2): The service request is executed by the selected CPU
 - DMA: The service request triggers a DMA channel transfer



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Assign a priority for each service request

- › A Service Request Priority Number (**SRPN**) from 0 to 255 must be assigned to each service request :
 - Depending on the selected Service Provider (TOS) the SRPN presents the following:
 - **CPUx**: The interrupt priority of the related Service request (SRPN 0 is neutral)
 - **DMA**: The number of the DMA channel to be triggered.

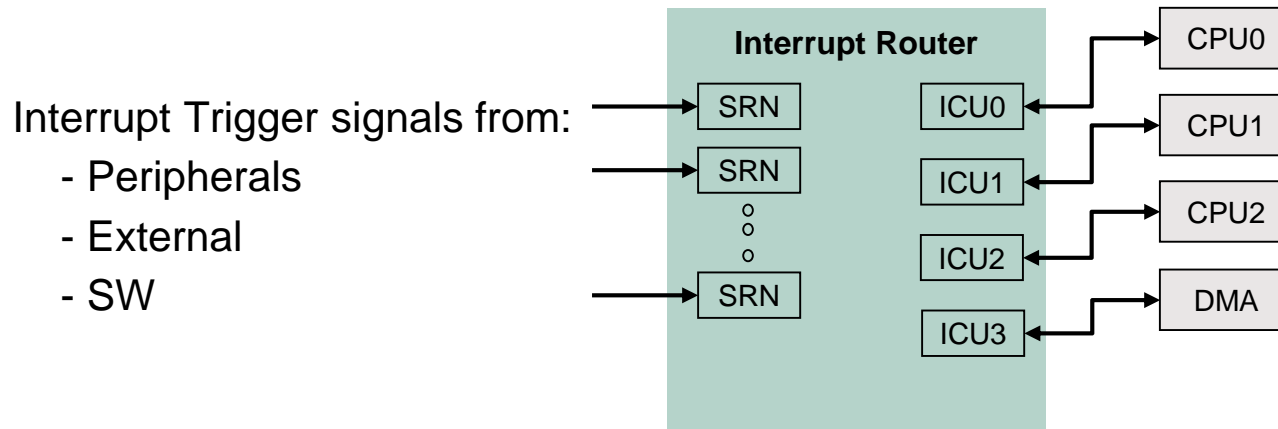


- › **Arbitration**: For each ISP_x, IR arbitrates among the group of pending Service Requests mapped to this ISP_x. Winner of an arbitration round is the pending SR with the highest priority (SRPN number).

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System integration

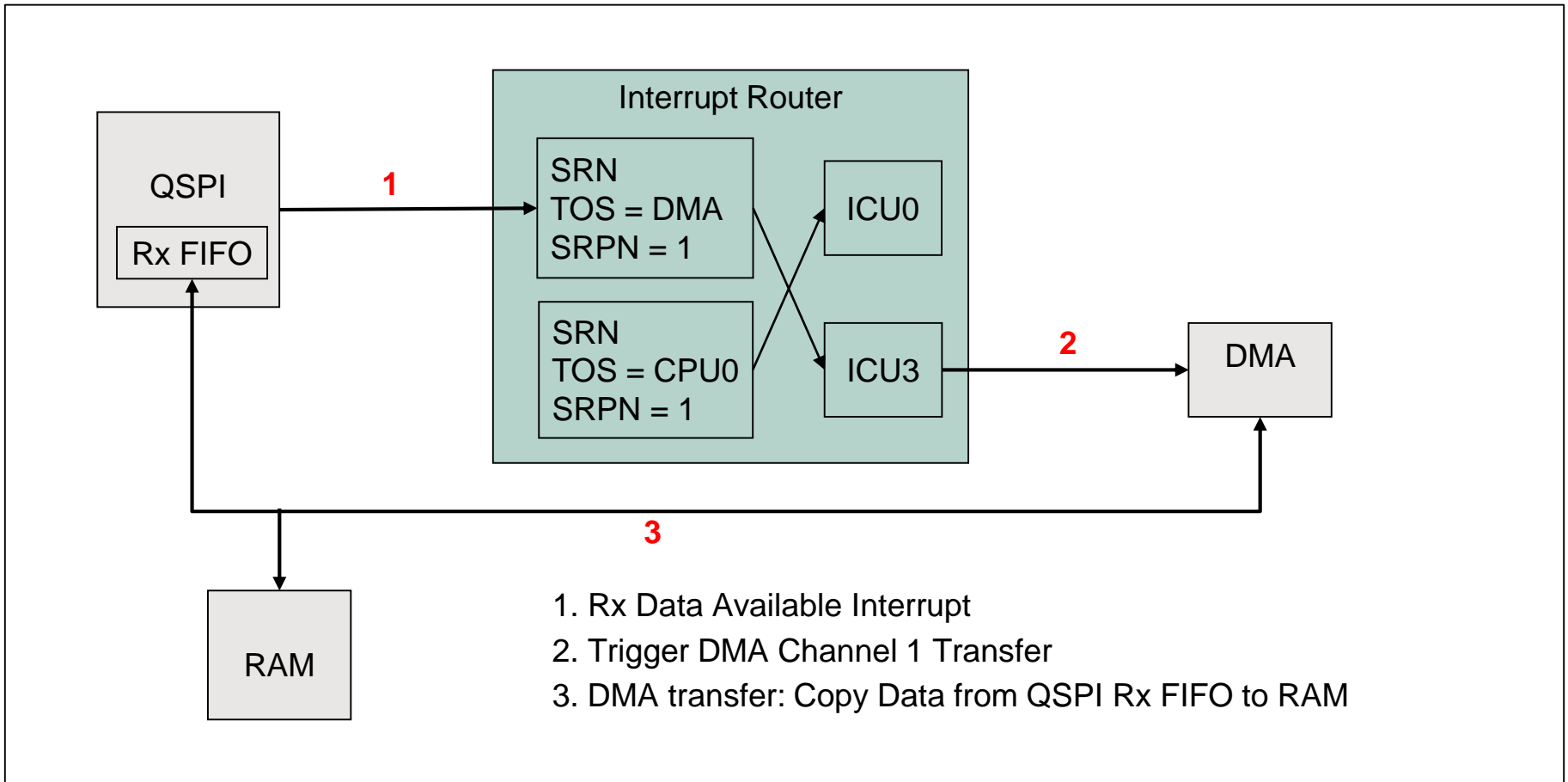
- › Each peripheral interrupt has a dedicated Service Request Node (SRN)
 - TOS and SRPN configuration, Interrupt Overflow, SW Interrupt Set/Clear
- › Each Service Provider has a dedicated Interrupt Control Unit (ICU)
 - Parallel and independant arbitration for pending service requests mapped to different ISPs



Application example

DMA transfer

- › In this example data is transferred from the QSPI FIFO registers to internal memory without any CPU intervention



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