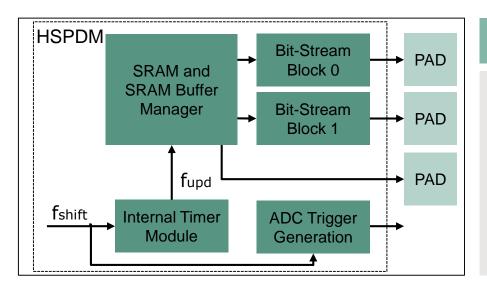
High Speed Pulse Density Modulation Module

AURIX™ TC3xx Microcontroller Training V1.0 2020-12



HSPDM High Speed Pulse Density Modulation Module





Highlights

- The High Speed Pulse Density Modulation (HSPDM) module is used to generate either a Pulse Density Modulated (PDM) bitstream or a Pulse Width Modulated (PWM) bit-stream with a fixed data rate up to 160 Mbps.
- Up to two independent synchronous bitstreams.

Key Features

Shift register generated bit-stream

ΔΣ modulator generated bit-stream

ADC Trigger Generation

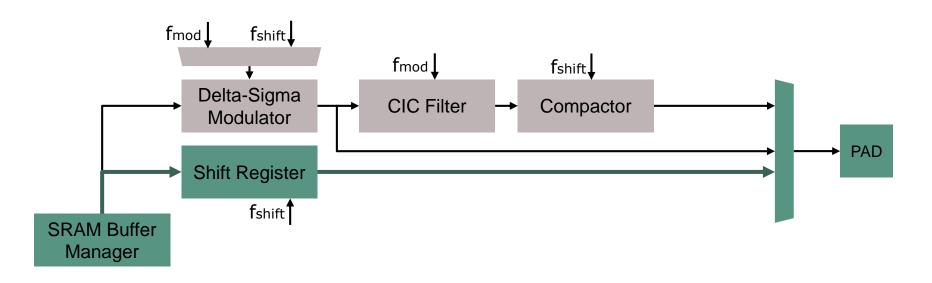
Customer Benefits

- PDM and PWM bit-stream generation
- Arbitrary waveform generation
- Ability to control an MMIC

Shift register generated bit-stream



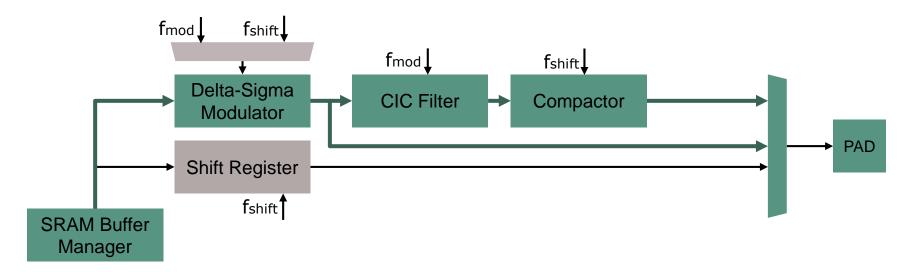
- In this mode, a 16-bit digital word is loaded by the bit-stream loader (inside the SRAM and SRAM buffer manager block).
- > The shift register serializes the 16-bit word and sends it bit-wise (LSB first) on the rising edge of the clock.
- At the output, a 1-bit bit-stream at 160 Mbps is generated which can be pushed out of the microcontroller through the multiplexer.
- > The Delta-Sigma modulator, the CIC filter and the Compactor are disabled in this mode of operation.
- > PWM signals with a resolution step of 6.25 ns can be generated in this mode.



ΔΣ modulator generated bit-stream



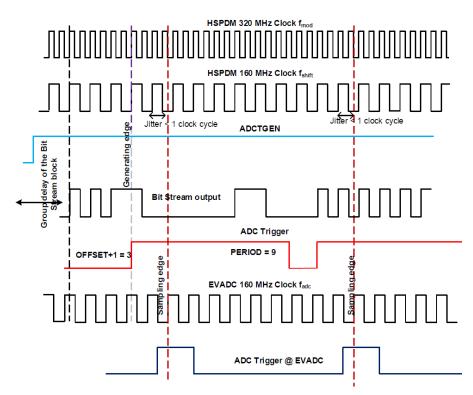
- Two modes can be chosen here:
 - ΔΣ modulator generated bit-stream with the CIC filter and the Compactor enabled:
 - A 16-bit digital word is loaded by the bit-stream loader at the input of the $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator runs at 320 MHz, generating a PDM bit-stream at 320 Mbps. The data rates higher than 160 Mbps are not supported by the microcontroller pads, therefore, the output of the modulator is decimated.
 - ΔΣ modulator generated bit-stream with the CIC filter and the Compactor disabled:
 - This mode is very similar with the above one, with the difference that the $\Delta\Sigma$ modulator is run at 160 MHz. The CIC filter and the Compactor are bypassed in this mode.



HSPDM ADC Trigger Generation



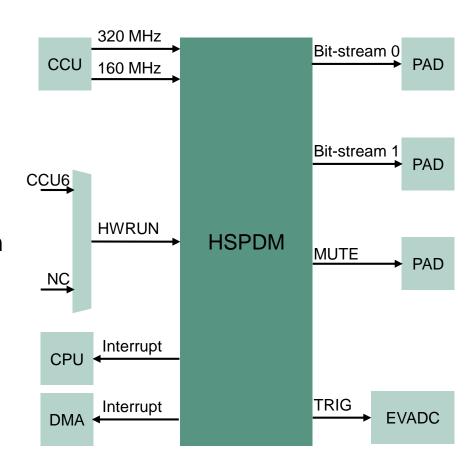
- The ADC Trigger Generation block inside of HSPDM generates a signal to trigger a group of Enhanced Versatile Analog-to-Digital Converters (EVADCs) to start the conversion.
- The user can easily enable/disable the ADC trigger generation or configure the trigger signal based on offset and period.



System integration



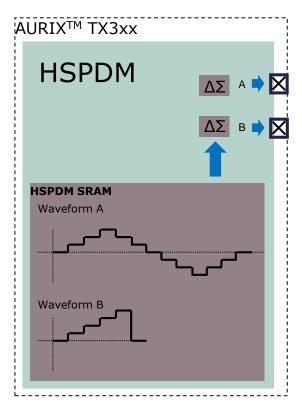
- The HSPDM can generate up to two independent 1-bit bit-streams. The bit-stream is a pulse-density modulated (PDM) bit-stream, which can be averaged outside the microcontroller using a low pass filter (LPF) to generate the analog voltage.
- The MUTE signal output from the microcontroller can be used to control external electronics (e.g. turn on or turn off an external transmitter).
- The clock signals are received from the Clocking Unit (CCU).
- HSPDM as many other peripherals can trigger interrupts which can be serviced by CPU or DMA.

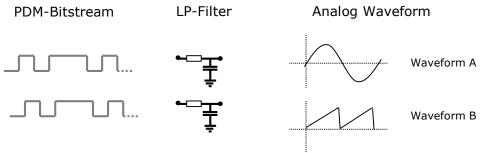


Application example Digital-to-Analog (DAC) Conversion



The main application of HSPDM is to create a DAC using the low frequency band up to 100 kHz.





- The waveform is stored as a set of digital datapoints (16-Bit) within the in-built SRAM of 8kB.
- The ΔΣ-Modulators can generate two independent 1-Bit pulse density modulated output bitstreams.
- A external low pass filter averages a bitstream to generate the analog voltage.
- The HSPDM together with external low pass filter may be used to control any analog interface device.

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