EBU
External Bus Unit
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Key Features
- Burst FLASH support
- Synchronous SRAM support
- Highly programmable access parameters

Highlights
- Allows to connect high variety of external memories
- Highly programmable access parameters for extended configuration capabilities to configure Bus components (Burst Flash, synchronous & asynchronous SRAM, NAND Flash, FPGA...)

Customer Benefits
- Extend the NVM capabilities for large SW Projects (code and constants)
- Extend the VM capabilities for large SW Projects (data)
- Wide variety of external memories can be supported
EBU
Burst FLASH support

The Memory Controller is designed to generate waveforms compatible with the access modes of:

- INTEL and compatible burst flash devices
- SPANSION and compatible burst flash devices
- Samsung OneNAND™ burst capable NAND flash and compatible devices
- M-Systems DiskOnchipG3 and compatible devices
Synchronous SRAM support

The Memory Controller is designed to generate waveforms compatible with the asynchronous/synchronous modes of:

- Standard asynchronous SRAM
- Standard synchronous SRAM
- INFINEON and MICRON cellular RAM
- Fujitsu and compatible FCRAM™/uTRAM™/CosmoRAM
- SSRAM from e.g. GSI/ISSI/IDT
Highly programmable access parameters

- Fully synchronous/asynchronous timing with flexible programmable timing parameters (address cycles, read wait cycles, data cycles). This allows optimized control waveforms to be generated for controlling accesses to the attached memory devices.
- Programmable WAIT function, which allows support of memory devices with a variable access latency.
- Programmable burst (mode and length).
- 8-bit/16-bit/32-bit device width.
- Page mode read accesses.
- Resynchronization of read data to a feedback clock to maximize the frequency of operation (optional).
The Memory Controller module for SRI-based systems connects on-chip controller cores (e.g. TriCore™ CPU, DMA Controller) to external resources such as memories and peripherals.

Any SRI master can (in conjunction with an SRI Matrix) access external memories through the Memory Controller.

A pin multiplexing scheme has been implemented to allow the use of low power, 5 V compatible pads for the 32 bit data bus.
Application example
Typical external memory system

Overview
› External Flash memory
› External SRAM memory

Advantages
› Extend the memory capabilities for large SW Projects (code, constants and data)
› Multiplexed access (address & data on the same bus)
› Data buffering (1 single write buffer to SRI & 2 read buffers)
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