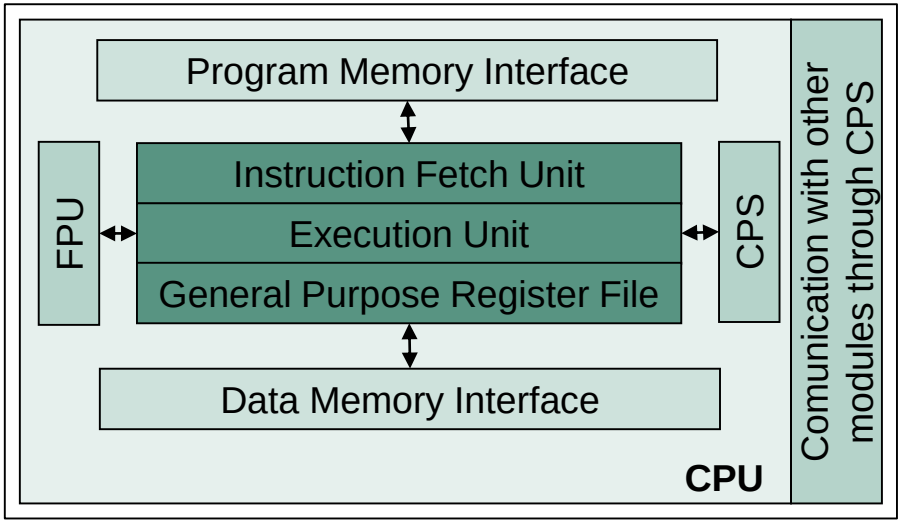
CPU

Central Processing Unit

AURIX™ TC2xx Microcontroller Training
V1.0 2019-03

Please read the Important Notice and Warnings at the end of this document

CPU
Central Processing Unit



Highlights

- The Central Processing Unit (CPU) comprises of an Instruction Fetch Unit, an Execution Unit, a General Purpose Register File (GPR), a CPU Slave interface (CPS), and Floating Point Unit (FPU).

Key Features

- Temporal protection system
- Flexible memory protection
- Wide range of supported instructions

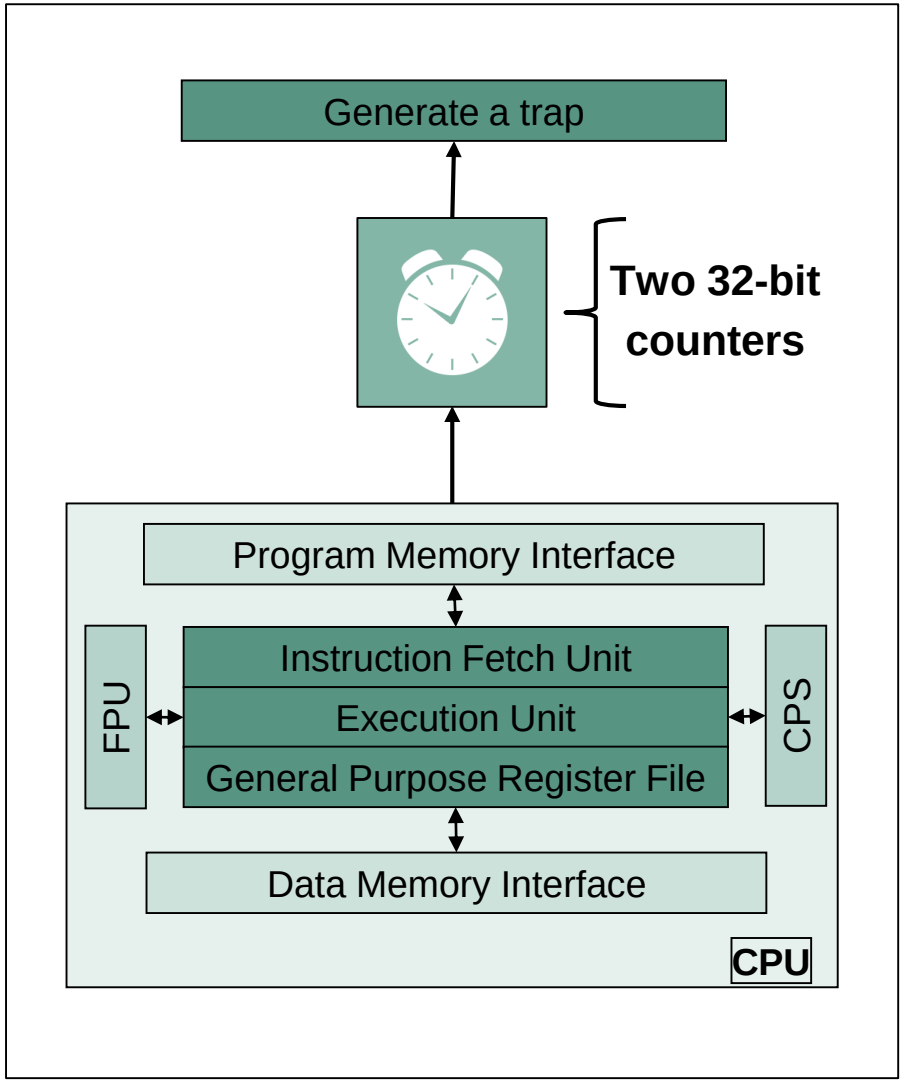
Customer Benefits

- Time bounded real time operation
- Multiple protection ranges over the memory
- Code optimization (e.g. reduced code size by using 16-bit & 32-bit instructions)

Copyright © Infineon Technologies AG 2019. All rights reserved.

CPU
Temporal protection system

A very common problem of real time systems is given by the tasks with a defined runtime. Overrunning this can lead to overall program failures.
Each core has a temporal protection system (TPS) formed out of two 32-bit decrementing counters clocked by the primary clock.
The operating system (OS) loads the expected runtime at task‘s start and a trap is generated when the counter reaches 0. Generating a trap and not an interrupt, protects the system in case the task is allowed to disable interrupts for periods of time.
Based on the counters‘ values (together with the time-out flags), it is ensured that the real time application is time bounded.



Copyright © Infineon Technologies AG 2019. All rights reserved.

CPU
Flexible memory protection

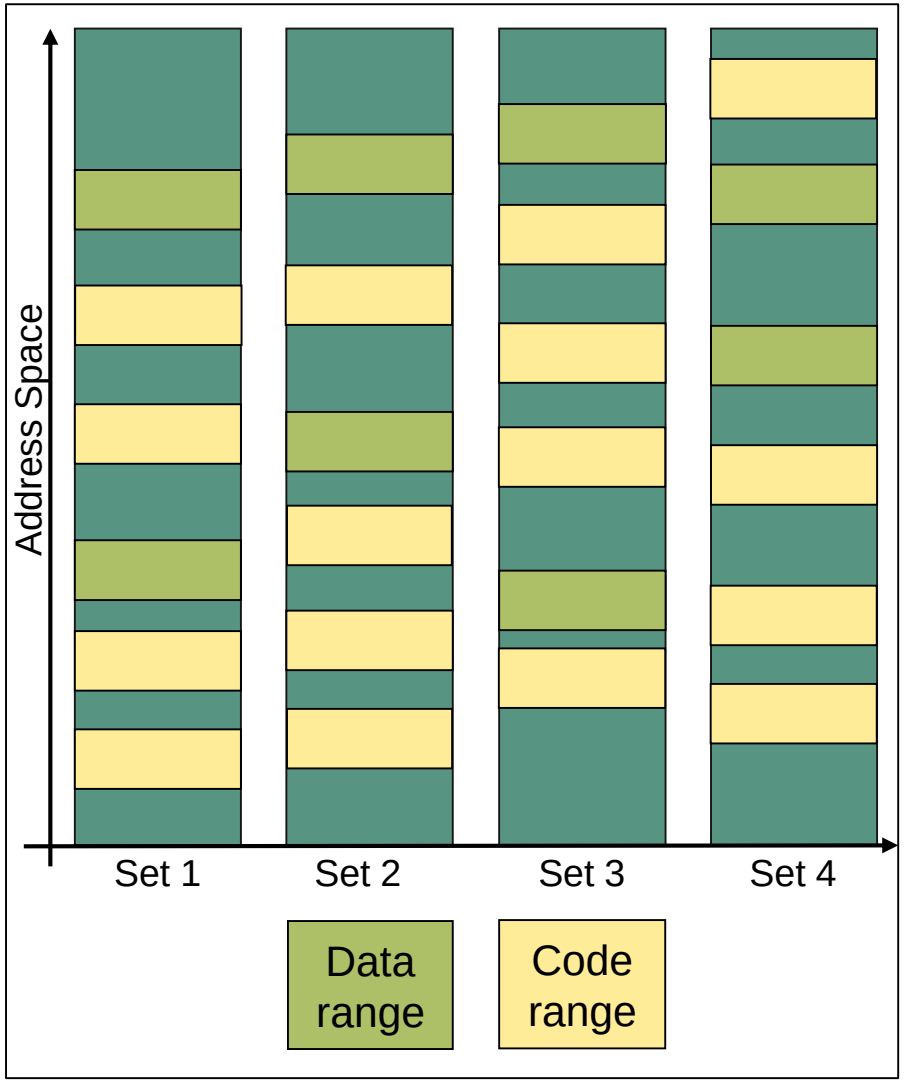
For each task of the real time system, memory resouces are defined. If these resources are outrun, failures appear in the application.

The memory protection stops a program overrunning its assigned region of memory and it is based on access permissions defined by address ranges.

Data access permissions are defined by any combination of write enable and read enable. Fetch access permision is based on access enable rights.

Fast permission switching is based on 4 protection sets with up to 16 defined data ranges and up to 8 defined code ranges.

The range to set asignment is flexible, which enables setting the right memory protection for the application at hand.

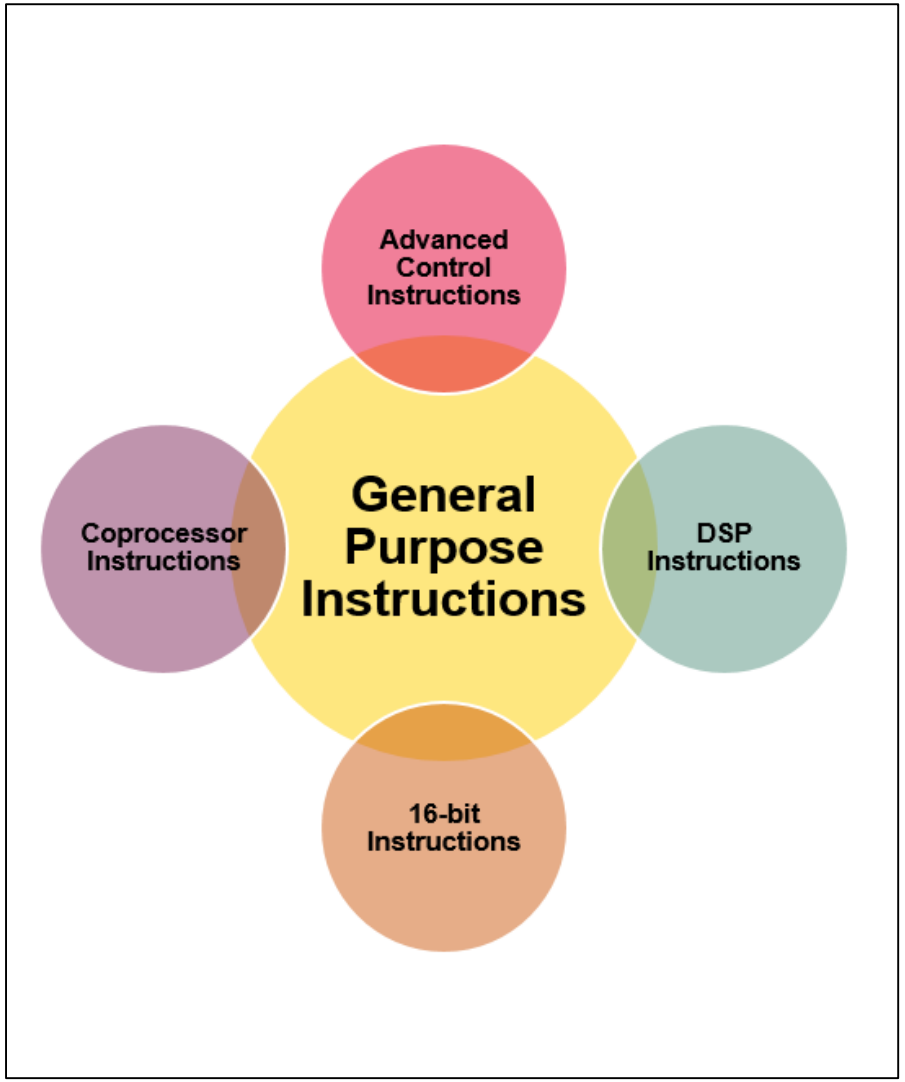


Copyright © Infineon Technologies AG 2019. All rights reserved.

CPU
Wide range of supported instructions

This very rich instruction set covers 16-bit and 32-bit format instructions, which can be freely mixed in the instruction stream, reducing code size and optimizing the application. The instruction set support a number of data types including bytes, signed and unsigned integers, single precision floating-point and 16- and 32-bit signed fractions.

TriCore™ Instruction Set	
General Purpose Instr.	Arithmetic, Logic Address Arithmetic & Comparison, Load/Store, Context Switch
Advanced Control Instr.	Bit-field, Bit-logical, Min/Max Comparison, Branch
Coprocessor Instr.	Floating Point
16-bit Subset	Load/Store, Arithmetic, Branch
Digital Signal Processor (DSP) Instr.	MAC, Saturated Math, DSP Addressing Modes



Copyright © Infineon Technologies AG 2019. All rights reserved.

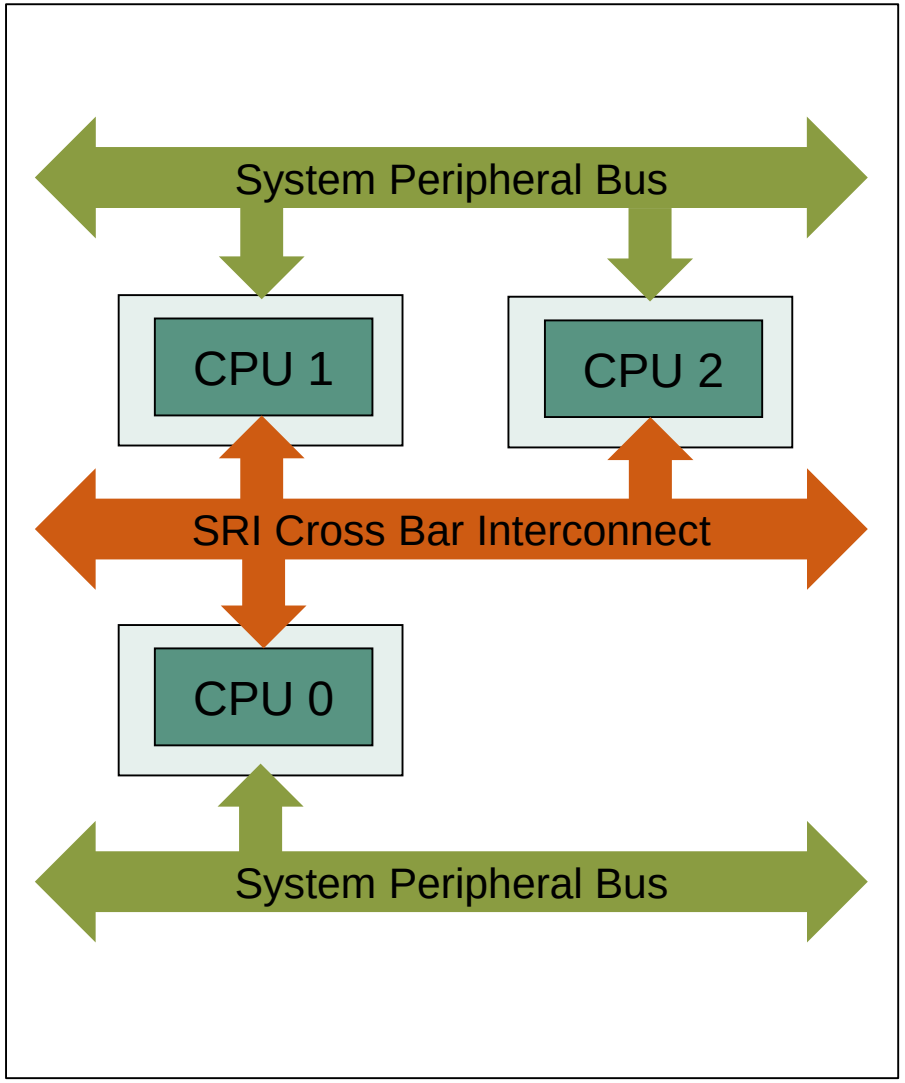
CPU
System Integration

The AURIX 32-bit microcontroller family contains a wide range of safety oriented devices varying from single core to triple core versions.

One of the most important features of the family is the "lockstep" capability. A core operating in Lockstep mode consists of a master and checker core. The checker core executes the same instructions as the master core, but it is two clock cycles out of phase. In case the outcome of a checker core is different from the master, an alarm is generated.

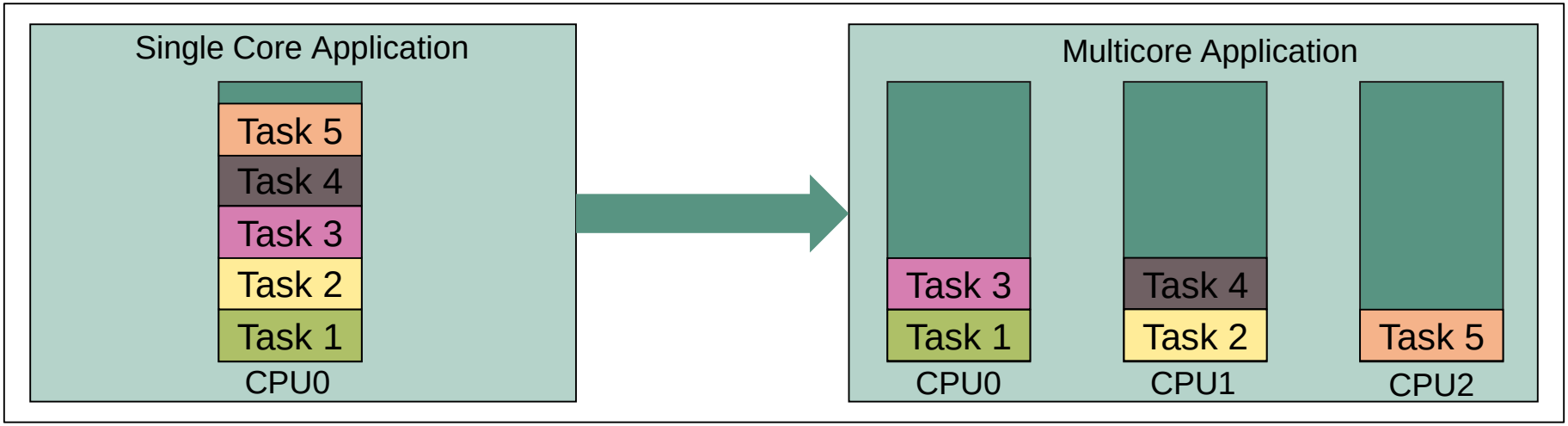
Moreover, another two flavors of cores are added: Performance Core (TC1.6P) or Efficiency Core (TC1.6E). TC1.6P cores are superscalar, being able to execute integer and load/store instructions in parallel and improving the performance by 15-25%. Nonetheless, both types of cores have a single precision, 2 FLOPS/cycle floating point unit.

No matter the type of core, each CPU is connected to the SRI Cross Bar Interconnect, which ensures the fast exchange of data between the cores. Moreover, the CPUs are connected to the System Peripheral Bus, which grant them access to all the peripherals. Each device has a highly predictable architecture, certain combination of performance/efficiency and lockstep/non-lockstep cores, which grant performance and safety to the applications.



Copyright © Infineon Technologies AG 2019. All rights reserved.

Application Example
Multicore application



Overview

Issue: Real-time applications running multiple tasks have the issue of overloading the CPU.

Solution: Switching to a multicore system, where tasks are divided over 2 or 3 cores. In the case of tasks depending on each other, the needed communication and scheduling will slightly reduce the performance.

Advantages

- Avoid CPU overload
- Improvement of overall system‘s performance up to 200%
- Clear division of tasks over the whole system (moving from „one-man show“ to „team work“)

Copyright © Infineon Technologies AG 2019. All rights reserved.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-03
Published by
Infineon Technologies AG
81726 Munich, Germany

© 2019 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
AURIX_Training_1_
Central_Processing_Unit

IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.