AUIRDC1170 User Guide

Reference Design for AUIRS1170S

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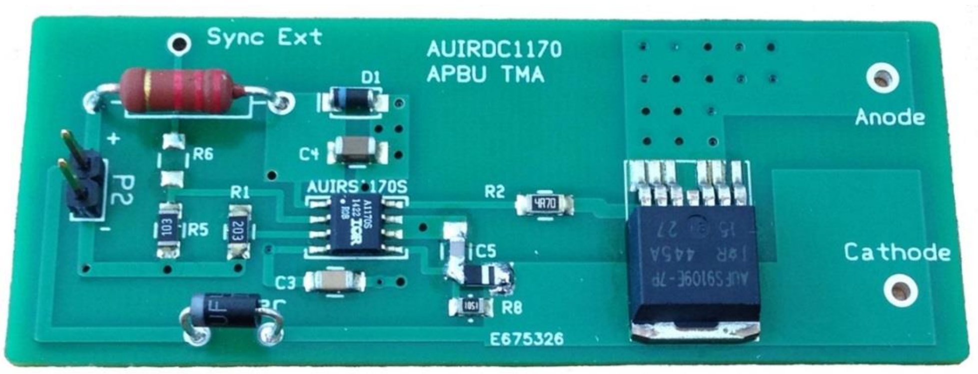
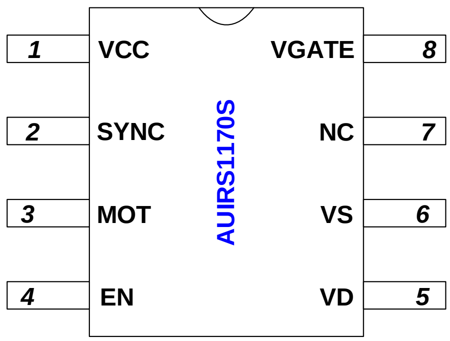


Introduction & Device Overview

The AUIRS1170S is an automotive qualified smart secondary side gate driver IC designed to drive N-channel power MOSFETs as synchronous rectifiers in both hard switching and soft switching / resonant converters. The IC can control one or more MOSFETs in parallel to emulate the behavior of very low Vf diodes.
The drain to source voltage of the MOSFET switch is sensed to determine the value of the current and the device is turned ON and OFF in close proximity of the zero current transition.
The pin-out for the 8 pin device is shown here below.



PIN #	Symbol	Description
1	VCC	Supply Voltage
2	SYNC	SYNC Input for direct turn off
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing and GND connection
7	NC	Not connected
8	VGATE	Gate Driver Output

From a functional point of view, the device is an improved and Automotive qualified version with respect to previous smart rectifier ICs, in that:

a) output current capability has been increased to 3A source / 6A sink;
b) a SYNC input has been added, which allows to anticipate the turn-off transition, or to delay the turn-on transition, complementing the Vds voltage sensing function. This is especially useful in hard switching topologies where shoot trough due to very short current transition between mosfets has to be avoided, such as in forward converters.

The AUIRS1170S main characteristics are shown in Table 1.

Topology	Resonant Half/Full Bridge, Flyback, Forward
V_D	200V
V_{OUT}	10.7 V
I_{O+} & I_{O-} (typical)	+3/-6A
Turn on propagation Delay	60ns (typical)
Turn off propagation Delay	50ns (typical)

Table 1: AUIRS1170S main characteristics

A very common application diagram is shown in figure 1: this is the typical center tapped output stage of a High Voltage DC/DC converter using Half/Full bridge LLC topology; due to its flexibility and features the same device is a perfect fit also in Flyback, ZVT fixed frequency (Phase Shift ZVS) and forward converters topologies.

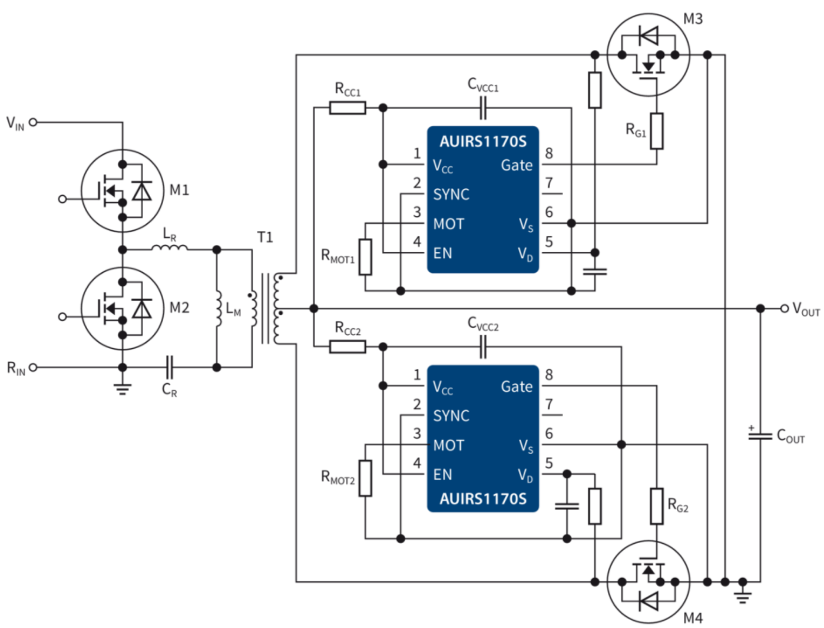


Figure 1: typical application diagram of the AUIRS1170S in a HV-DC/DC converter

The detailed functionality of each pin is described in the AUIRS1170S data sheet. For a more detailed introduction to device's operation, external components calculation and general layout guidelines, see also AN1205.

Reference Board Description

The reference board is designed to emulate the behavior of a TO247 or TO220 diode and directly replace it in its socket.
It includes a AUIRS1170S IC, biasing circuitry and one AUIRFS9109-7P or IPB180N10S4-02, 100V power mosfet with 2.4 mOhm rdson at Tj=25C.
Schematic is shown in Figure 2, while the layout is depicted in Figure 3.
The board is just 1.16 x 2.995 square inches (about 29 x 77mm) and can be interfaced to the specific customer converter board by the simple A and K connections, just like a power diode.

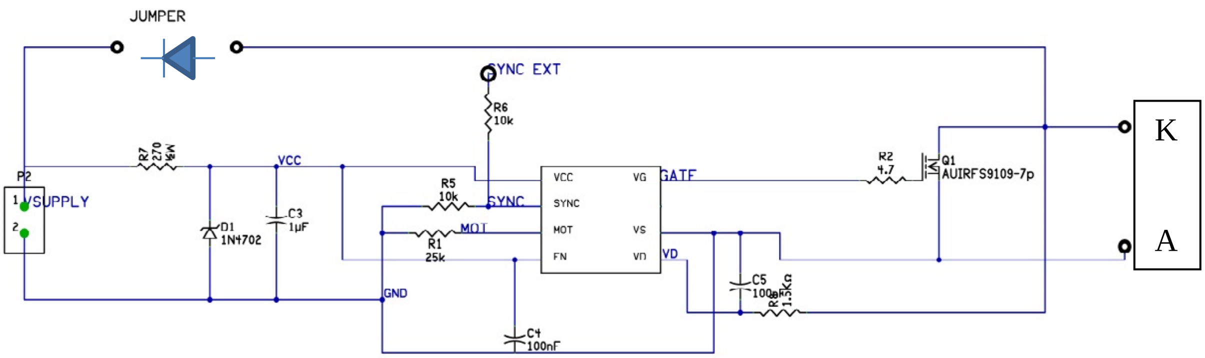


Figure 2: Reference board schematic

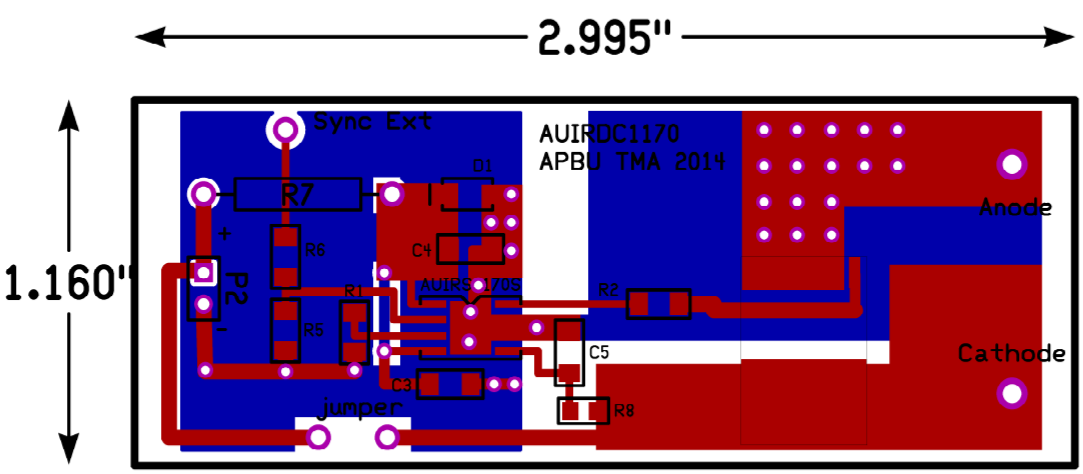


Figure 3: reference board layout

How to use AUIRDC1170

Voltage ratings

The maximum voltage limit between anode and cathode outputs is dictated in this demoboard by the power mosfet.
The 100V mosfet allows the board to be used in non-isolated converters with battery voltage of 48Vnom, or on the secondary side of isolated converters whose transformer secondary output voltage does not exceed 100V.
Because the IC is rated 200V and the mosfet allows for a certain amount of avalanche energy, 100V maximum rating can be exceeded for short periods of time (i.e. in case of voltage spikes during converter commutations) provided the extra dissipation due to avalanche energy is taken into account.
In no cases the K to A reverse voltage shall exceed 200V.

Power losses

The maximum current rating is dictated by the mosfet characteristics and by the board thermal resistance. The board has been characterised at IFX Labs and has a $Rth_{pcb\text{-}amb}$ of 19.5 C/W, without any airflow.
Not considering any avalanche energy, the mosfet power dissipation can be calculated, as a first approximation, as follows:

$$Ploss = Rds_{on} * Irms^2 + Psw$$

The body diode conduction losses are not considered because they happen for a very short period of time during each switching cycle.
Because the turn-off threshold of the IC is very close to zero, it is also assumed that the mosfet channel turn-off will occur at nearly zero current, therefore body diode recovery losses are also quite negligible.

From the considerations above, an indication of the I_{RMS} current rating of this demoboard, as function of ambient temperature Tamb and switching frequency is shown in Figure 4, at Vdc = 48V, Vout = 12V and when using Rgate = 4.7 Ohm.

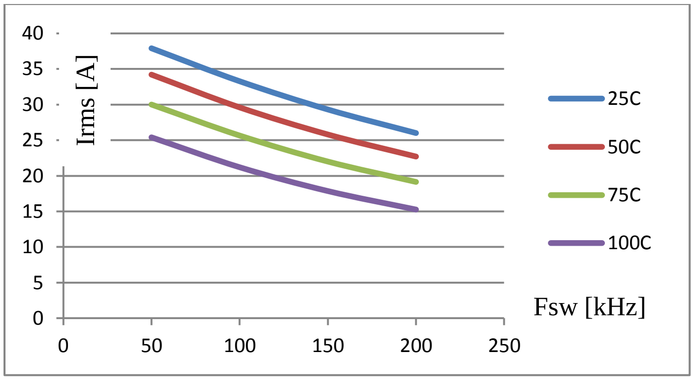


Figure 4: I_{RMS} rating vs Tamb and Fsw

Demoboard auxiliary supply

The AUIRS1170S needs some auxiliary power to properly work, here in the following the calculation example.

In the reference board, such power can be provided by an external, isolated, power supply, connected to connector P2, or can be directly derived by the Cathode terminal (the drain of the mosfet) by placing a 200V - 1A diode between the two "jumper" vias.

The board is equipped with a power resistor R_7 between the P2 positive terminal and the Vcc of the IC, while the zener diode D1 limits Vcc to 12V.

The value and the power rating of R_7 has to be determined depending on the available external auxiliary supply at P2 pins or, in case the self-supply option is chosen, depending on the voltage across K-A and its duty cycle.

Some basic indications on how to calculate R_7 in this last case are in the following chapter.

Supply resistor value

The Vcc filter capacitor will be charged via R_7 only when the mosfet is in its OFF state. Let's call this voltage Vdc. Let's also consider the case of a fixed frequency, PWM-modulated converter and assume the mosfet will be in its OFF state during a time = D*Tsw, likely because during this time the converter main control switch will be in ON state (and the "SR diode" in OFF state like in a flyback or buck converter).

The charging current via R_7 will be given by:

$$I_{R7} = I_L + I_Z$$

Where I_L is the current into the IC Vcc pin (Iqcc + FET gate current) and I_Z is the minimum current to bias the 12V zener diode. I_L depends upon many factors, including fsw, Vcc and the FET's Ciss. A general approximation is given by:

$$I_L = Iqcc + \frac{1}{2} * Ciss * Vcc * fsw \ \ [A]$$

Therefore by equating the needed supply charge vs. the input charge at every cycle, the following equation holds:

$$Q_{tot} = I_L * T = \frac{I_L}{fsw} \equiv \frac{Vdc - Vz}{R_7} * \frac{D}{fsw} \ \ [nC]$$

The Ciss of the AUIRS9109-7P is about 5nF. At fsw=100kHz, considering *Iqcc = 2mA* and *Iz = 1mA*, this corresponds to a $I_L = 2mA + 3mA + 1mA = 6mA$.

As a concrete example let's assume now a 48V converter, whose Vdc_{min} = 40V and D = 30%. From the equation above the maximum R_7 value as function of the duty cycle D at Vdc = 40V becomes:

$$R_{7max} = \frac{Vdc - Vz}{I_L} * D = \frac{40 - 12}{0.006} * D = 1400\ [\Omega]$$

As expected, at high duty cycle the mosfet remains OFF for a longer time and a higher R_7 is sufficient to provide the I_L + Iz current. On the other hand, for D becoming shorter, R_7 has less time available to supply the AUIRS1170S and its value becomes lower.

Power dissipation

As an example, let's assume R_7 = 2.2kOhm (demoboard case).
In the situation above R_7 will now be able to provide auxiliary supply for D > 47% and the Vcc filter shall provide the power for all the time the synch mosfet is in its ON state = (1-D)*Tsw.
The power dissipated into R_7 can be estimated as follows:

$$Pdiss_{R7} \cong \left(\frac{Vdc - Vz}{R_7}\right)^2 * R_7 * D = \left(\frac{40 - 12}{2.2k}\right)^2 * 2.2k * 0.47 \cong 168mW$$

Therefore, a 0.5W resistor will be enough, provided Tamb is limited to the value dictated by the resistor specifications.

Vcc filter capacitor

Now, the Vcc filter capacitor has to be sized. It will provide the charge during the (1-D)*Tsw time. Assuming to accept a max of 1V voltage drop, the capacitor value as function of D is estimated as follows:

$$Cmin \cong \frac{I_L}{\Delta V} \frac{(1 - Dmin)}{fsw} = \frac{6m}{1} \frac{(1 - 0.05)}{100^3} = 57nF$$

Therefore, a 100nF capacitor is enough to cover a duty cycle D range between 5% and 95%. To get some margin, a 1uF capacitor is used on the board, and another 100nF is placed close to the Enable pin, tied to Vcc

Switching Noise filtering

The board is equipped with a small filter (R8-C5) placed between the mosfet drain and pin Vd of AUIRS1170S. For the sizing of such filter, please refer to AN1205.
The resistor on pin 3 of the IC (MOT pin) is set at 20kOhm. This gives a Minimum ON Time of about 800nsec (please refer to AUIRS1170S Data Sheet for more details about MOT functionality).

The functionality of the AUIRS1170S is always guaranteed in the board because the Enable pin (pin4) is directly connected to Vcc. There are no provisions to disable the IC, except by using the external Synch,
The board is equipped with a Ext. Synch input. For the Synch function, please refer to AUIRS1170S Data Sheet. The IC Synch input (pin 2) is active high, so in the board it is pulled down by a 10kOhm resistor. Another 10kOhm resistor connects pin2 with external Synch.
Pin2 must NEVER go beyond Vcc, therefore considering the voltage divider provided by R5 and R6, the external Synch voltage must never exceed 2*Vcc.

Reference Board Main waveforms

This AUIRDC1170 demoboard was demonstrated in a hard switching positive-tied synchronous buck converter as in Fig. 5. In this topology the AUIRS1170S has been used to drive the upper (or synch) Fet, this way thanks to this device we implemented a Buck converter without the need of a high side driver.

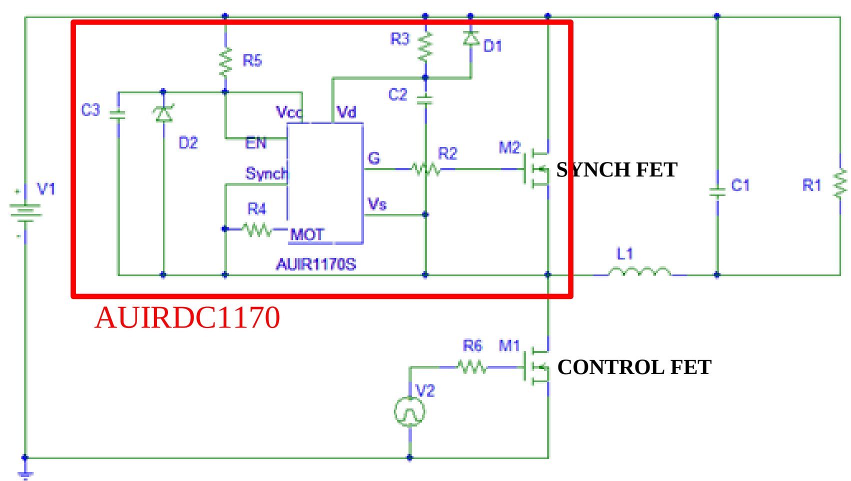


Figure 5: the positive-tied synch. Buck converter test schematic

Figure 6 shows the main converter waveforms, recorded in the following conditions:

Vin = 48V
Vout = 26V
D = 54%
Iout = 8.5A
Fsw = 50kHz

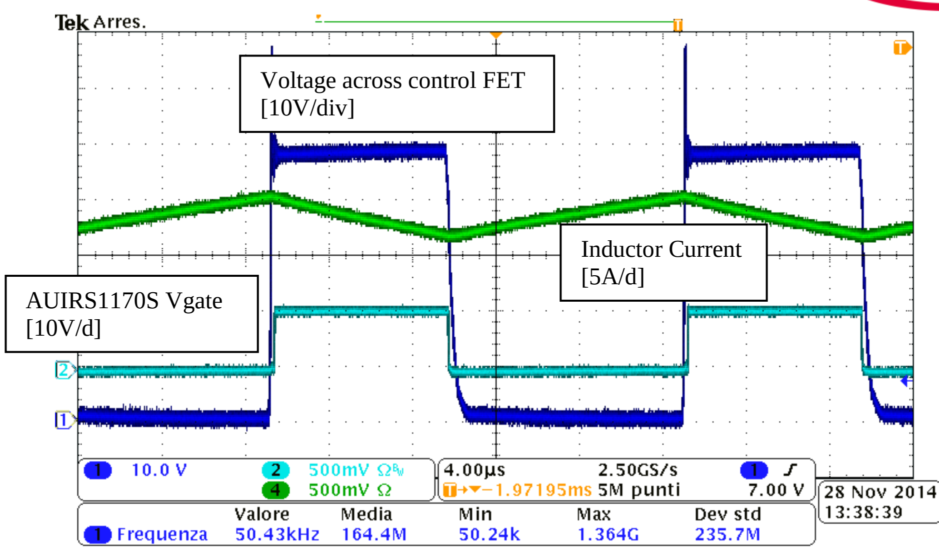


Figure 6: Positive-tied Buck converter waveforms

As show in Fig.6, after the control Fet turns-off, the AUIRS1170S immediately turns-on the floating Synch. Fet and keeps it in conduction until the control Fet turns back on at the beginning of the following cycle. During the synch Fet conduction the inductor discharges its energy to the load, therefore its current decreases.

Conclusions

The AUIRDC1170 evaluation board provides a simple and effective tool to quickly evaluate the AUIRS1170S smart driver IC, by simply replacing the little board into the original TO220 or TO247 diode socket of a DC/DC converter. Possible applications include hard switching or resonant topologies, with switching frequencies up to several hundred kHz, voltages up to 100V and currents up to several tens of amps.

References

- AUIRS1170S Data sheet
- Application Note AN1205 - Design of Secondary Side Rectification using the AUIRS1170S Smart-Rectifier Control IC
- Article: A Novel, High Efficiency Approach to Input Bridges

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