



The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

Continuity of Ordering Part Numbers

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

ON-SCREEN DISPLAY CONTROLLER

**ASSP FOR SCREEN DISPLAY CONTROLLER
MB90096**

USER'S MANUAL

ON-SCREEN DISPLAY CONTROLLER

**ASSP FOR SCREEN DISPLAY CONTROLLER
MB90096**

USER'S MANUAL

1. The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
2. The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.
3. The contents of this document may not be reproduced or copied without the permission of FUJITSU, Ltd.
4. FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5. Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
6. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.

CONTENTS

1 OVERVIEW	1
1.1 Description.....	1
1.2 Features	1
2 PINS	3
2.1 Pin Assignment.....	3
2.2 Pin Description.....	4
2.3 Block Diagram	6
3 DISPLAY FUNCTIONS	7
3.1 Screen Configuration	7
3.1.1 Screen configuration	7
3.1.2 Screen display modes	9
3.1.3 Screen output control	10
3.1.4 Screen display position control	11
3.2 Font ROM Configuration.....	17
3.3 Display Memory (VRAM) Configuration.....	18
3.3.1 Display memory and display screen	18
3.3.2 Writing to Display Memory	19
3.4 Text Display	21
3.4.1 Displayed character configuration	21
3.4.2 Character colors	24
3.4.3 Character trimming	25
3.4.4 Line enlarged display	31
3.4.5 Graphic character control	33
3.4.6 Blink control	36
3.4.7 Transparent/translucent color control	39
3.5 Character Background Display	41
3.5.1 Character background display	41
3.5.2 Shaded background succeeding character merge display	44
3.5.3 Shaded background succeeding line merge display	45
3.5.4 Character background extended display	46
3.6 Line Background Display	47
3.6.1 Line background display	47
3.6.2 Shaded background succeeding line merge display	49
3.7 Screen Background Display	55
3.7.1 Screen background character display	55
3.7.2 Screen background color display	57
3.8 Sprite Character Display.....	58
3.9 Command ROM Transfer Control.....	61
4 CONTROL FUNCTIONS	63
4.1 Serial Command Control	63
4.2 Dot Clock Control.....	64

4.3	Sync Signal Input.....	67
4.3.1	Vertical synchronization detection	67
4.3.2	Field detection	68
4.4	Display Signal Output	71
4.4.1	Display signal output timing	71
4.5	Scan Methods.....	74
5	DISPLAY CONTROL COMMANDS	77
5.1	Command List.....	77
5.2	Command Description	79
6	APPLICATIONS	94
6.1	Application Circuit Example	94
6.2	Power Supplies	95
6.3	Treatment of Unused Pins	96
6.4	Notes on Use	97
6.5	Notes on Graphic Character Design	103
6.6	Notes on Loop Filter Design	104
6.6.1	Notes on designing a loop filter	104
6.6.2	Obtaining the time constant of the loop filter (lag-lead filter) for the MB90096	104
6.6.3	Evaluating the loop filter	109
APPENDIX	113

1 OVERVIEW

1.1 Description

The MB90096 is a multisync, on-screen display controller (OSDC) responding to a wide range of horizontal synchronization rates from 15 kHz to 120 kHz.

The MB90096 can display up to 32 characters by 16 lines at a high resolution of 24-by-32 dots per character; it is best suited for display on wide, large screen TVs and high-definition televisions (HDTVs) as well as on high resolution PC monitors.

The MB90096 provides the sprite display, screen background text display, and graphics display functions, enabling a variety of GUI displays.

The MB90096 contains display memory (VRAM), character font ROM, and a voltage-controlled oscillator (VCO), allowing characters to be displayed with few external components. It also contains command table ROM for storing display command data, minimizing the potential load on the microcontroller or microcomputer.

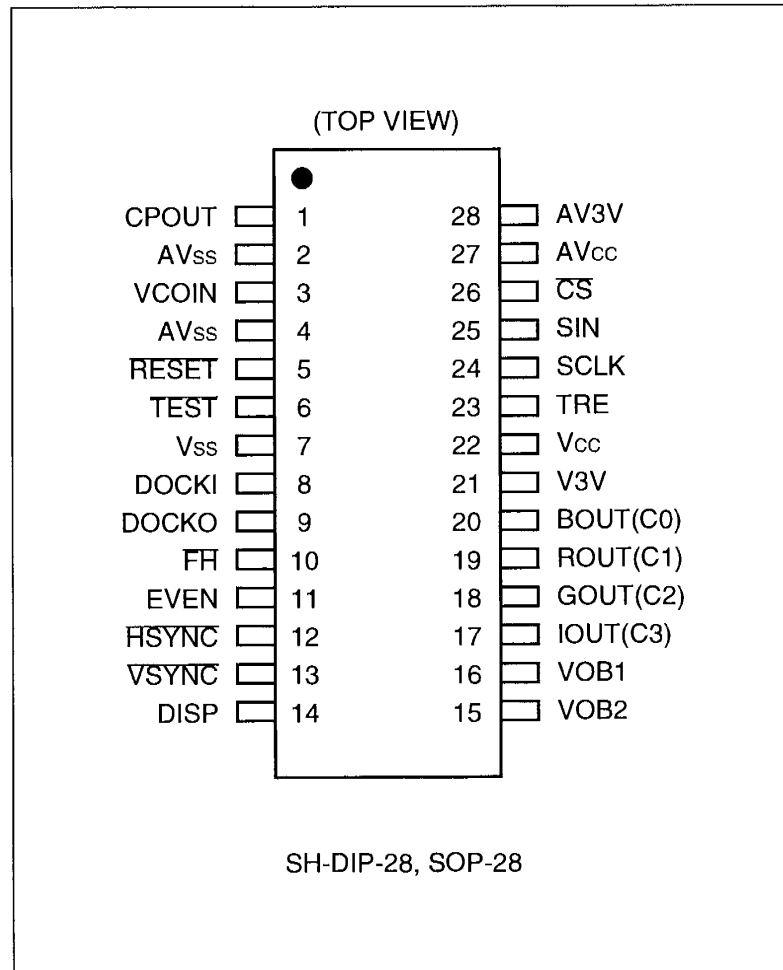
1.2 Features

- Main screen display capacity: Up to 32 characters × 16 lines (512 characters)
- Font sizes:
 - L size: 24 × 2h* dots (horizontal × vertical)
 - M size: 18 × 2h* dots (horizontal × vertical)
 - S size: 12 × 2h* dots (horizontal × vertical) *: h = 9 to 16The L, M, or S size can be set for each character.
Graphic characters can be displayed only in the L or S size.
Two values of "h" can be set for each screen, either of which is selected for each line.
- Character types: 512 different characters integrated
(user-settable through the entire area)
- Display modes:
 - Normal character/graphic character display
(Set for each character)
 - Trimmed display (horizontal trimming/pattern background)
(Set for each screen)
 - Character background (solid-filled/shaded background)
(Set for each character)
 - Line background (solid-filled/shaded background)
(Set for each line)
 - Enlarged display (normal, double width, double height, double height × double width) (Set for each line)
 - Blink display: Blinking (Set for each character)
Blink cycle and duty ratio (Set for each screen)
- Sprite character display (Only in graphics display mode):
 - Capable of displaying one block (of up to 2 × 2 characters, movable vertically or horizontally in 2-dot units) on the main screen
 - Only the first 256 characters (character codes 000 to 0FFH) can be set.

- Screen background character display (Only in graphics display mode):
 Capable of displaying a repetitive pattern (consisting of up to 2
 × 2 characters) below the main screen
 Only the first 256 characters (character codes 000 to 0FFH)
 can be set.
- Display colors:
 Character color/background color:
 16 colors each (Set for each character)
 Line background color/character trimming color:
 16 colors each (Set for each line)
 Screen background color: 16 colors (Set for each screen)
 Graphic character dot color: 16 colors (Set for each dot)
 Shaded background frame color (highlight/shadow):
 16 colors each (Set for each screen)
- Display position control:
 Horizontal display start position: Settable in 4-dot units
 (Set for each screen)
 Vertical display start position: Settable in 4-dot units
 (Set for each screen)
 Line spacing control: Settable in 2-dot units (Set for each line)
- Character/color signal output: ROUT, GOUT, BOUT, IOUT (color signals)
 VOB1 (OSD display period output signal)
 VOB2 (Translucent color period output signal)
- Command transfer function (macro service):
 16 Kbytes of internal command table ROM
- Range of supported horizontal synchronization rates:
 15 kHz to 120 kHz (PLL circuit integrated)
- Microcontroller/microcomputer interface:
 16-bit serial input (3 signal input pins)
- Package:
 SH-DIP-28, SOP-28
- Supply voltage:
 +5 V

2 PINS

2.1 Pin Assignment



2.2 Pin Description

Pin name	Pin No.	Input/output	Function
CPOUT	1	Output	Output pin for horizontal-sync phase comparison result signal . This pin is connected to an external lowpass filter.
VCOIN	3	Input	Internal VCO voltage input pin. This pin inputs the voltage signal from the external lowpass filter.
DOCKI	8	Input	Dot clock input pin. This pin is used only for operation with an externally generated dot clock.* ¹ Input a horizontal sync signal* ² (pin 12) to the pin when not in use. The pin has an internal pull-up resistor.
DOCKO	9	Output	Output pin for the dot clock generated by the internal VCO. This pin can be fixed to the High level by the command.
HH	10	Output	Output pin for the horizontal sync signal generated by the PLL circuit.
EVEN	11	Input	Field control signal input pin. This pin is disabled if noninterlaced display or internal generation is selected with the command. The pin has an internal pull-up resistor.
HSYNC	12	Input	Horizontal sync signal input pin. Dot clock generation is based on the cycle of the signal. The active level is programmable. The pin has an internal pull-up resistor.
VSNC	13	Input	Vertical sync signal input pin. The active level is programmable. The pin has an internal pull-up resistor.
DISP	14	Input	Display output (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) control pin. Setting this pin to the Low level forces the display output to the inactive level.* ³ The pin has an internal pull-up resistor.

*1 : Input the clock signal even during resets including the power-on reset.

For details, see “(1) Initial state after reset input” in Section 6.4 “Notes on Use.”

*2 : The active level of the input horizontal sync signal can accept either High or Low.

During resets including the power-on reset, the DOCKI pin must input either the signal fixed to the Low level or the horizontal sync signal which becomes Low at least once.

For further details, see “(1) Initial state after reset input” in Section 6.4 “Notes on Use.”

*3 : The display signals (IOUT, ROUT, GOUT, BOUT, VOB1, and VOB2) of the MB90096 may be output in the horizontal or vertical blanking interval.

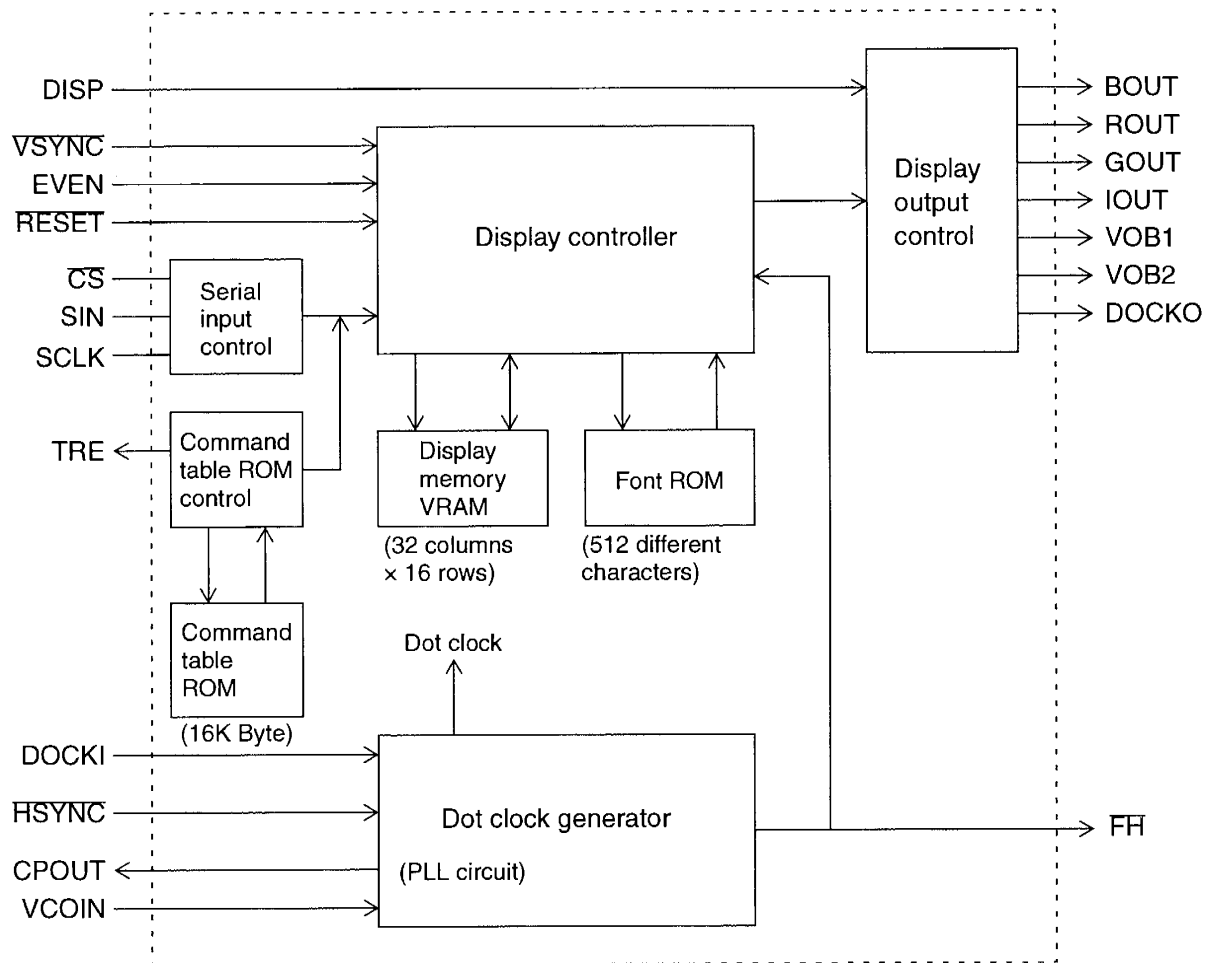
Since devices such as TV and computer monitors set the reference color level in the horizontal/vertical blanking interval, usually, the display signals of the MB90096 must be masked by the DISP pin in that period.

(Continued)

Pin name	Pin No.	Input/ output	Function
IOUT (C3) GOUT(C2) ROUT(C1) BOUT(C0)	17 18 19 20	Output	Color signal output pins. The active level is programmable.
VOB1	16	Output	OSD display period output pin. The active level is programmable.
VOB2	15	Output	Translucent color period output pin. The active level is programmable.
SCLK	24	Input	Serial transfer shift clock input pin. The pin has an internal pull-up resistor.
SIN	25	Input	Serial data input pin. The pin has an internal pull-up resistor.
\overline{CS}	26	Input	Chip select pin. For serial transfer, set this pin to the Low level. The pin has an internal pull-up resistor.
TRE	23	Output	Output pin to indicate that command transfer or fill operation is being executed. The signal is output at the active High level.
RESET	5	Input	Reset input pin. Input a Low level*4 signal to this pin when turning on the power. The pin has an internal pull-up resistor.
TEST	6	Input	Test signal. This pin inputs a High level (fixed) signal during normal operation. The pin has an internal pull-up resistor.
Vcc	22	—	+5 V power supply pin.
V3V	21	—	Connect a 0.1 μ F capacitor between this pin and Vss.
Vss	7	—	Ground pin.
AVcc	27	—	VCO +5 V power supply pin.
AV3V	28	—	Connect a 0.1 μ F capacitor between this pin and AVss.
AVss	2, 4	—	VCO ground pin.

*4: When the power is turned on, keep the input at the Low level for at least 1 ms after Vcc (AVcc) becomes stable.

2.3 Block Diagram



3 DISPLAY FUNCTIONS

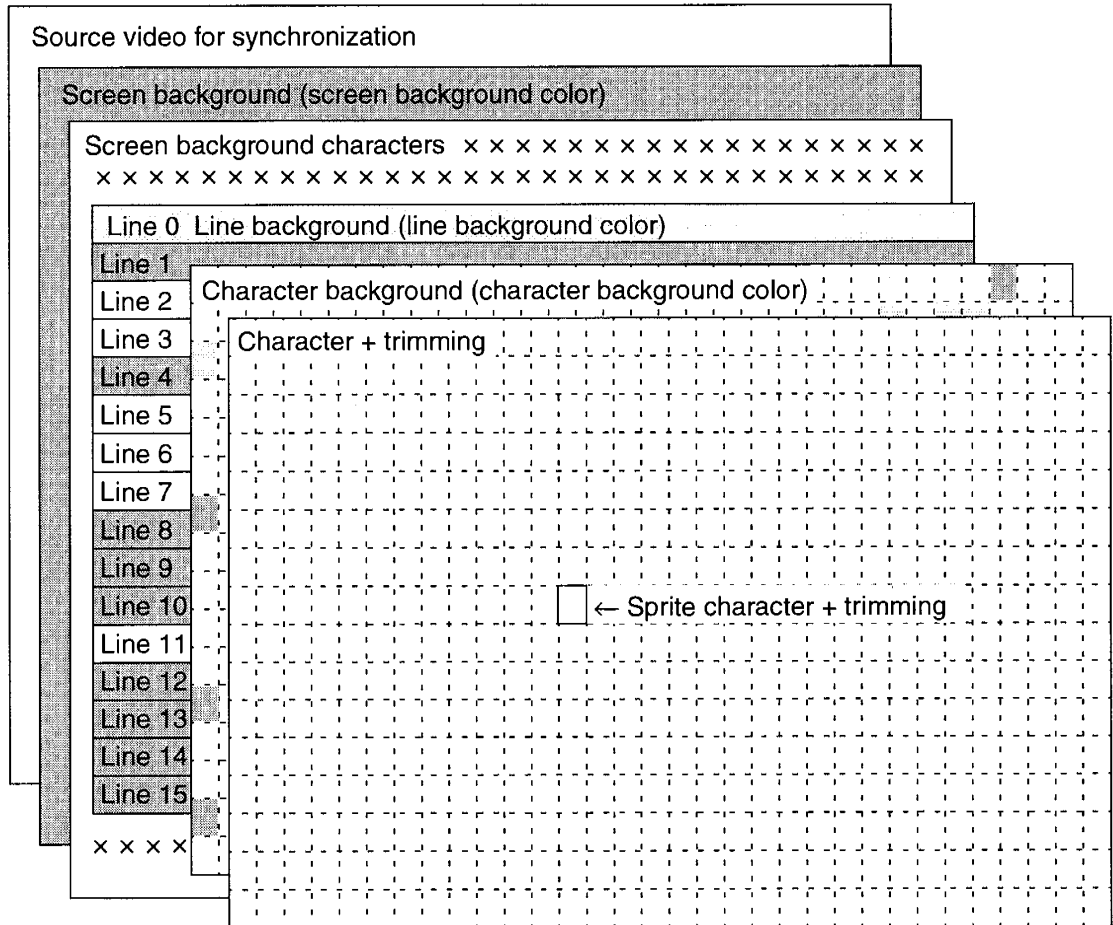
3.1 Screen Configuration

3.1.1 Screen configuration

The display screen consists of various screen elements.

	Display screen name		Screen configuration	Display position control
<div> Top layer <div> ↑ ↓ </div> Bottom layer </div>	Sprite character (+ trimming)		1 sprite character (consisting of 2 × 2 characters max.)	Horizontal/vertical: In 2 dots
	Main screen	Character (+ trimming)	32 characters × 16 lines	Horizontal/vertical: In 4 dots
		Character background	32 characters × 16 lines	(Character/ background concurrent control)
		Line background	16 lines (Full display from the left to right end of the screen)	(Character/ background concurrent control)
	Screen background character (+ trimming)		1 type (Repeatedly displayed pattern of 2×2 characters)	Fixed
	Screen background		(Full screen display in single color)	(None)

- Screen configuration drawing



Note: When a line is displayed on a line, the shaded background shadow frame for the line background overrides the character display.
 The shaded background shadow frame for the character background overrides the character display and the shaded background shadow frame for the line background.

3.1.2 Screen display modes

Display screen name		Display mode											
Screen background		Undisplay											
		Display											
Screen background character		Undisplay											
		Display	Pattern of 2 (vertical) × 2 (horizontal) characters				Character attribute		Graphic character				
Main screen	Line background	Undisplay						Line spacing	0 to 14 dots				
		Solid-fill display											
		Shaded background concaved display				Shaded background convexed display	Independent						
		Shaded background succeeding line merge					Merge						
	Character background	Undisplay											
		Solid-fill display						Character background extended (enabled with line spacing control on)	Normal				
		Shaded background concaved display	Shaded background succeeding character merge	Independent	Shaded background convexed display	Independent							
		Shaded background succeeding line merge		Merge		Merge	Extended						
	Character	Character attribute	Graphic character										
			Normal character	Undisplay (blank character)									
				Display	Trimming output control	Undisplay	Trimming mode	Horizontal trimming 1	Trimming type	Undisplay			
						Display with no character background				Horizontal trimming 2	Right trimming		
						Undisplay only within shaded background					Pattern background 1	Left trimming	
						Full display				Pattern background 2	Both-side trimming		
				Undisplay									
				Display	Consisting of a single character				Character attribute	Graphic character			
					Consisting of 2 horizontally lined characters								
					Consisting of 2 vertically stacked characters								
					Consisting of 2 × 2 characters								

3.1.3 Screen output control

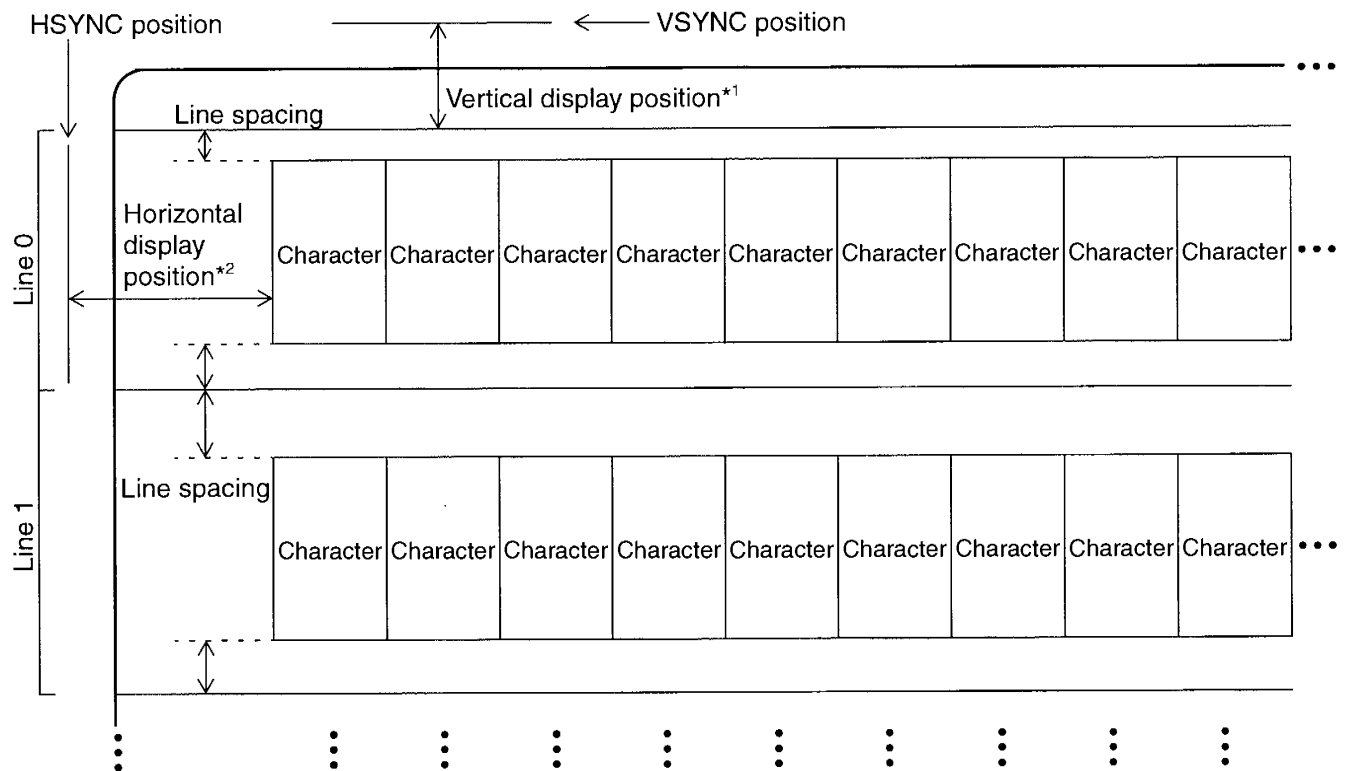
Display screen control	
Elements to be controlled	Control bit name (unit of control)
Character + trimming + character background + line background	DSP (screen)
Character + trimming + character background	LDS (line)
Character	M8 to M0 (character)
Character trimming	LFD to LFA (line)
Character background	MM1, MM0 (character)
Line background	LM1, LM0 (line)
Screen background character	PDS (screen)
Screen background color	UDS (screen)
Sprite character	SDS (screen)

3.1.4 Screen display position control

(1) Display position control on the main screen

The MB90096 controls the display start positions of a character (or a line of characters), character trimming, character background, and line background simultaneously.

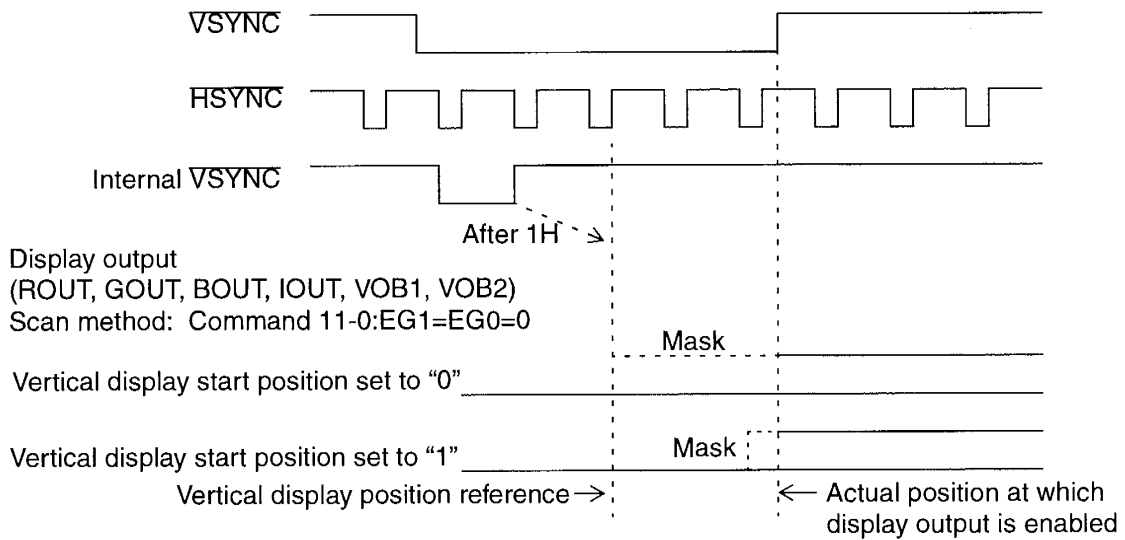
- Vertical display position: Vertical display position control (command 5-2), Bits Y8 to Y0
Set the vertical display start position relative to the VSYNC position.
The position can be set between 0 and 2044 dots in 4-dot units.
- Horizontal display position: Horizontal display position control (command 5-3), Bits X8 to X0
Set the vertical display start position relative to the HSYNC position.
The position can be set between 0 and 2044 dots in 4-dot units.
- Line spacing: Line control data set 1 (command 3), Bits LW2 to LO0
Set the number of dots to specify the width of the areas to be kept above and below the characters on each line.
The spacing specified by the set value will be kept both above and below the characters.
The line spacing can be set between 0 and 14 dots in 2-dot units for each line.
(Note: When line double-height display is on, the line spacing is doubled as well.)



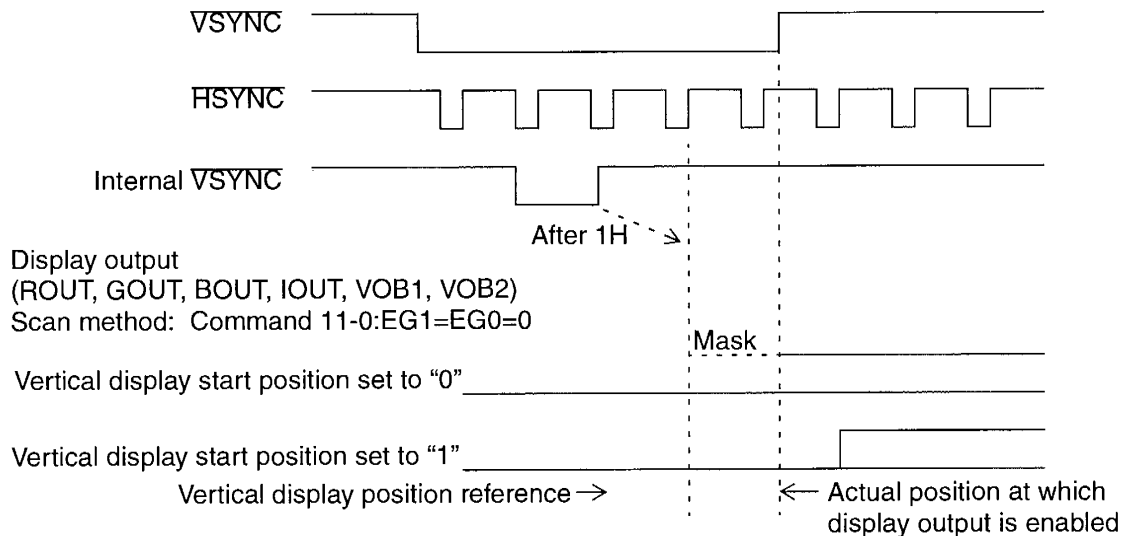
*1: Vertical display position

Counting for the vertical display position is started 1H after the internal VSYNC signal as shown below.

- When VHE = 0



- When VHE = 1



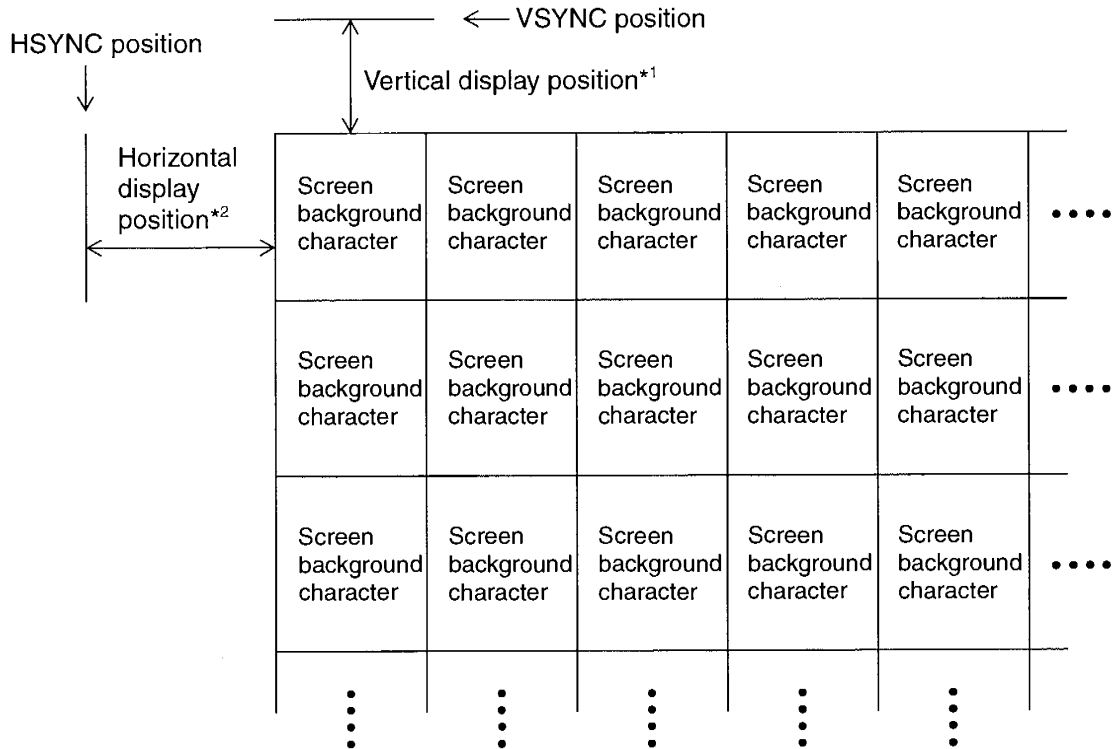
*2: Horizontal display position

The horizontal display position setting is offset as follows:

- When dot clock control 1 (command 11-2) DC0 = 0 (with an external dot clock input)
The set value is offset by about 98 dot clocks from the trailing edge of the horizontal sync signal (input to pin 12) pulse.
- When dot clock control 1 (command 11-2) DC0 = 1 (with the internal VCO selected)
The set value is offset by about 98 dot clocks from the trailing edge of the FH signal (output from pin 10) pulse.

- Notes:**
- Although the vertical display position reference is common to all scan methods (set by command 11-0:EG1, EG0), the progress of counting is different among them. (For details, see Section 4.5 “Scan Methods.”)
 - Display is started usually at the set display position. When $\overline{\text{VSYNC}}$ or $\overline{\text{HSYNC}}$ is active, however, the display outputs (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) are masked.
 - The offset (98 dot clocks) to the horizontal display position involves an error of several dot clocks, depending on the input timings of the dot clock and horizontal sync signal pulses, the PLL lock status, and on the display signal pin output delay.
For fine adjustment of the actual display position, check it during actual operation.

(2) Display position control of screen background characters



*1: Vertical display position

The vertical display position reference is the same as that on the main screen; it is 1H after the internal VSYNC signal.

*2: Horizontal display position

The horizontal display position setting is offset as follows:

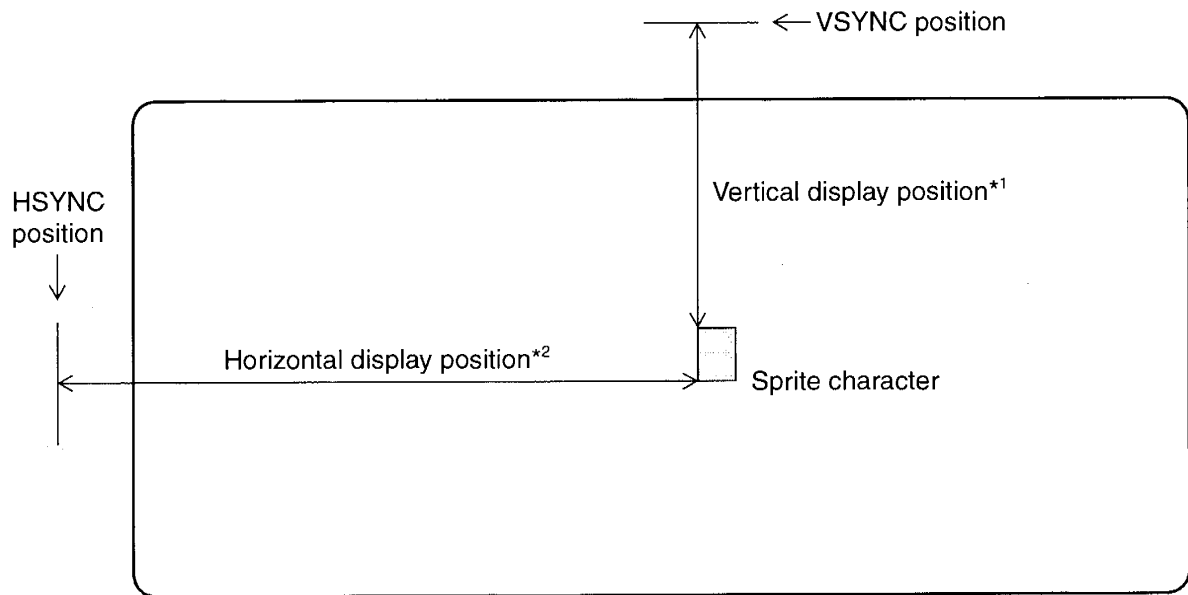
- When dot clock control 1 (command 11-2) DC0 = 0 (with an external dot clock input)
The set value is offset by about 65 dot clocks from the trailing edge of the horizontal sync signal (input to pin 12) pulse.
- When dot clock control 1 (command 11-2) DC0 = 1 (with the internal VCO selected)
The set value is offset by about 65 dot clocks from the trailing edge of the FH signal (output from pin 10) pulse.

- Notes:**
- The offset (65 dot clocks) to the horizontal display position involves an error of several dot clocks, depending on the input timings of the dot clock and horizontal sync signal pulses, the PLL lock status, and on the display signal pin output delay.
For fine adjustment of the actual display position, check it during actual operation.
 - When VSYNC or HSYNC is active, the display outputs (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) are masked.

(3) Display position control of sprite characters

The MB90096 controls the display start positions of a sprite character and its trimming.

- Sprite character vertical display position: Sprite character control 4 (command 9-0), Bits SY9 to SY0
Set the vertical display start position relative to the VSYNC position.
The position can be set between 0 and 2046 dots in 2-dot units.
- Sprite character horizontal display position: Sprite character control 5 (command 9-1), Bits SX9 to SX0
Set the vertical display start position relative to the HSYNC position.
The position can be set between 0 and 2046 dots in 2-dot units.



***1: Vertical display position**

The vertical display position reference is the same as that on the main screen; it is 1H after the internal VSYNC signal.

***2: Horizontal display position**

The horizontal display position setting is offset as follows:

- When dot clock control 1 (command 11-2) DC0 = 0 (with an external dot clock input)
The set value is offset by about 82 dot clocks from the trailing edge of the horizontal sync signal (input to pin 12) pulse.
- When dot clock control 1 (command 11-2) DC0 = 1 (with the internal VCO selected)
The set value is offset by about 82 dot clocks from the trailing edge of the FH signal (output from pin 10) pulse.

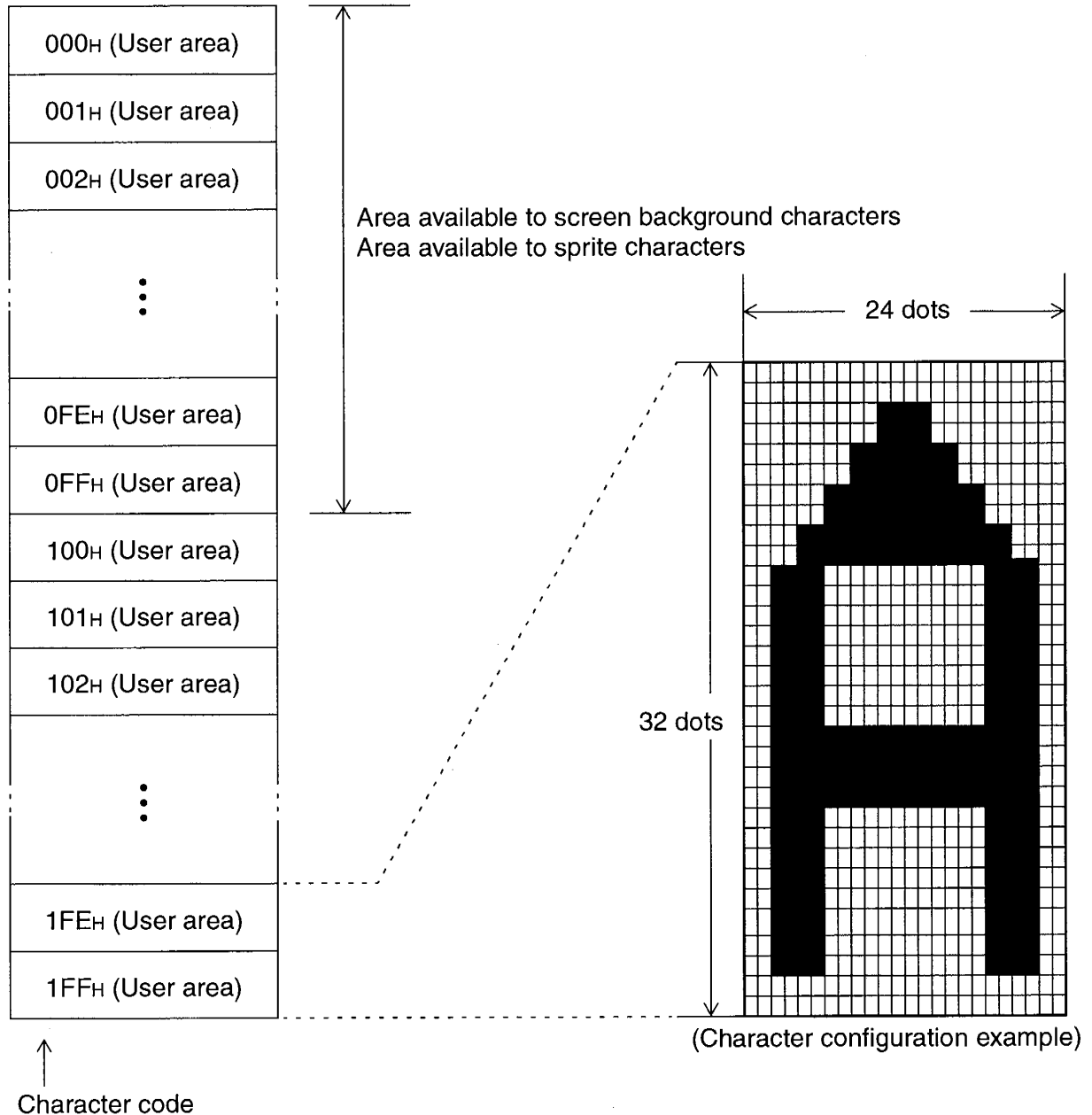
- Notes:**
- The offset (82 dot clocks) to the horizontal display position involves an error of several dot clocks, depending on the input timings of the dot clock and horizontal sync signal pulses, the PLL lock status, and on the display signal pin output delay.
For fine adjustment of the actual display position, check it during actual operation.
 - Display is started usually at the set display position. When $\overline{\text{VSYNC}}$ or $\overline{\text{HSYNC}}$ is active, however, the display outputs (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) are masked.

3.2 Font ROM Configuration

The font ROM is configured 512 characters each made up of 24×32 dots.

- All of 512 characters can be set freely by the user.
(Note, however, that a blank character must be set as one of the characters.)
- The screen background character area and sprite character area are 000H to 0FFH.

Font ROM



3.3 Display Memory (VRAM) Configuration

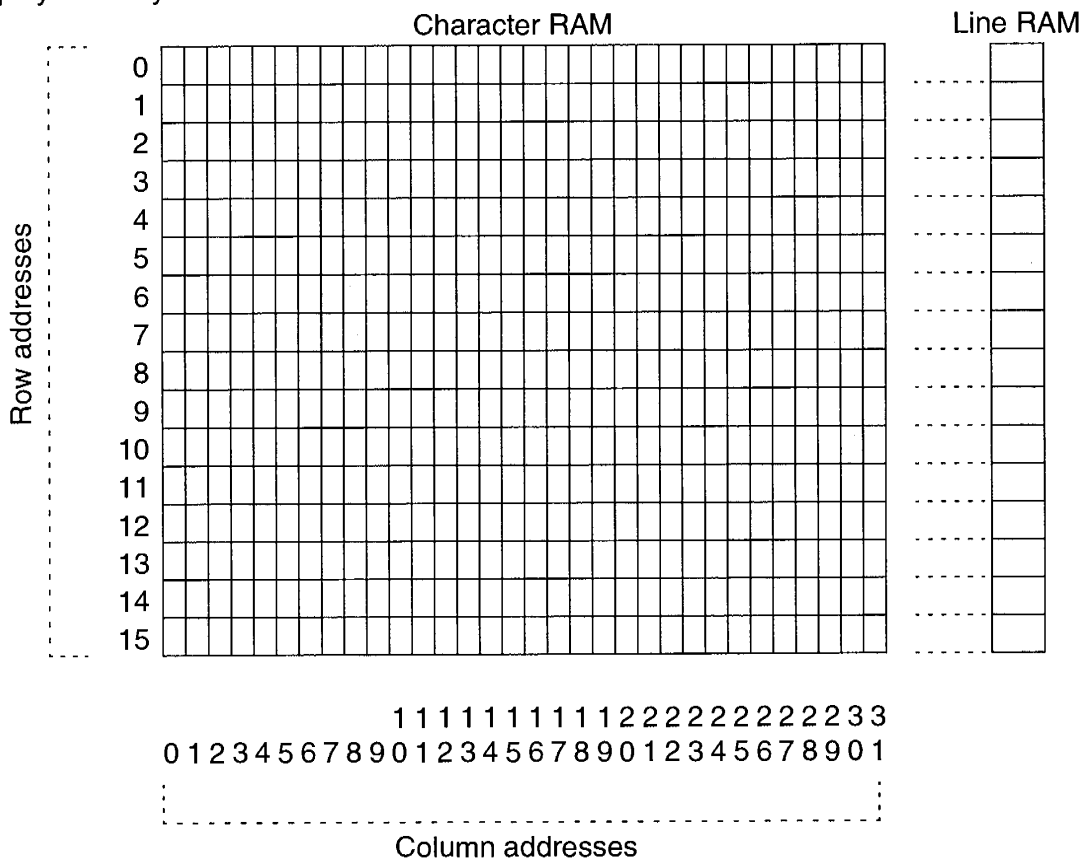
The display memory (VRAM) consists of the character RAM for setting individual characters and the line RAM for setting individual lines.

- Character RAM: 32 characters × 16 lines (512 characters in total)
- Line RAM: 16 lines

3.3.1 Display memory and display screen

Areas of character RAM and those of line RAM correspond to displayed characters and lines on a one-to-one basis, respectively.

○ Display memory

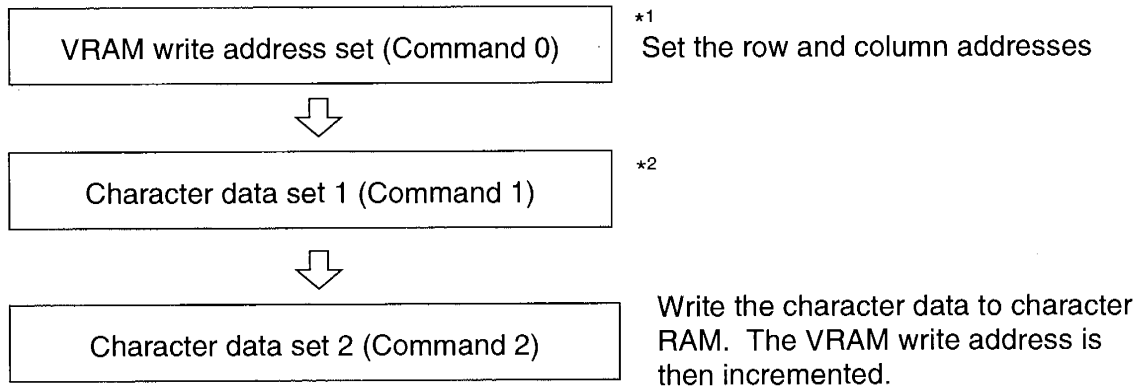


3.3.2 Writing to Display Memory

(1) Writing characters to character RAM

(1) Writing a single character

Use the following commands to write data on an arbitrary character to an arbitrary address in character RAM:

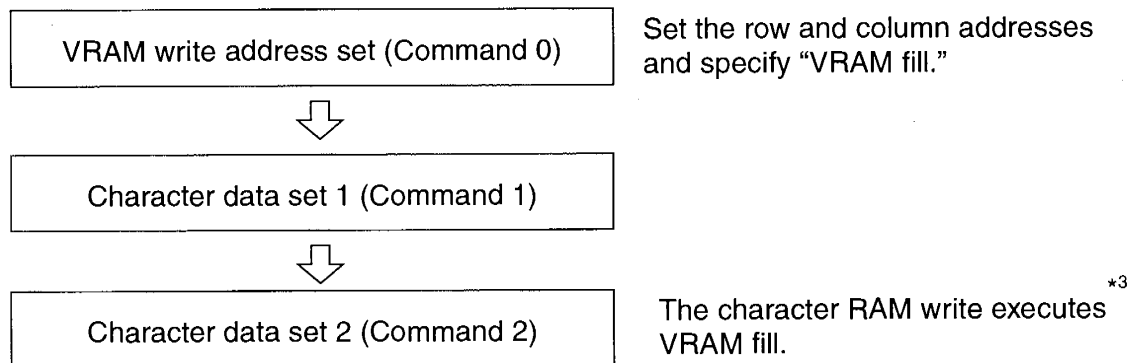


*1: When writing to consecutive addresses continuously, you can omit this command for the latter character RAM write.

*2: You can also omit this command if the current character data is the same as the one set by the preceding “character data set 1” command.

(2) Writing multiple characters collectively (VRAM fill)

Use the following commands to write data on an arbitrary character to an area of character RAM from an arbitrary address to the last address, filling the area with that data:



*3: During execution of VRAM fill, the TRE pin maintains High-level output.

The VRAM fill execution time depends on the dot clock frequency. The reference value for VRAM fill of an entire screen is as follows:

Dot clock 10 MHz: About 2 ms
Dot clock 20 MHz: About 1 ms
Dot clock 40 MHz: About 0.5 ms

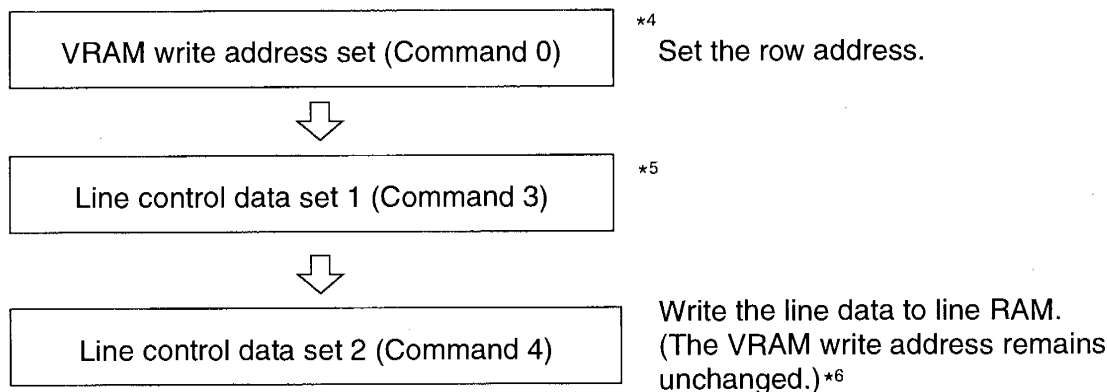
An attempt to issue commands 1 to 4 during execution of VRAM fill causes both the VRAM fill and the issuance of the commands to fail.

Issuing command 0 (FL = 0) during execution of VRAM fill aborts the VRAM fill.

To set a VRAM write address when VRAM fill has aborted, issue command 0 again to set the address.

(2) Writing to line RAM

Use the following commands to write data on an arbitrary line to an arbitrary address in line RAM:



*4: The line RAM fill function is not available. (It is prohibited to specify “Line RAM fill.”)

*5: You can omit this command if the current line control data is the same as the one set by the preceding “line control data set 1” command.

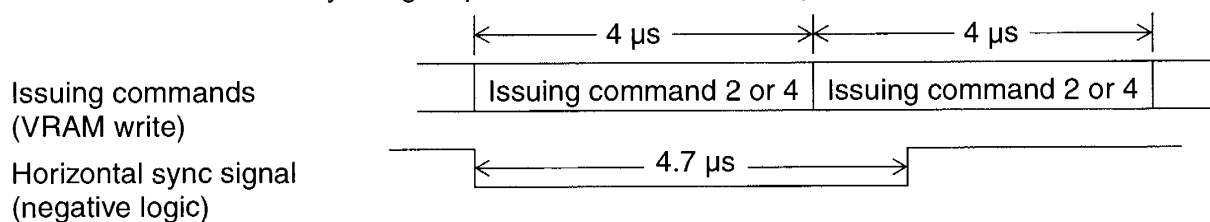
*6: Any line RAM write does not increment the VRAM write address. You must therefore set a line address for each line.

Note: • Normal writing to VRAM requires input of a standard horizontal sync signal. Input of an invalid horizontal sync signal may cause VRAM write to fail.

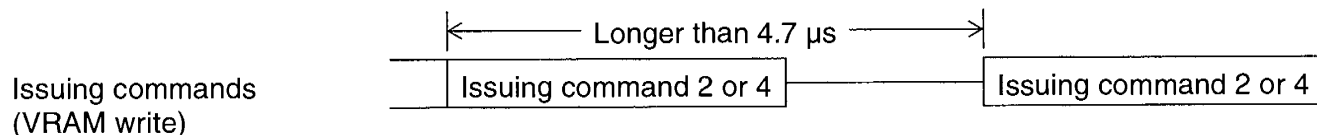
- Also, you must set the horizontal sync signal pulse width and VRAM write cycle (the interval between commands 2 and 4 to be issued) such that: horizontal sync signal pulse width < VRAM write cycle.

Example: Assuming the continuous writing with SCLK for serial transfer in 4 MHz

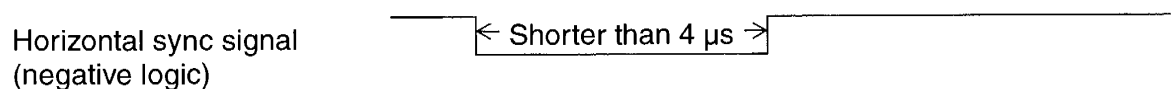
Write period into VRAM is $(1/4 \text{ MHz}) \times 16 [\text{cycle per command}] = 4\mu\text{s}$. Horizontal sync signal pulse width for normal NTSC is approx. $4.7\mu\text{s}$. Adjustment is required including the VRAM write period adjustment or making the horizontal sync signal pulse width to less than $4\mu\text{s}$.



■ Adjustment example 1. Setting the VRAM write cycle to longer than $4.7\mu\text{s}$



■ Adjustment example 2. Setting the horizontal sync signal pulse width to shorter than $4\mu\text{s}$



3.4 Text Display

3.4.1 Displayed character configuration

For each character to be displayed, you can set the vertical and horizontal sizes.

Each character is displayed by clipping the specified size of the specified character data from font ROM, starting at the upper leftmost dot.

- Character horizontal size control (Setting for each character)

Character data set 1 (Command 1): Bits MS1 and MS0

MS1	MS0	Character horizontal size
0	0	S size: 12 dots
0	1	M size: 18 dots*
1	0	L size: 24 dots
1	1	(Setting prohibited)

*: The M size cannot be specified for graphic characters.

- Line character vertical size type control (Setting for each line)

Line control data set 1 (Command 3): Bit LHS

LHS	Line character vertical size type
0	Character vertical size A
1	Character vertical size B

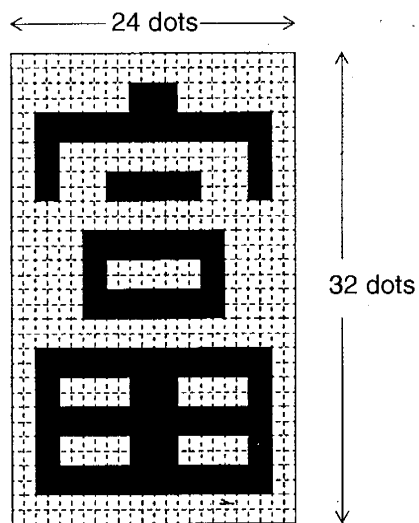
- Character vertical size A/B

Character vertical size control (Command 6-0): Bits HA2 to HA0/HB2 to HB0

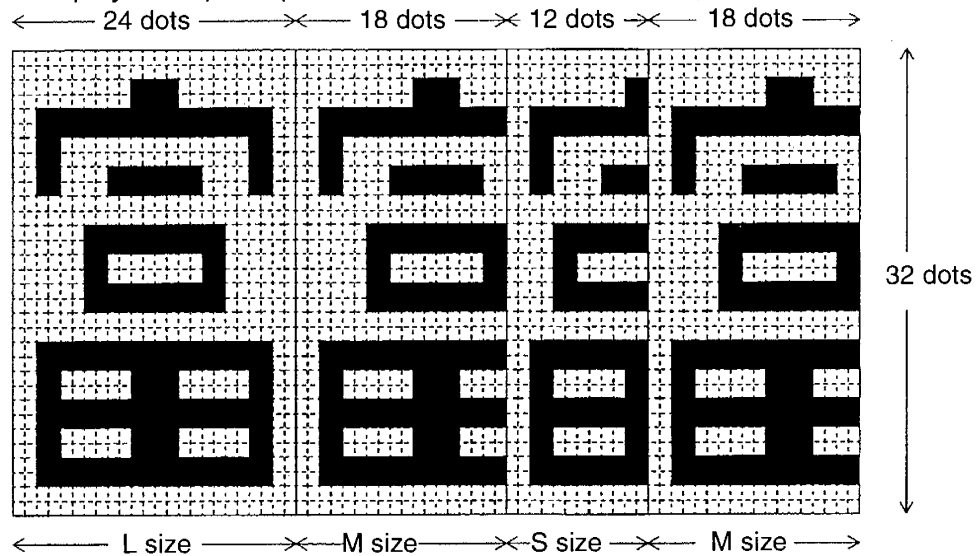
HA2/ HB2	HA1/ HB1	HA0/ HB0	Character vertical size A/B
0	0	0	18 dots
0	0	1	20 dots
0	1	0	22 dots
0	1	1	24 dots
1	0	0	26 dots
1	0	1	28 dots
1	1	0	30 dots
1	1	1	32 dots

● Display examples

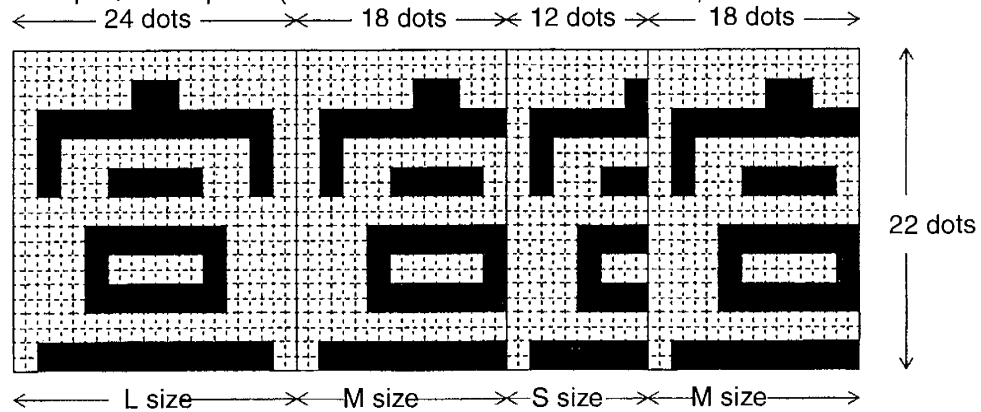
- A character stored in font ROM



- Display example 1 (vertical character size = 32 dots)

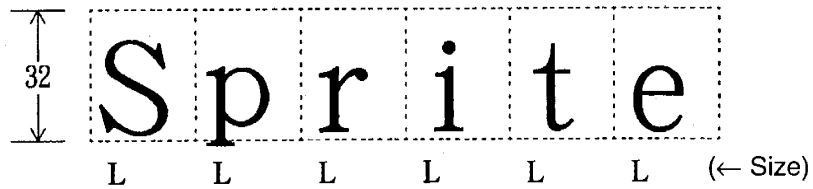


- Display example 2 (vertical character size = 22 dots)



- Applied display examples

- Example of displaying characters all in the L size



32

S p r i t e

L L L L L L (← Size)

- Example of displaying characters in the L, M, and S sizes



32

S p r i t e

L M M S S M (← Size)

- Example of displaying characters in the L/M/S horizontal sizes and variable vertical sizes



18

かんじ じ しょ

32

漢字辞書

32

A B C D E

18

a b c d e

3.4.2 Character colors

- Character colors (Setting for each character, selected from among 16 colors)

Character data set 1 (Command 1): Bits MC3 to MC0

Character color				Character color signal output			
MC3	MC2	MC1	MC0	IOUT pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

Note: The above table assumes display color signal output logic control (command 13-0) with DCX = 0.

3.4.3 Character trimming

(1) Trimming output control

Trimming output control turns on or off the trimming of characters depending on their character background type.

One of the four character background types can be set for each line.

- Trimming output control (Setting for each line)

Line control data set 1 (Command 3): Bits LFD and LFC

Trimming output control (Setting for each line)		Character background type (Setting for each character)			Trimming output
LFD	LFC	MM1	MM0	Background display	
0	0	0	0	Undisplay	×
		0	1	Solid background	×
		1	0	Concaved, shaded background	×
		1	1	Convexed, shaded background	×
0	1	0	0	Undisplay	○
		0	1	Solid background	×
		1	0	Concaved, shaded background	×
		1	1	Convexed, shaded background	×
1	0	0	0	Undisplay	○
		0	1	Solid background	○
		1	0	Concaved, shaded background	×
		1	1	Convexed, shaded background	×
1	1	0	0	Undisplay	○
		0	1	Solid background	○
		1	0	Concaved, shaded background	○
		1	1	Convexed, shaded background	○

×: Off*

○: On

*: The display is “no pattern background” in pattern background 1 or 2 mode.

(2) Trimming type control

Trimming display is controlled by selecting the combination of one of the four trimming types set for each screen and one of the four trimming outputs set for each line.

- Trimming type control (Setting for each screen)

Screen output control 2 (Command 5-1): Bits FM1 and FM0

Trimming type control		Trimming type
FM1	FM0	
0	0	1-dot horizontal trimming
0	1	2-dot horizontal trimming
1	0	Pattern background 1
1	1	Pattern background 2

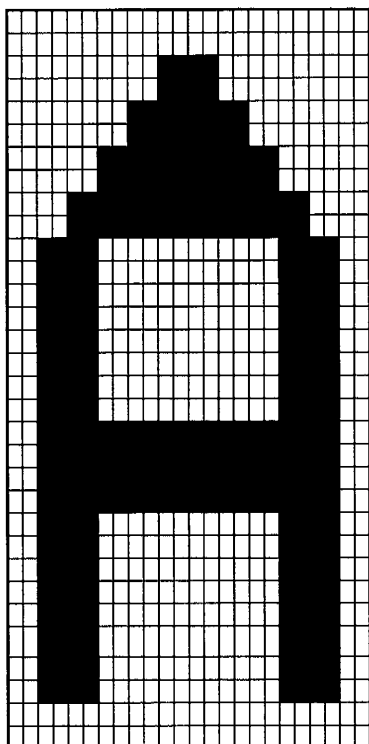
- Trimming control (Setting for each line)

Line control data set 1 (Command 3): Bits LFB and LFA

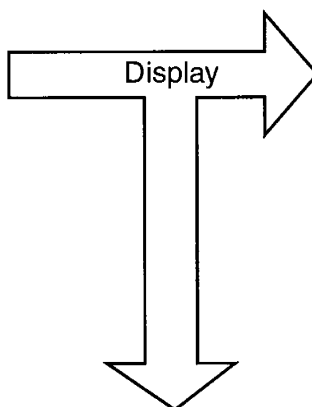
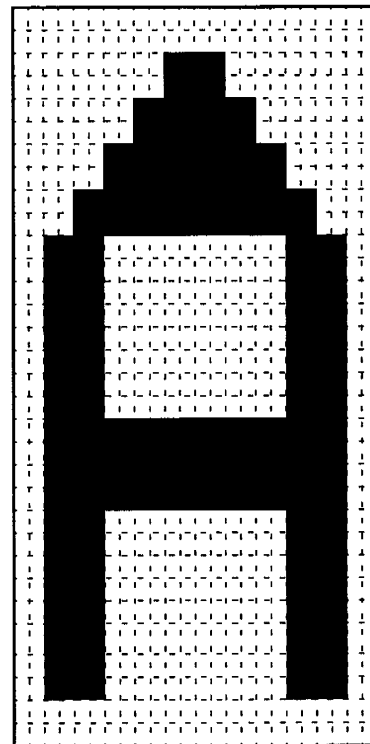
Trimming control		Trimming output
LFB	LFA	
0	0	Undisplay
0	1	Right trimming
1	0	Left trimming
1	1	Both-side trimming

- Display example of single-dot horizontal trimming (FM1, FM0 = 0, 0)

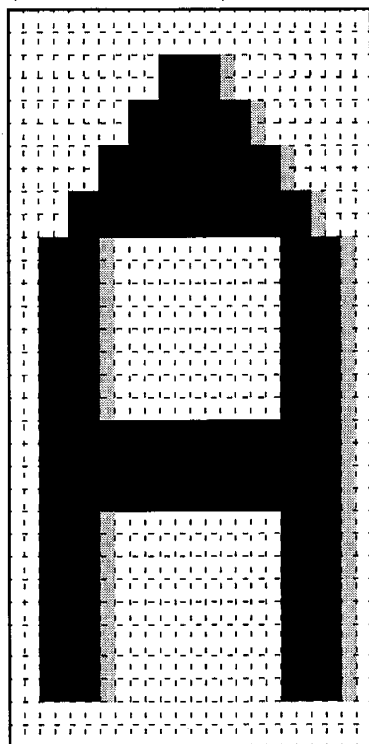
Font ROM (original image data)



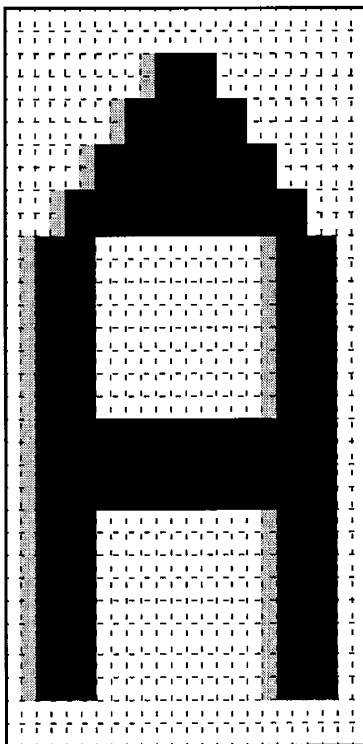
No trimming (LFB, LFA = 0, 0)



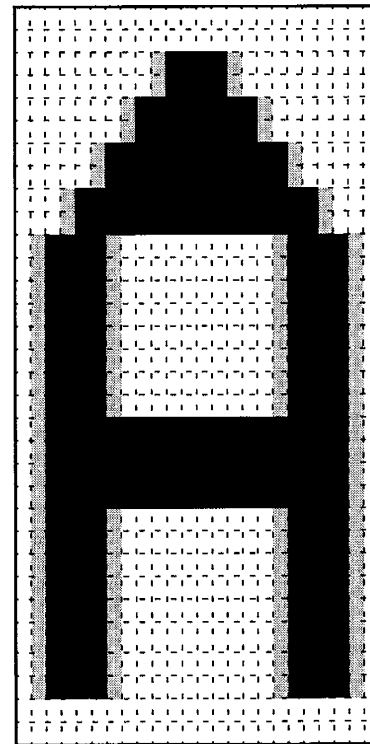
Right trimming
(LFB, LFA = 0, 1)



Left trimming
(LFB, LFA = 1, 0)

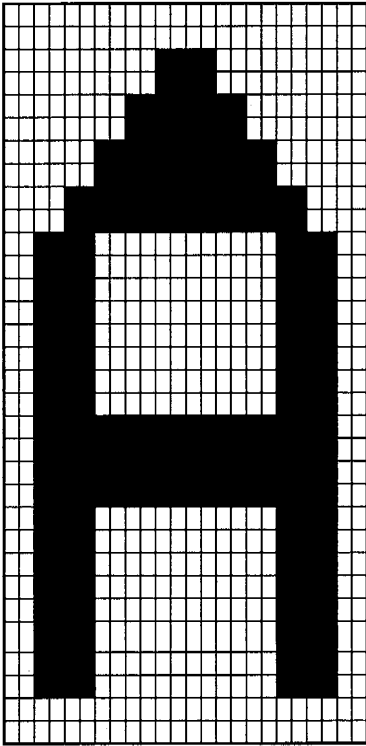


Both-side trimming
(LFB, LFA = 1, 1)

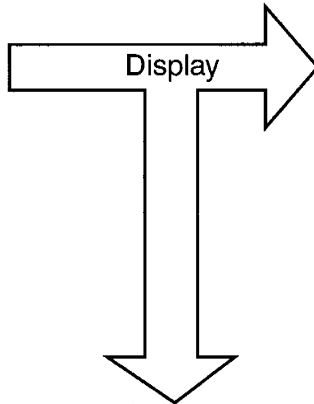
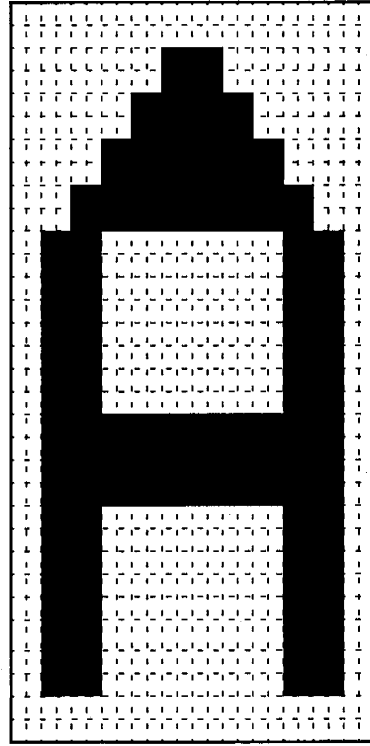


■ Display example of double-dot horizontal trimming (FM1, FM0 = 0, 1)

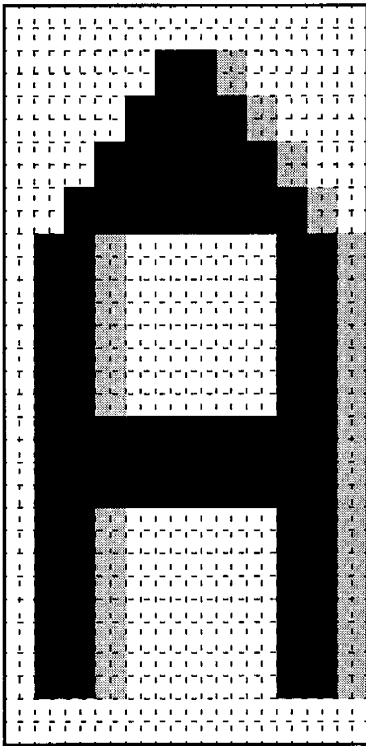
Font ROM (original image data)



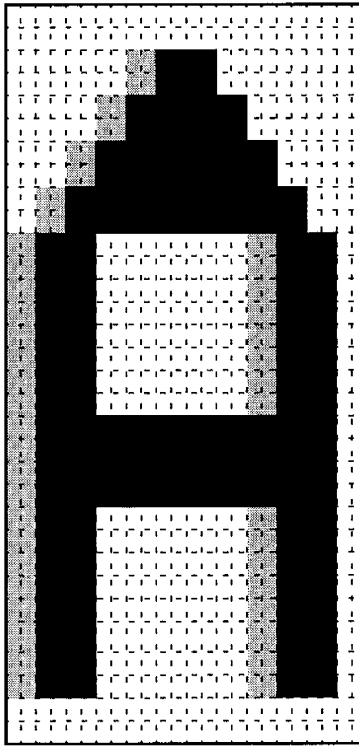
No trimming (LFB, LFA = 0, 0)



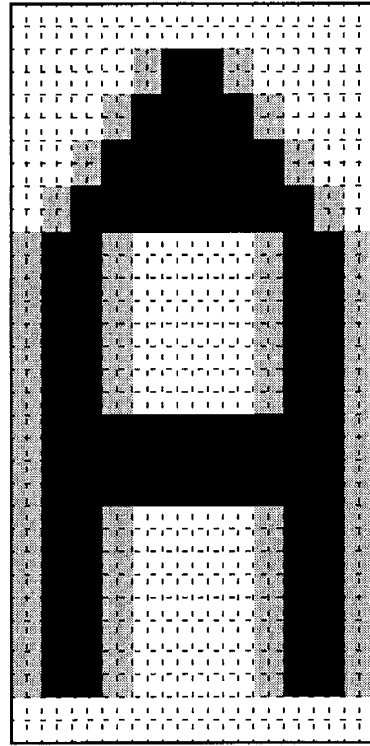
Right trimming
(LFB, LFA = 0, 1)



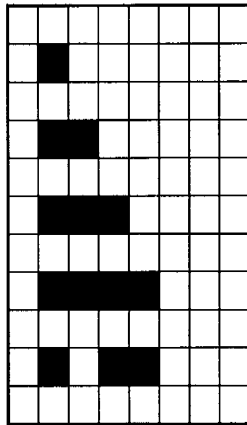
Left trimming
(LFB, LFA = 1, 0)



Both-side trimming
(LFB, LFA = 1, 1)

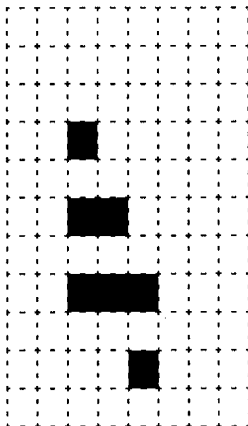


Font ROM (original image data)

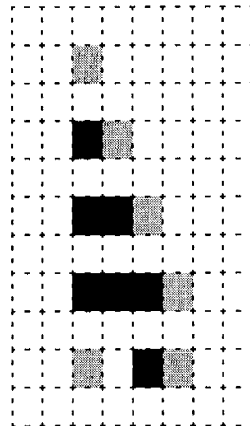


■ Display example of pattern background 1 (FM1, FM0 = 1, 0)

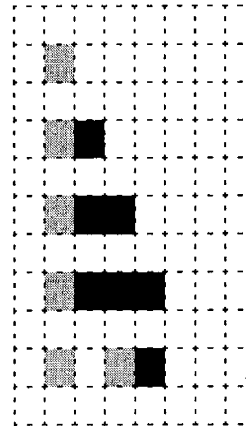
No pattern background
(LFB, LFA = 0, 0)



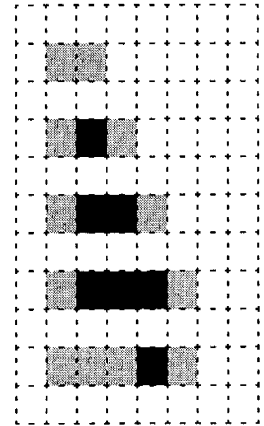
Right pattern background
(LFB, LFA = 0, 1)



Left pattern background
(LFB, LFA = 1, 0)

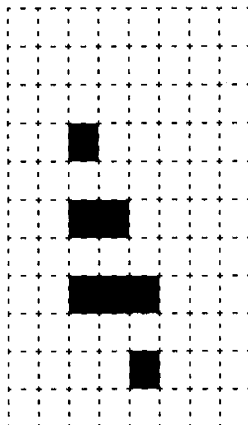


Both-side pattern background
(LFB, LFA = 1, 1)

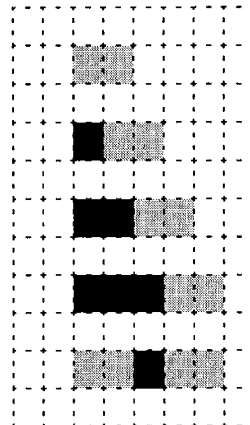


■ Display example of pattern background 2 (FM1, FM0 = 1, 1)

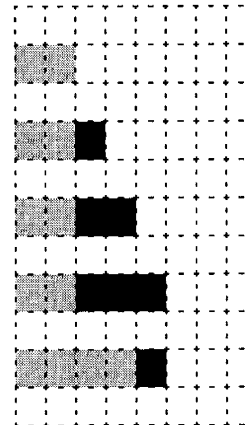
No pattern background
(LFB, LFA = 0, 0)



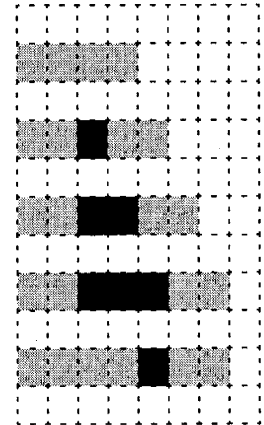
Right pattern background
(LFB, LFA = 0, 1)



Left pattern background
(LFB, LFA = 1, 0)



Both-side pattern background
(LFB, LFA = 1, 1)



(3) Trimming colors

- Trimming colors (Setting for each line, selected from among 16 colors)
Line control data set 1 (Command 3): Bits LF3 to LF0

Character trimming color				Character color trimming signal output			
LF3	LF2	LF1	LF0	IOUT pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

Note: The above table assumes display color signal output logic control (command 13-0) with DCX = 0.

(4) Trimming display rules

- Trimming dots for a character can be displayed in the right-side or left-side adjacent character area only when the character background types of the two characters are the same.
- Trimming dots for the character at the left or right end of a line can be displayed beyond the character area only when the character background type is “no character background.”
- Trimming dots on a line are enlarged when the line is displayed enlarged.

3.4.4 Line enlarged display

Line enlarged display control controls the display size of each line including the characters, character backgrounds, and line background on that line (as well as the line spacing portions). This also controls enlargement of the shadow frames of shaded backgrounds and trimming dots. Note that the lines following the line for which line enlarged display has been specified are shifted down accordingly.

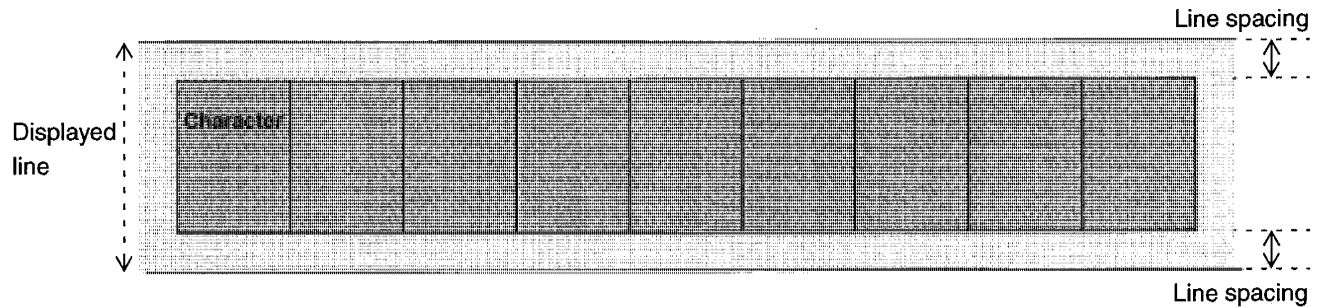
- Line enlargement control (Setting for each line)

Line control data set 2 (Command 4): Bits LG1 and LG0

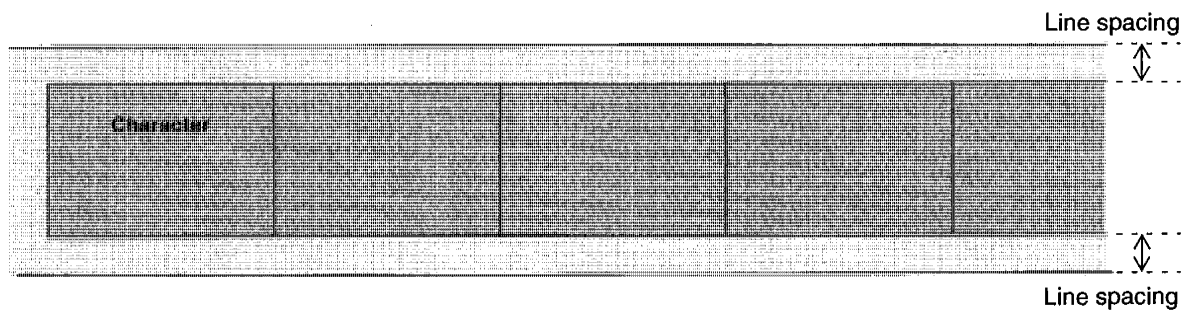
LG1	LG0	Display size
0	0	Normal size
0	1	Double-width size
1	0	Double-height size
1	1	Double-width/height size

(1) Line enlarged display examples

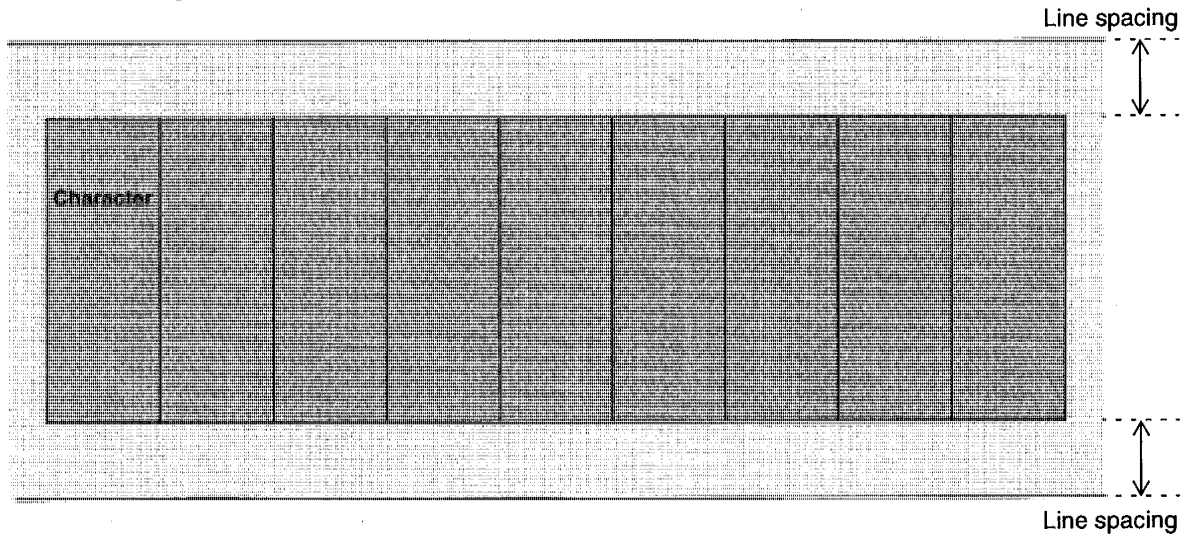
- Normal size



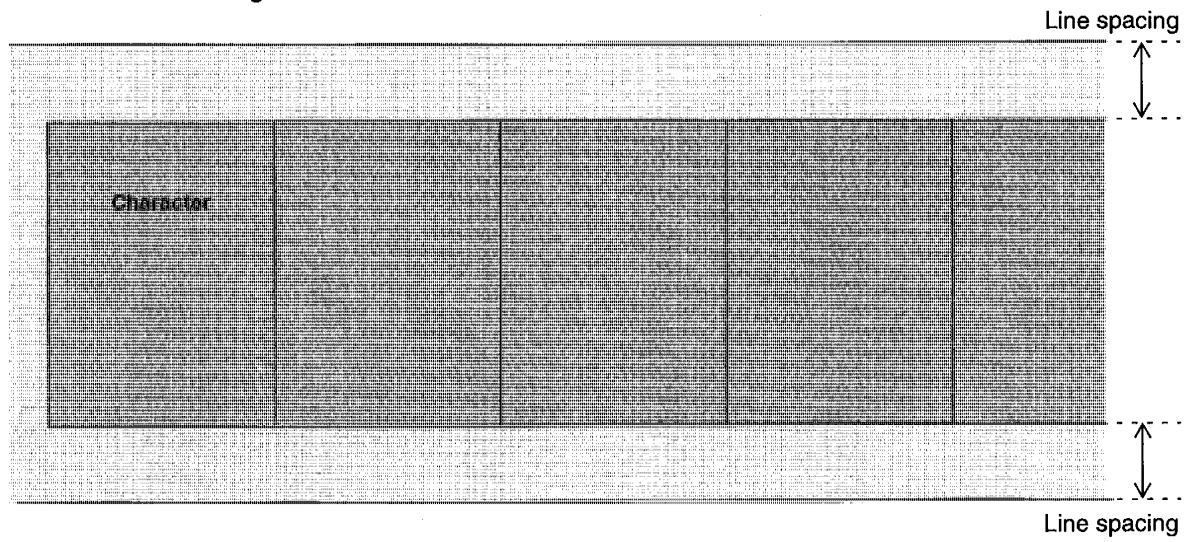
- Double-width size



- Double-height size



- Double-width/height size



3.4.5 Graphic character control

Graphic character control allows graphic display to be set. Although the resolution of graphic characters is half that of normal characters both horizontally and vertically, graphic characters can be colored in 16 colors dot by dot.

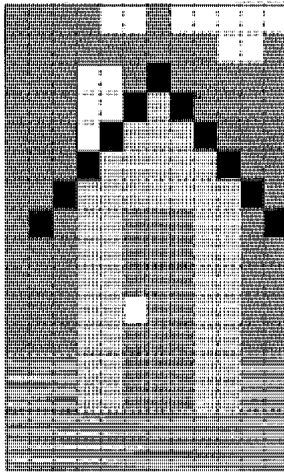
- Character/graphic character control (Setting for each character)

Character data set 2 (Command 2): Bit MG

MG	Character/graphic character control
0	Normal character
1	Graphic character

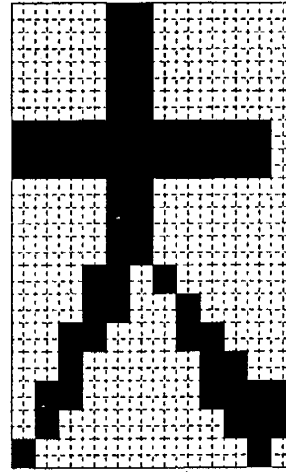
Note that the M size cannot be specified for graphic characters.

Graphic display example

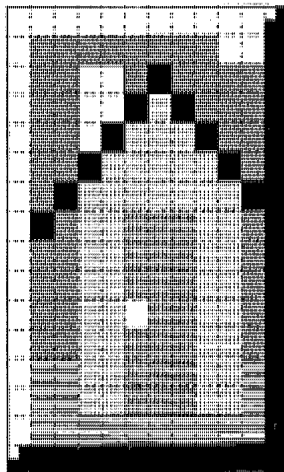
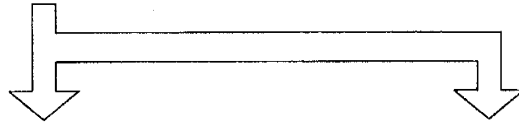


(MG=1)

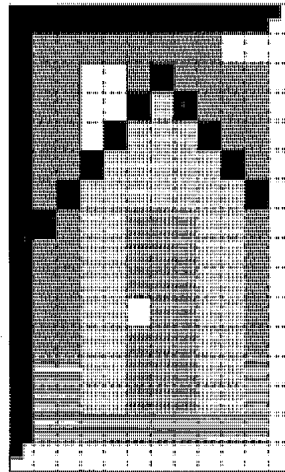
Normal character display example



(MG=0)



(MM1=1, MM0=1)



(MM1=1, MM0=0)

[Shaded background display is enabled even for graphic characters.]

- Graphic color/trimming color replace control (Setting for each screen)

Graphic color control (Command 6-3): Bit GF

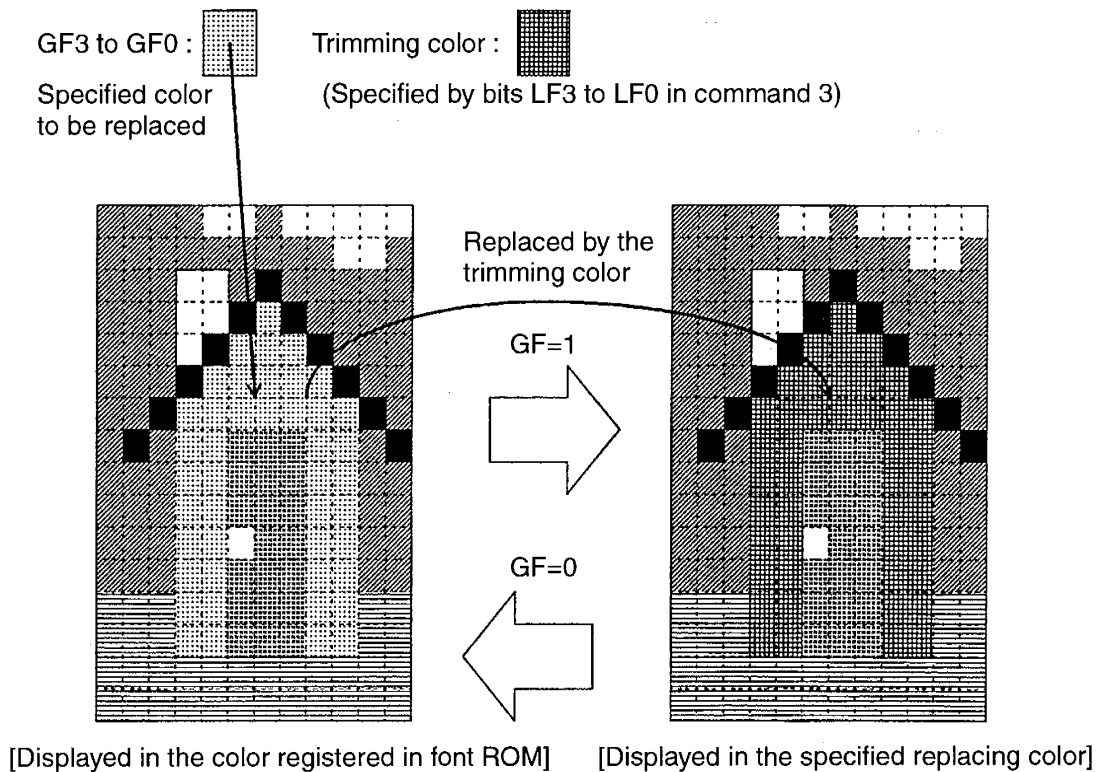
Usually, each dot of a graphic character is displayed in the color registered in font ROM. You can however replace an arbitrary graphic color by a different color on the screen by setting bit GF to 1 and resetting the color set by bits GF3 to GF0 to the character trimming color specified in command 3 (bits LF3 to LF0) as the replacing color.

GF	Graphic color/trimming color replace control
0	Prevent the specified color from being replaced.
1	Replace the specified color by the trimming color.

- Code of the color to be replaced by the trimming color (Setting for each screen)

Graphic color control (Command 6-3): Bits GF3 to GF0

■ Example of color replacement



- Graphic color/character color replace control (Setting for each screen)

Graphic color control (Command 6-3): Bit GC

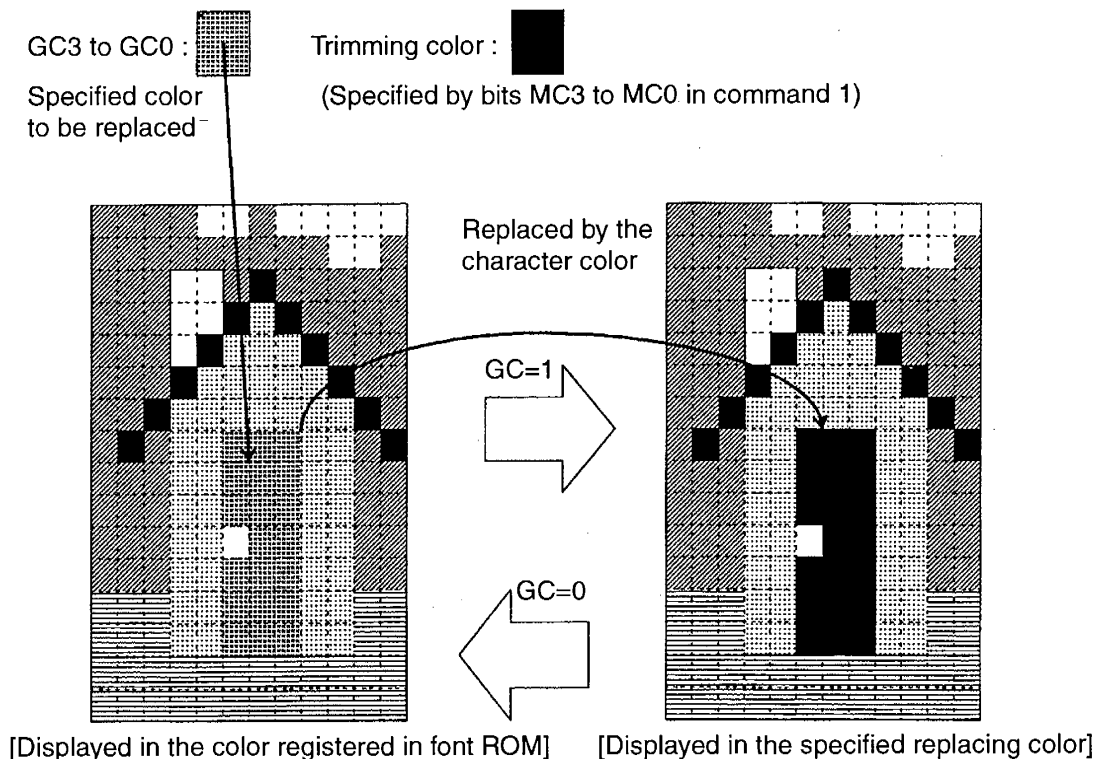
Usually, each dot of a graphic character is displayed in the color registered in font ROM. You can however replace an arbitrary graphic color by a different color on the screen by setting bit GC to 1 and resetting the color set by bits GC3 to GC0 to the character color specified in command 1 (bits MC3 to MC0) as the replacing color.

GC	Graphic color/character color replace control
0	Prevent the specified color from being replaced.
1	Replace the specified color by the character color.

- Code of the color to be replaced by the character color (Setting for each screen)

Graphic color control (Command 6-3): Bits GC3 to GC0

■ Example of color replacement



Tip: If you set the character background of a graphic character to "solid-filled," the transparent-color dots can be displayed in the character background color instead.

3.4.6 Blink control

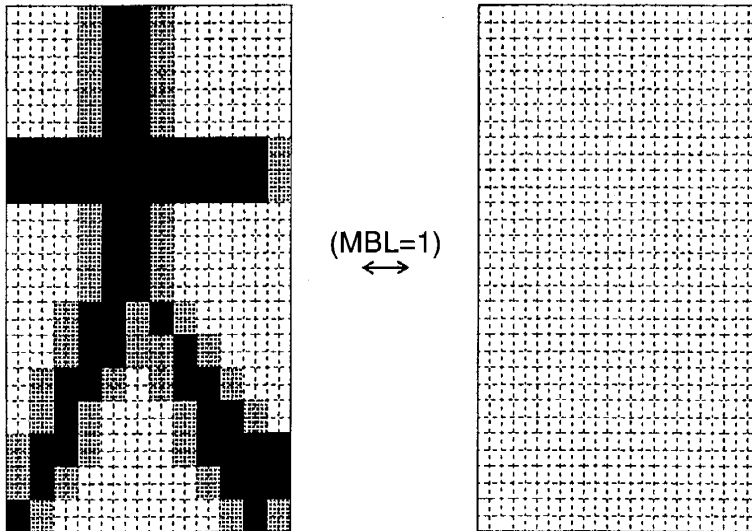
Blink control can turn on or off blinking of each character.

- Blink control (Setting for each character)

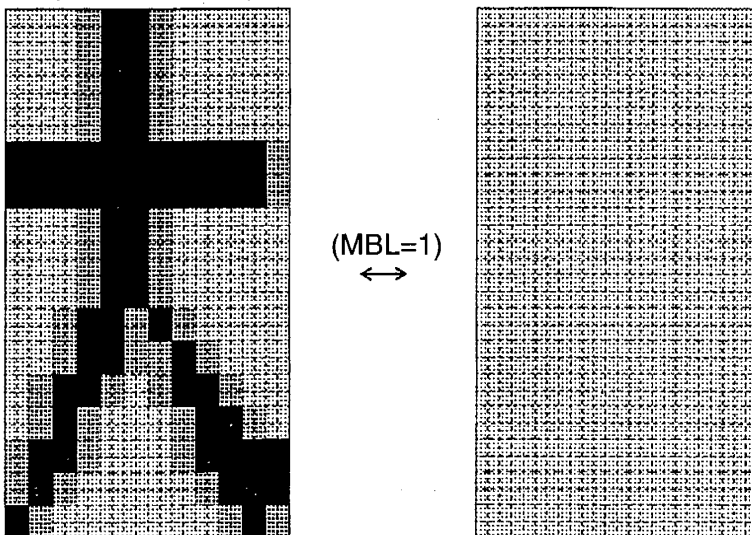
Character data set 2 (Command 2): Bit MBL

MBL	Blink control
0	Blink OFF (Normal display)
1	Blink ON

- Example of a blinking character with no background (MM1, MM0 = 0, 0)

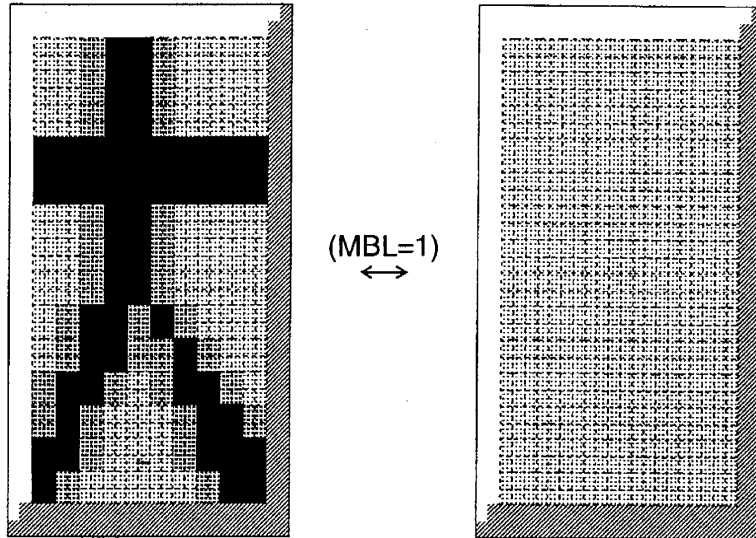


- Example of a blinking character with a solid-filled background (MM1, MM0 = 0, 1)



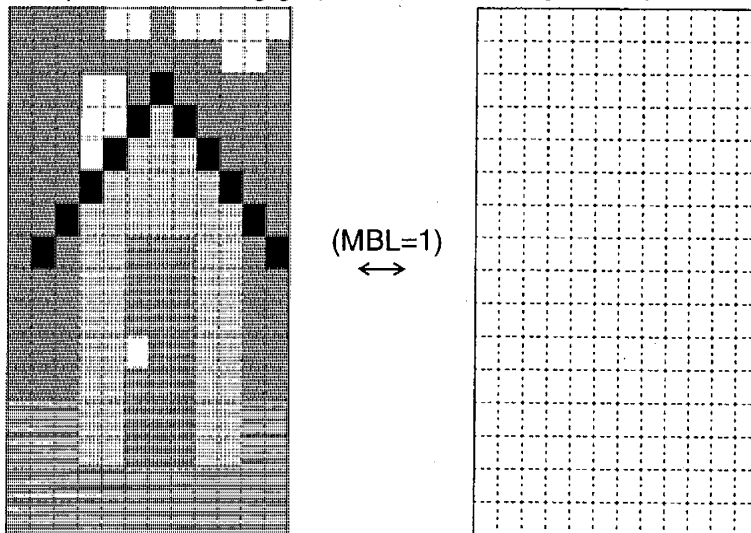
[The solid-filled background remains displayed even when the character itself comes out during blinking.]

- Example of a blinking character with a shaded background (MM1, MM0 = 1, 1)



[The solid-filled background remains displayed even when the character itself comes out during blinking.]

- Example of a blinking graphic with no background (MM1, MM0 = 0, 0)



The blink cycle and duty ratio can be set.

- Blink cycle control (Setting for each screen)

Screen output control 2 (Command 5-1): Bits BT1 and BT0

BT1	BT0	Blink cycle
0	0	16 × VSYNC
0	1	32 × VSYNC
1	0	48 × VSYNC
1	1	64 × VSYNC

- Blink duty ratio control (Setting for each screen)

Screen output control 2 (Command 5-1): Bits BD1 and BD0

BD1	BD0	(On:Off) Blink duty ratio
0	0	1:0 (Always on)
0	1	1:1
1	0	1:3
1	1	3:1

3.4.7 Transparent/translucent color control

- Transparent color control (Setting for each screen)

Transparent/translucent color control (Command 6-2): Bit TC

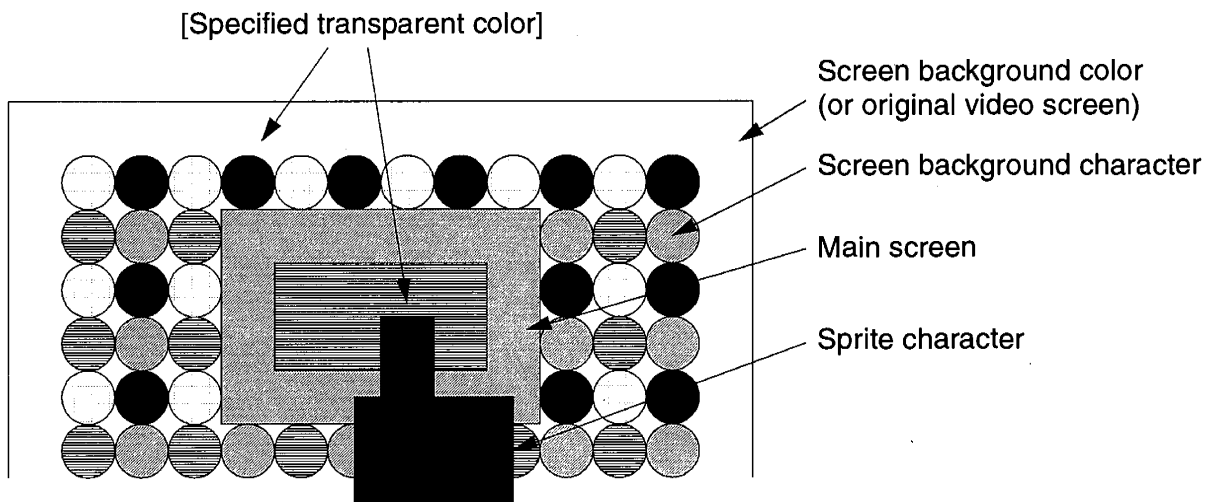
Normally, each screen is displayed while masking the lower screens (layers). Bit TC allows the areas in one (specified in TC3 to TC0) of 16 colors to be displayed transparent (where the screen on the lower layer are visible).

TC	Transparent color control
0	Disable transparent color control.
1	Enable transparent color control.

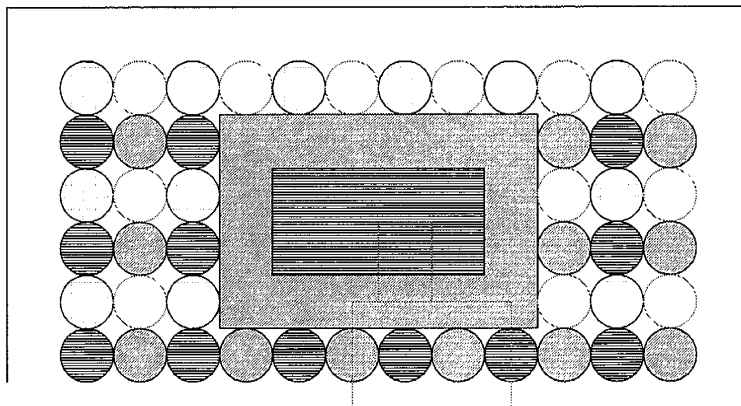
- Transparent color code (Setting for each screen)

Transparent/translucent color control (Command 6-2): Bits TC3 to TC0

- Example of setting a transparent color (Setting the color of ■ areas below as a transparent color)



↓TC=1 TC3-TC0 : ■ (Specified transparent color) ↑TC=1



- Translucent color control (Setting for each screen)

Transparent/translucent color control (Command 6-2): Bit HC

Like bit TC for transparent color control, bit HC allows the areas in one (specified in HC3 to HC0) of 16 colors to be displayed translucent. In addition, the VOB2 pin outputs the translucent color display period signal at the same timing.

Note1: The VOB2 pin output signal assumes translucent color processing using an external circuit.

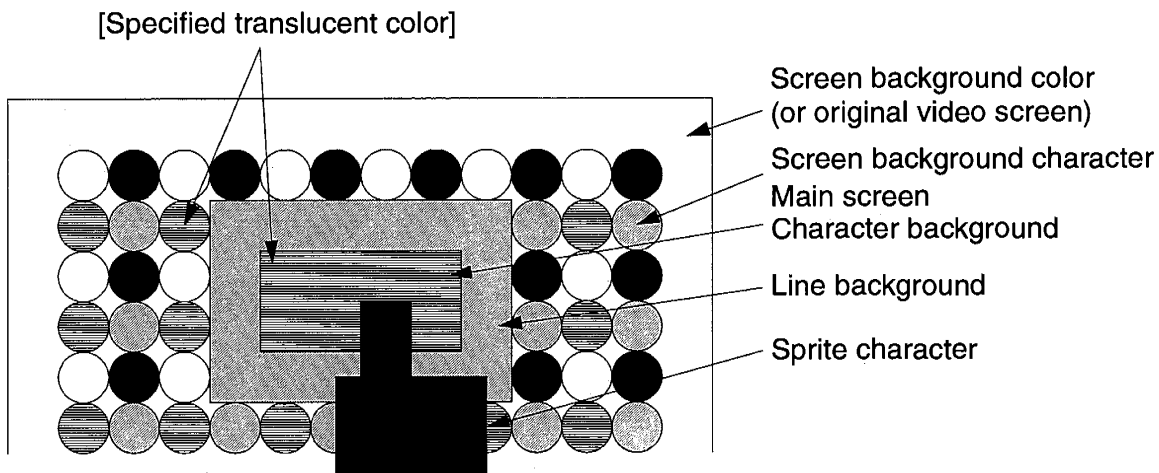
Note2: The translucent color display period signal is output for areas other than characters, trimming, and graphics.

TC	Translucent color control
0	Disable translucent color control.
1	Enable translucent color control.

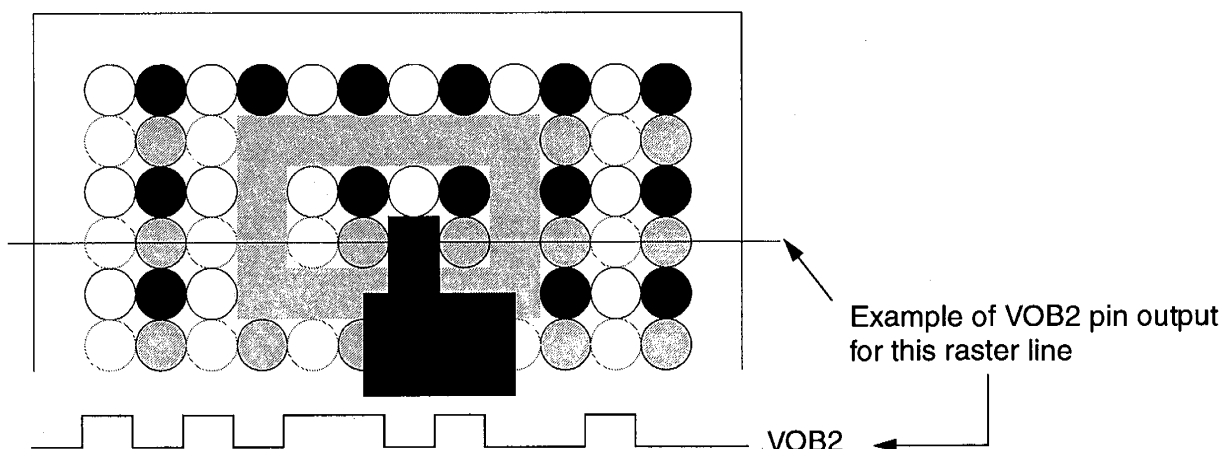
- Translucent color code (Setting for each screen)

Transparent/translucent color control (Command 6-2): Bits HC3 to HC0

- Example of setting a translucent color (Setting the color of ■ areas below as a translucent color)



↓HC=1 HC3-HC0 : ■ (Specified translucent color) ↑HC=1



3.5 Character Background Display

3.5.1 Character background display

- Character background control (Setting for each character)

Character data set 1 (Command 1): Bits MM1 and MM0

MM1	MM0	Character background
0	0	No background (undisplay)
0	1	Solid-filled background
1	0	Concaved, shaded background
1	1	Convexed, shaded background

- Shaded background highlight color (Setting for each screen, selected from among 16 colors)

Shaded background frame color control (Command 6-1): Bits BH3 to BH0

Shaded background highlight color				Shaded background highlight color signal output			
BH3	BH2	BH1	BH0	IOUT pin	GOUT pin	ROUT pin	BOUT pin
—	—	—	0	—	—	—	Low
—	—	0	—	—	—	Low	—
—	0	—	—	—	Low	—	—
0	—	—	—	Low	—	—	—
—	—	—	1	—	—	—	High
—	—	1	—	—	—	High	—
—	1	—	—	—	High	—	—
1	—	—	—	High	—	—	—

- Shaded background shadow color (Setting for each screen, selected from among 16 colors)

Shaded background frame color control (Command 6-1): Bits BS3 to BS0

Screen background color				Screen background color signal output			
BS3	BS2	BS1	BS0	IOU pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

- Character background color (Setting for each character, selected from among 16 colors)

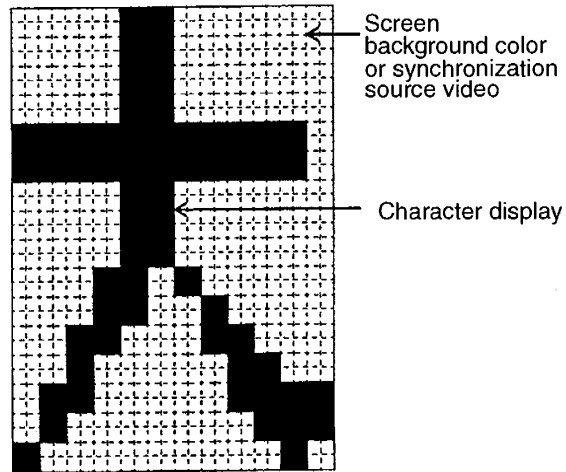
Character data set 1 (Command 1): Bits MB3 to MB0

Character background color				Character background color signal output			
MB3	MB2	MB1	MB0	IOU pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

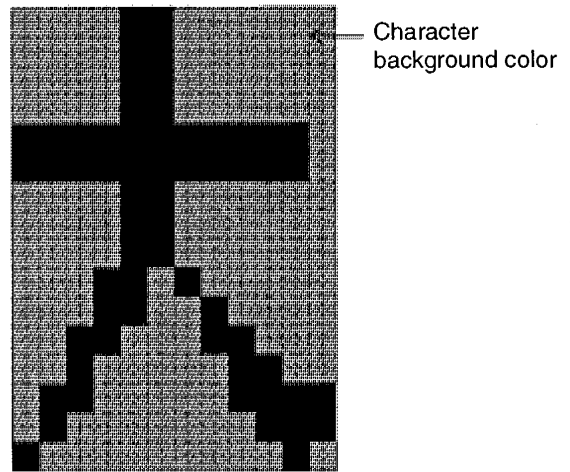
Note: The above table assumes display color signal output logic control (command 13-0) with DCX = 0.

- Display examples

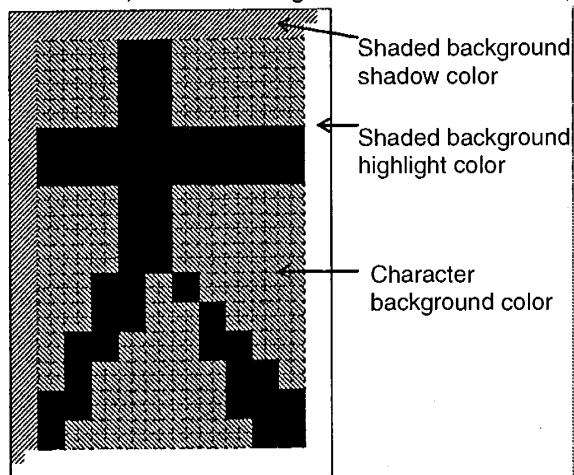
1) No background



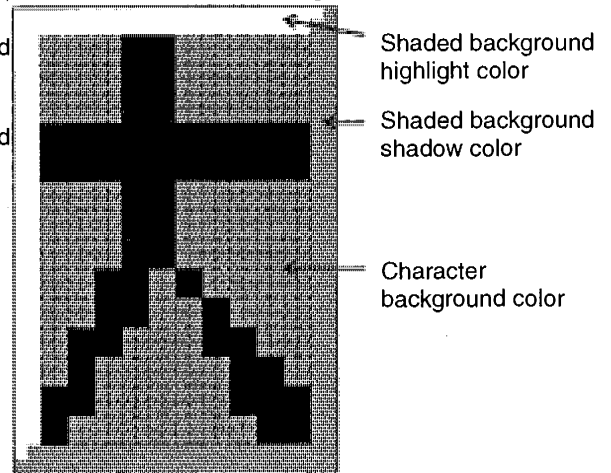
2) Solid-filled background



3) Concaved, shaded background



4) Convexed, shaded background



[The shaded background frame for a character is displayed inside the circumference of the character area.]

3.5.2 Shaded background succeeding character merge display

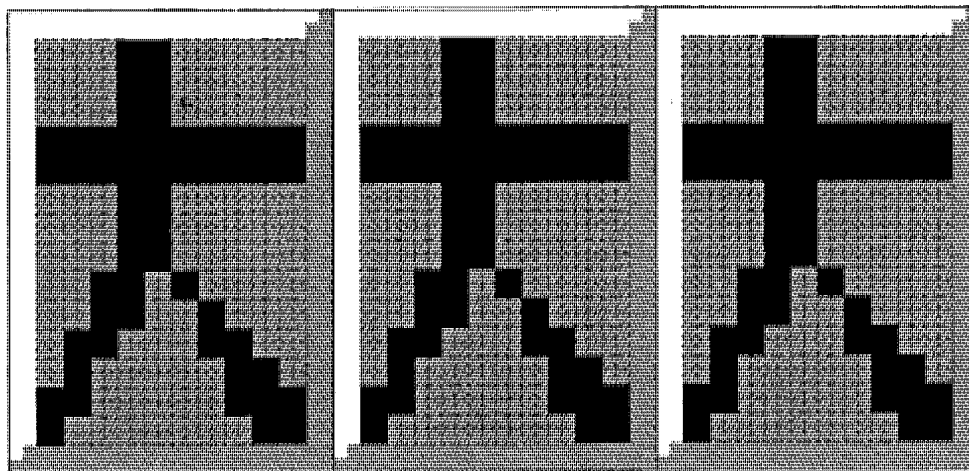
Specifying “shaded background succeeding character merge display” for a character undisplay the right line of the shadow frame of the character and the left line of the shadow frame of the next character. This enables two or more characters with shaded backgrounds to be joined horizontally.

- Shaded background succeeding character merge control (Setting for each character)

Character data set 2 (Command 2): Bit MR

MR	Shaded background succeeding character merge control
0	OFF
1	ON

- Display examples of independent characters with shaded backgrounds

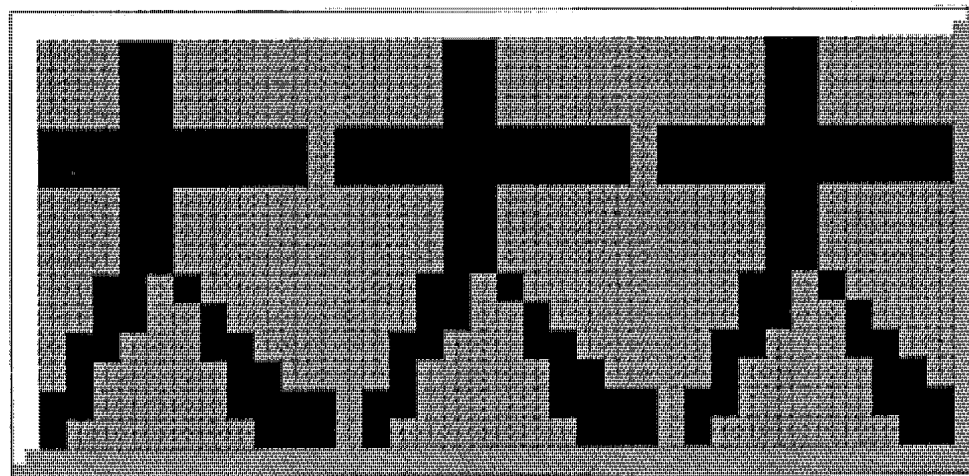


(Succeeding character merge = OFF)

(Succeeding character merge = OFF)

(Succeeding character merge = OFF)

- Display examples of merged characters with shaded backgrounds



(Succeeding character merge = ON)
(No character background)

(Succeeding character merge = ON)
(Solid-filled background)

(Succeeding character merge = OFF)
(Convexed, shaded background)

3.5.3 Shaded background succeeding line merge display

Specifying both of “shaded background succeeding line merge display” and “character background extended display” for a line undisplay the lower lines of the shadow frames of the characters on that line and the upper lines of the shadow frames of the characters on the next line.

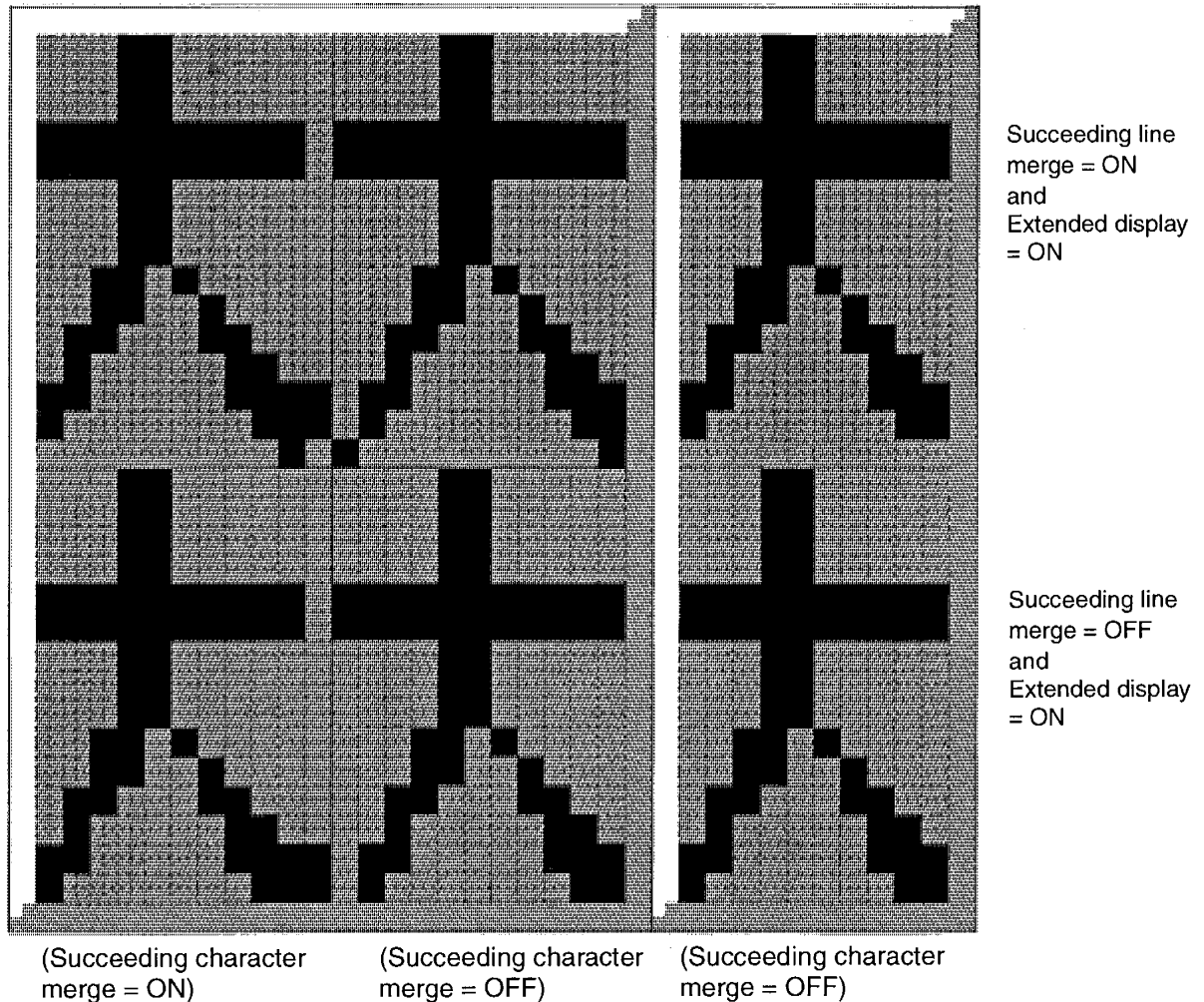
This enables two or more lines of characters with shaded backgrounds to be joined vertically.

- Shaded background succeeding line merge control (Setting for each line)

Line control data set 2 (Command 4): Bit LD

LD	Shaded background succeeding line merge control
0	OFF
1	ON

- Display examples of merged lines of characters with shaded backgrounds



Note: If character background extended display is not specified, shaded background succeeding line merge display is disabled for character backgrounds.

3.5.4 Character background extended display

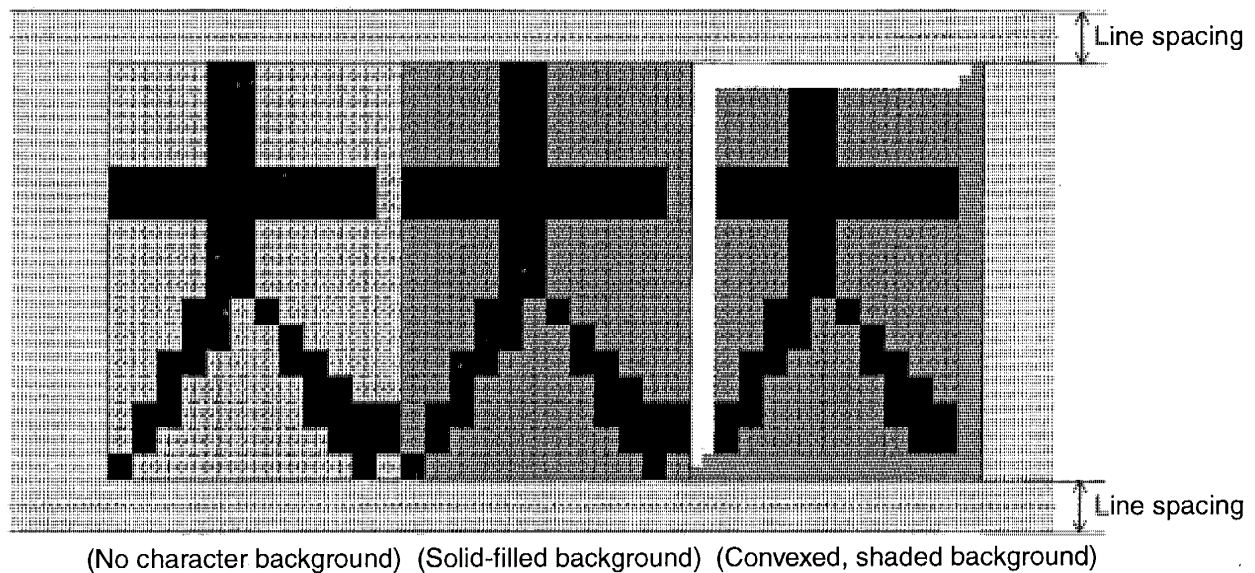
Character background extended display extends character backgrounds to line spacing portions.
(Note that this setting is required to apply shaded background succeeding line merge display to character backgrounds.)

- Character background extended display (Setting for each line)

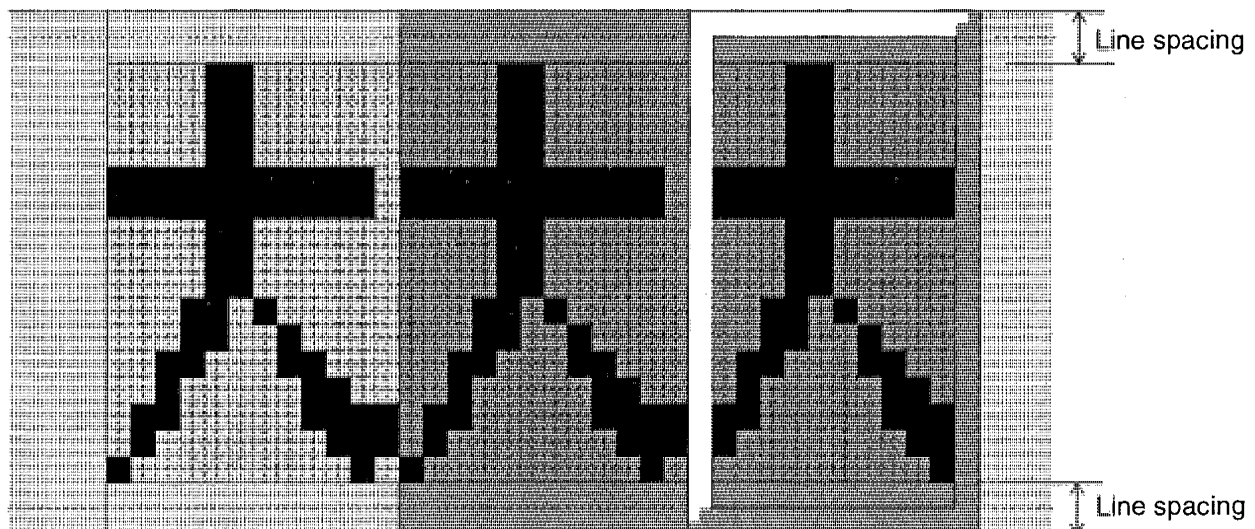
Line control data set 2 (Command 4): Bit LE

LE	Character background extended display
0	OFF (Normal display)
1	ON (Extended display)

- Display example with character background extended display = OFF



- Display example with character background extended display = ON



3.6 Line Background Display

3.6.1 Line background display

The background of a line is displayed in the line area of the characters on the line, the areas to the right and left of the area, and the line spacing areas above and below it.

- Line background control (Setting for each line)

Line control data set 2 (Command 4): Bits LM1 and LM0

LM1	LM0	Line background
0	0	No background (undisplay)
0	1	Solid-filled background
1	0	Concaved, shaded background
1	1	Convexed, shaded background

- Line background color (Setting for each line, selected from among 16 colors)

Line control data set 2 (Command 4): Bits L3 to L0

Line background color				Line background color signal output			
L3	L2	L1	L0	IOUT pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

Note: The above table assumes display color signal output logic control (command 13-0) with DCX = 0.

- Shaded background highlight color (Setting for each screen, selected from among 16 colors)

Shaded background frame color control (Command 6-1): Bits BH3 to BH0

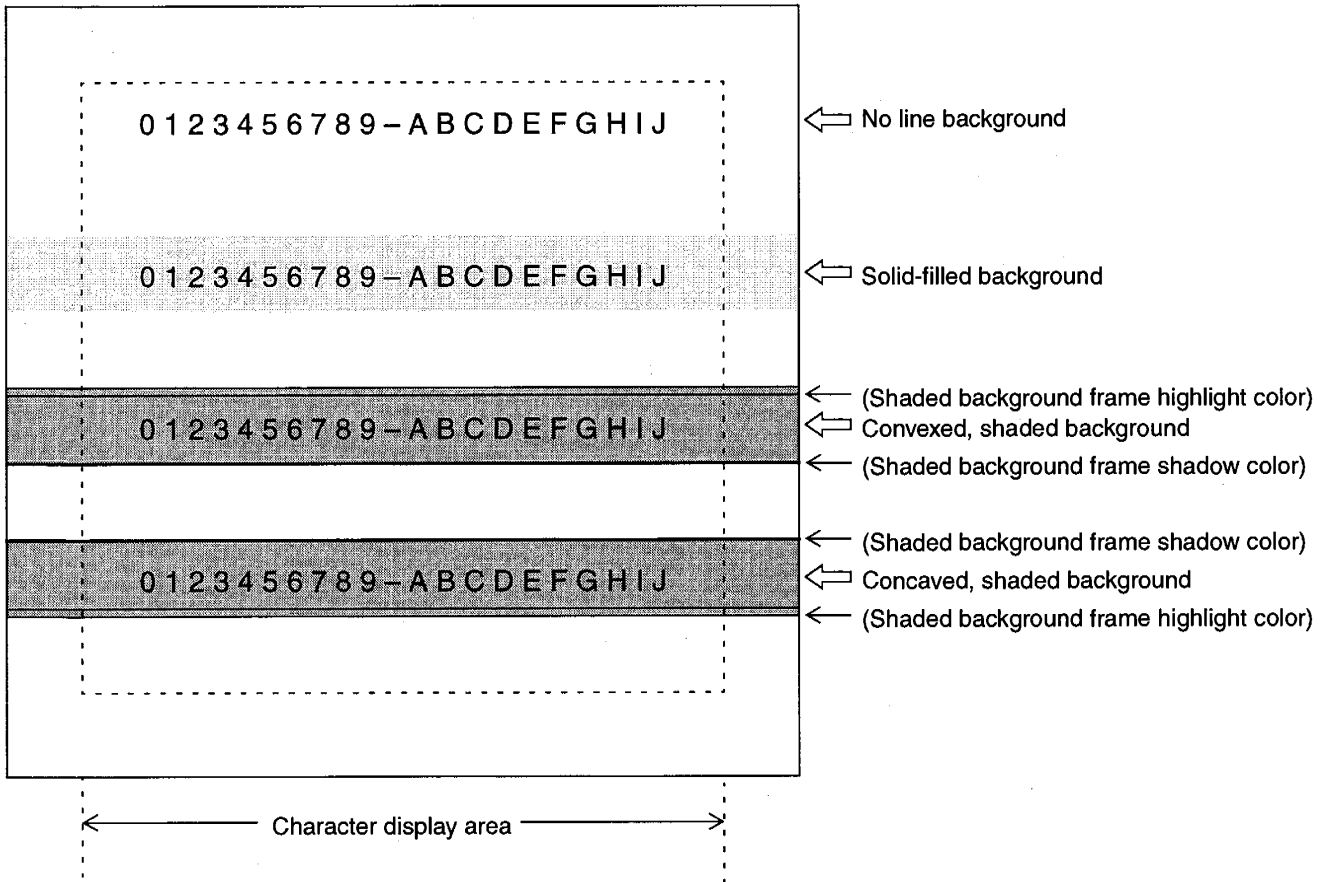
Note: Used also for shaded character background display.

- Shaded background shadow color (Setting for each screen, selected from among 16 colors)

Shaded background frame color control (Command 6-1): Bits BS3 to BS0

Note: Used also for shaded character background display.

- Line background display examples



3.6.2 Shaded background succeeding line merge display

Specifying “shaded background succeeding line merge display” for a line enables the line to be displayed with the line background merged with that of the next line.

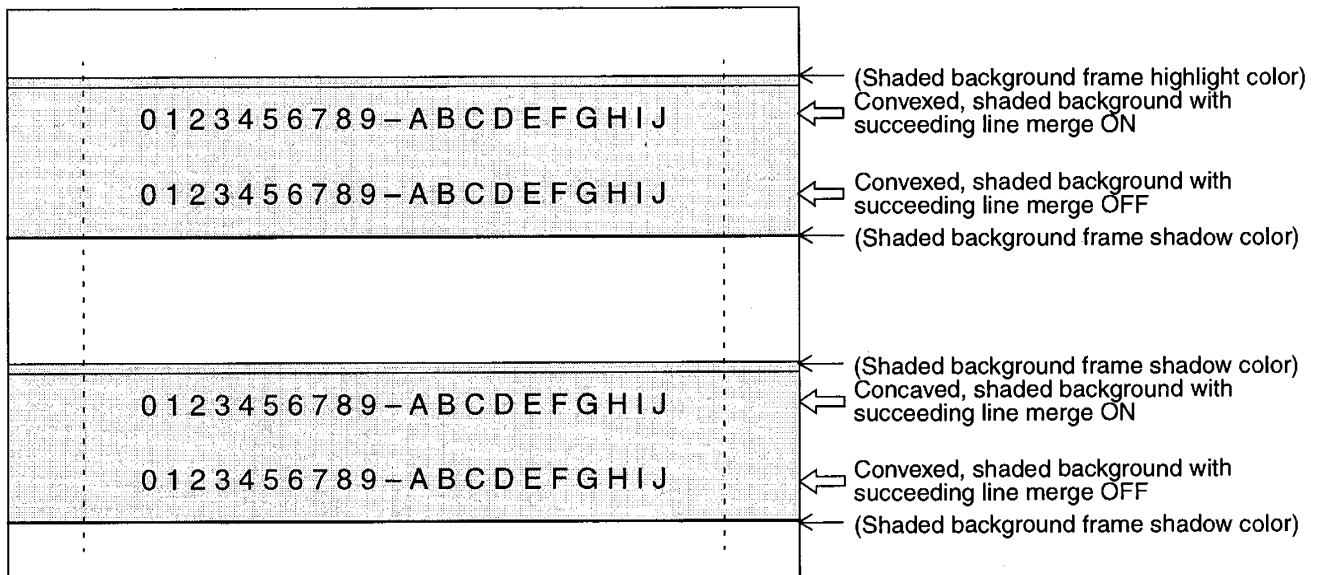
This undisplay the lower line of the line background shadow frame of the current line and the upper line of the line background shadow frame of the next line.

- Shaded background succeeding line merge control (Setting for each line)

Line control data set 2 (Command 4): Bit LD

LD	Shaded background succeeding line merge control
0	OFF
1	ON

- Examples of shaded background succeeding line merge display



Note: Specifying shaded background succeeding line merge display applies merge control to the character and line backgrounds at the same time.

If character background extended display is off, however, merge control ignores shaded background characters.

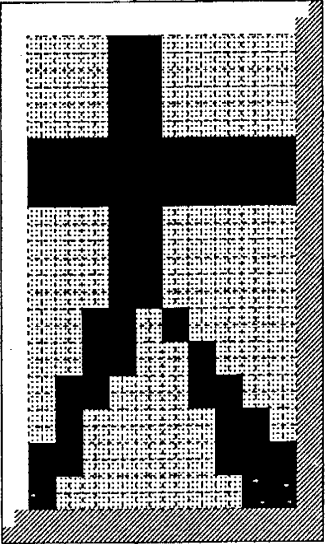
Display example of a combination of shaded character background display and shaded line background display (1)

Shaded line background

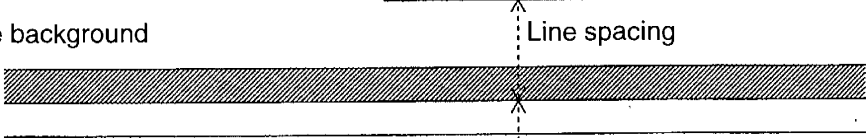


Shaded character background

Bit LD = 0
Bit LE = 0



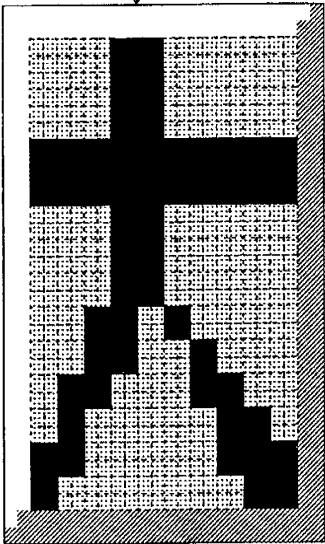
Shaded line background



Shaded line background

Shaded character background

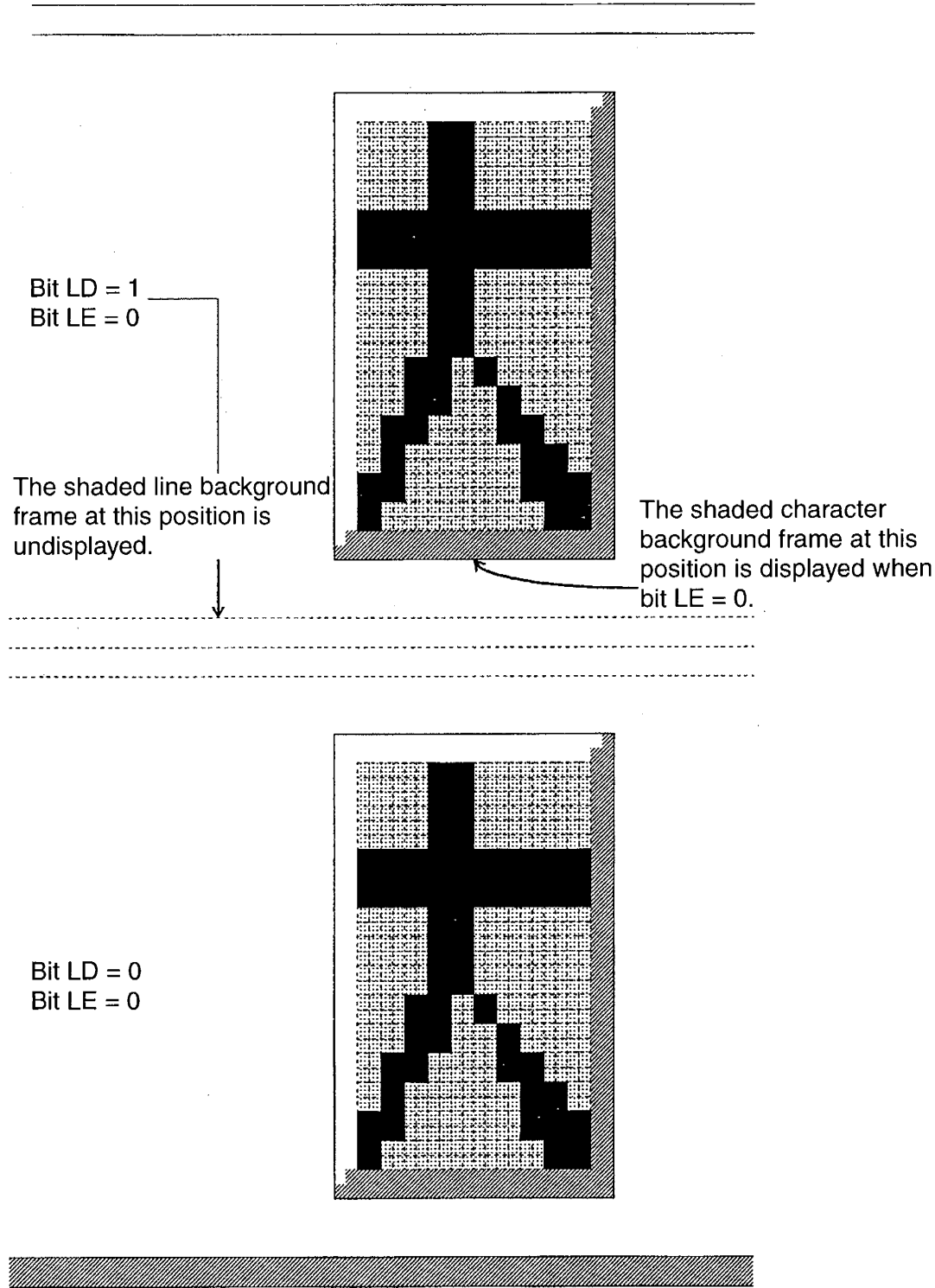
Bit LD = 0
Bit LE = 0



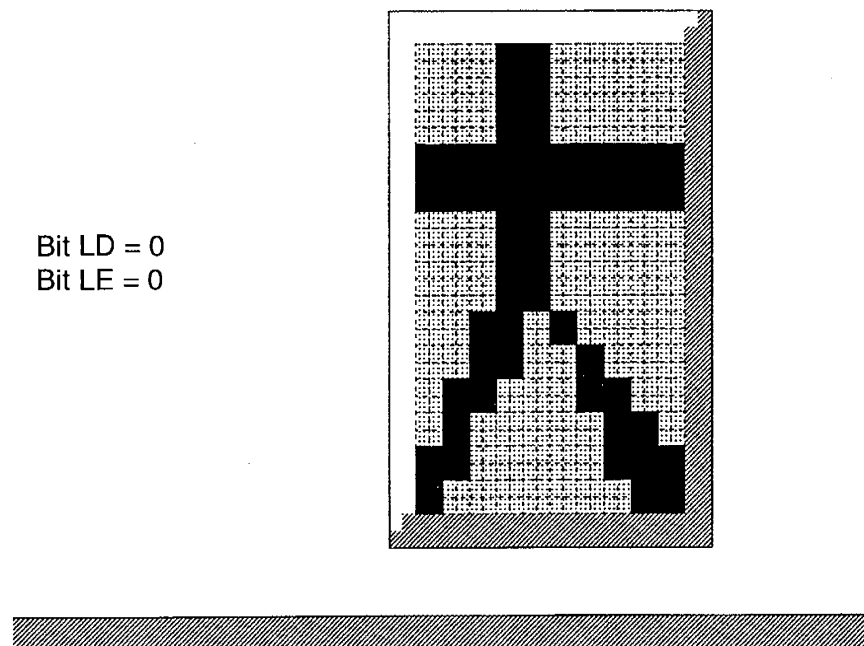
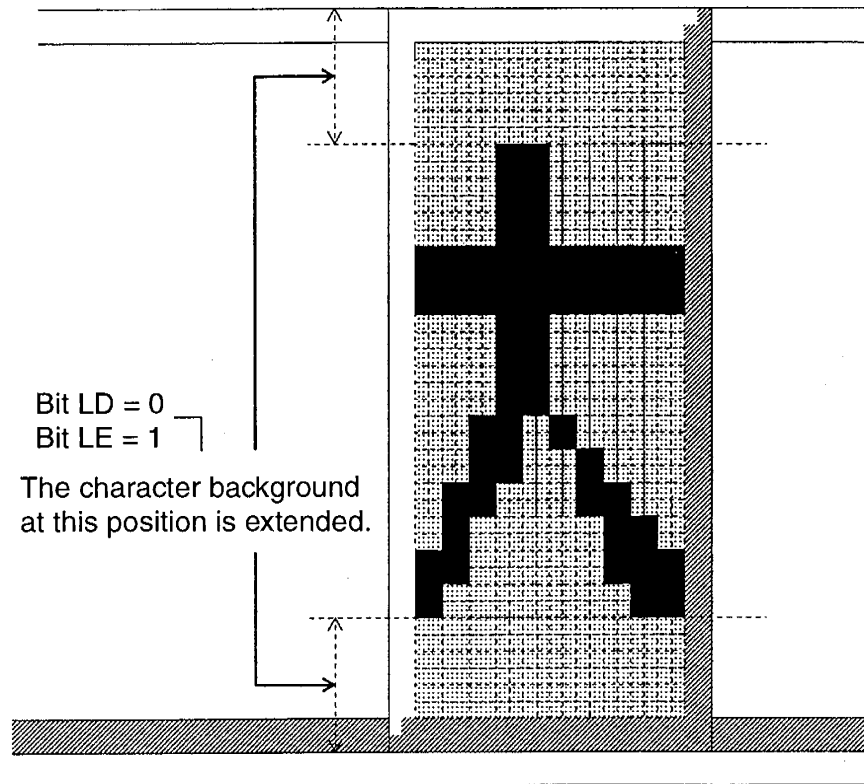
Shaded character background



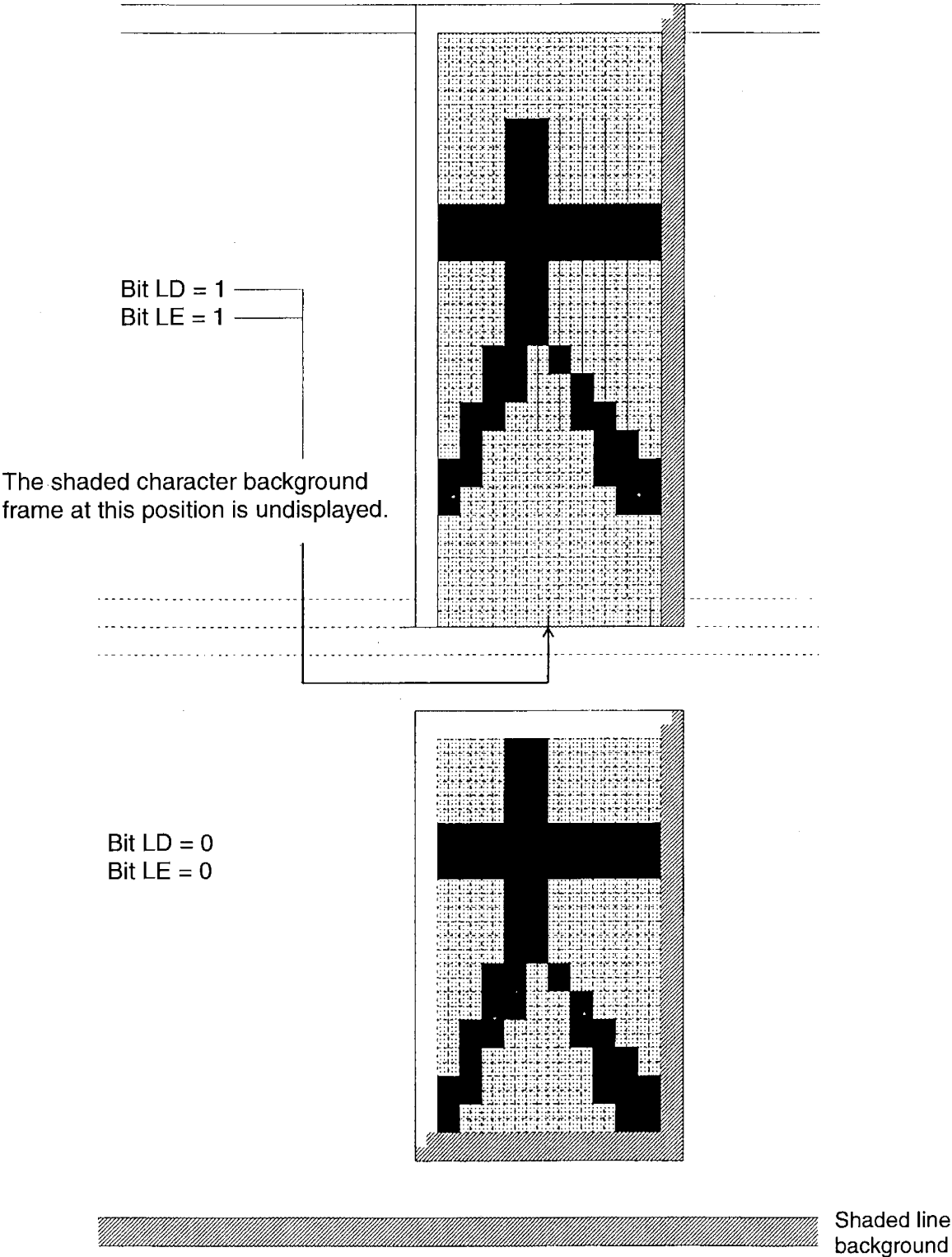
Display example of a combination of shaded character background display and shaded line background display (2)



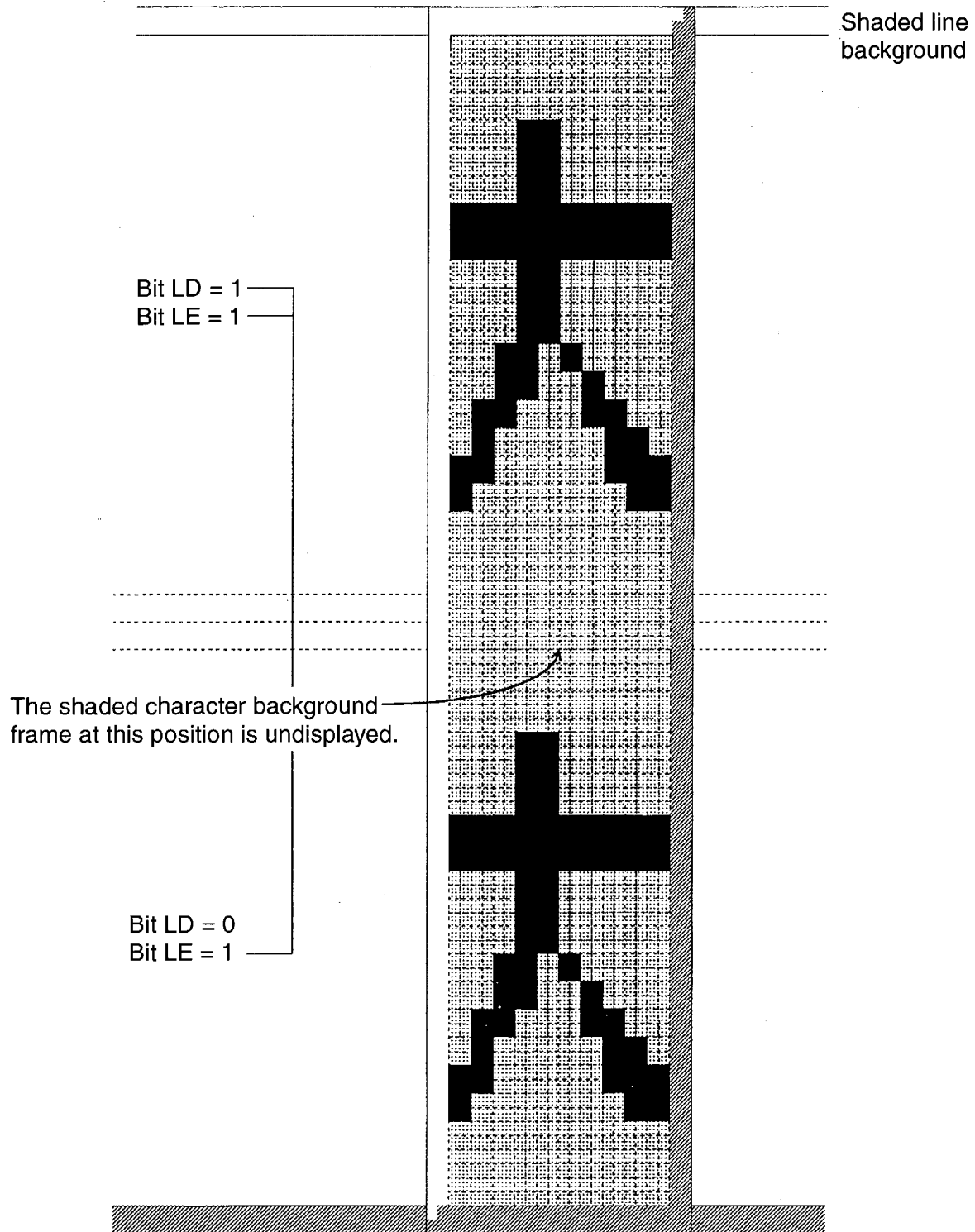
Display example of a combination of shaded character background display and shaded line background display (3)



Display example of a combination of shaded character background display and shaded line background display (4)



Display example of a combination of shaded character background display and shaded line background display (5)



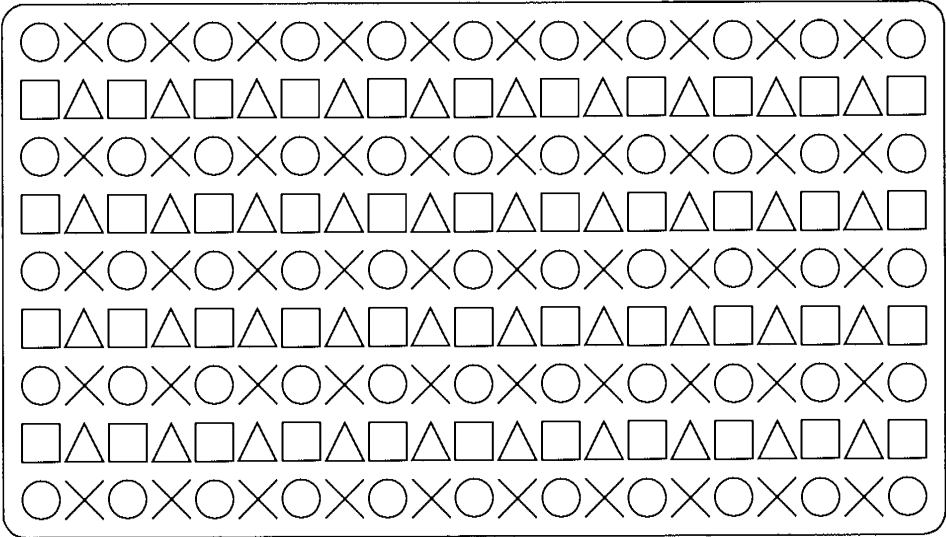
3.7 Screen Background Display

3.7.1 Screen background character display

Screen background character display is graphic character display by which the entire screen is filled with the repeatedly displayed same blocks of two by two, or four characters.

(1) Configuration of screen background character display

- Example of screen background character display



(2) Screen background character display control

- Screen background character output control

Screen output control 1 (Command 5-0): Bit PDS

PDS	Screen background character display
0	OFF
1	ON

- Screen background character code

Screen background character control 2 (Command 7-1): Bits PM7 to PM0

Of character codes 00H to FFH for 256 types of characters, only those character codes which are multiples of 4 can be set (PM0 = PM1 = 0).

Note: Only the L size of graphic characters can be used as screen background characters.

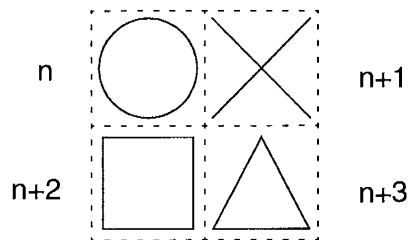
- Screen background character vertical size control

Screen background character control 4 (Command 7-3): Bits PH2 to PH0

PH2	PH1	PH0	Display vertical size
0	0	0	18 dots
0	0	1	20 dots
0	1	0	22 dots
0	1	1	24 dots
1	0	0	26 dots
1	0	1	28 dots
1	1	0	30 dots
1	1	1	32 dots

- Screen background character configuration control

Fixed block of 2 characters (vertical) × 2 characters (horizontal)



3.7.2 Screen background color display

The OSDC can output a screen background color for the entire screen as the bottom layer.

- Screen background output control

Screen output control 1 (Command 5-0): Bit UDS

UDS	Screen background color output
0	OFF
1	ON

- Screen background color control

Screen background character control 4 (Command 7-3): Bits U3 to U0

One of 16 colors can be set.

Screen background color				Screen background color signal output			
U3	U2	U1	U0	IOUT pin	GOUT pin	ROUT pin	BOUT pin
–	–	–	0	–	–	–	Low
–	–	0	–	–	–	Low	–
–	0	–	–	–	Low	–	–
0	–	–	–	Low	–	–	–
–	–	–	1	–	–	–	High
–	–	1	–	–	–	High	–
–	1	–	–	–	High	–	–
1	–	–	–	High	–	–	–

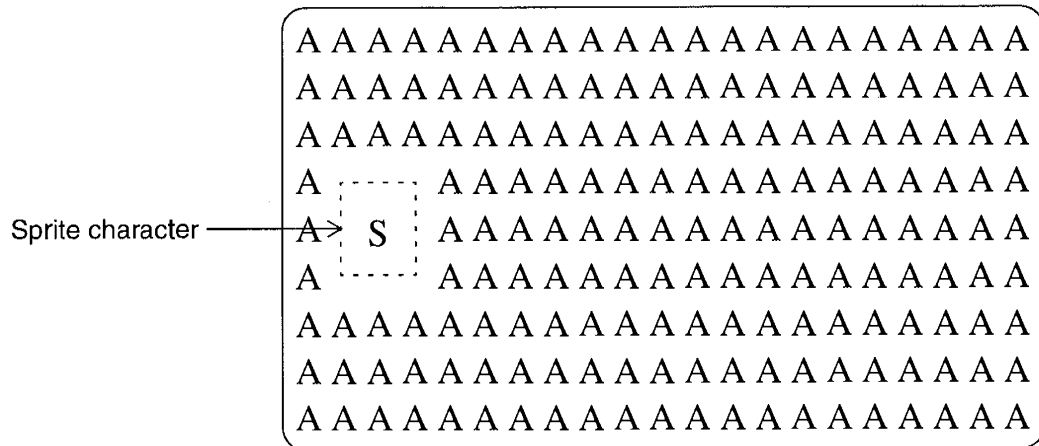
Note: The above table assumes display color signal output logic control (command 13-0) with DCX = 0.

3.8 Sprite Character Display

Sprite characters are displayed on the top layer. The OSDC supports sprite display of only graphic characters.

(1) Sprite character configuration

- Sprite character display example



(2) Sprite character display control

- Sprite character output control

Screen output control 1 (Command 5-0): Bit SDS

SDS	Sprite character output
0	OFF
1	ON

- Sprite character code

Sprite character control 2 (Command 8-1): Bits SM7 to SM0

A sprite character code can be selected from among character codes 00H to FFH for 256 types of characters.

When the sprite character consists of two or four characters, only a character code which is a multiple of 4 (SM0 = SM1 = 0) can be set.

Note: Only the L size of graphic characters can be used as sprite characters.

- Sprite character vertical display position control

Sprite character control 4 (Command 9-0): Bits SY9 to SY0

Settable between 0 and 2046 dots in 2-dot units.

- Sprite character horizontal display position control

Sprite character control 5 (Command 9-1): Bits SX9 to SX0

Settable between 0 and 2046 dots in 2-dot units.

- Sprite character vertical size control

Sprite character control 3 (Command 8-2): Bits SH3 to SH0

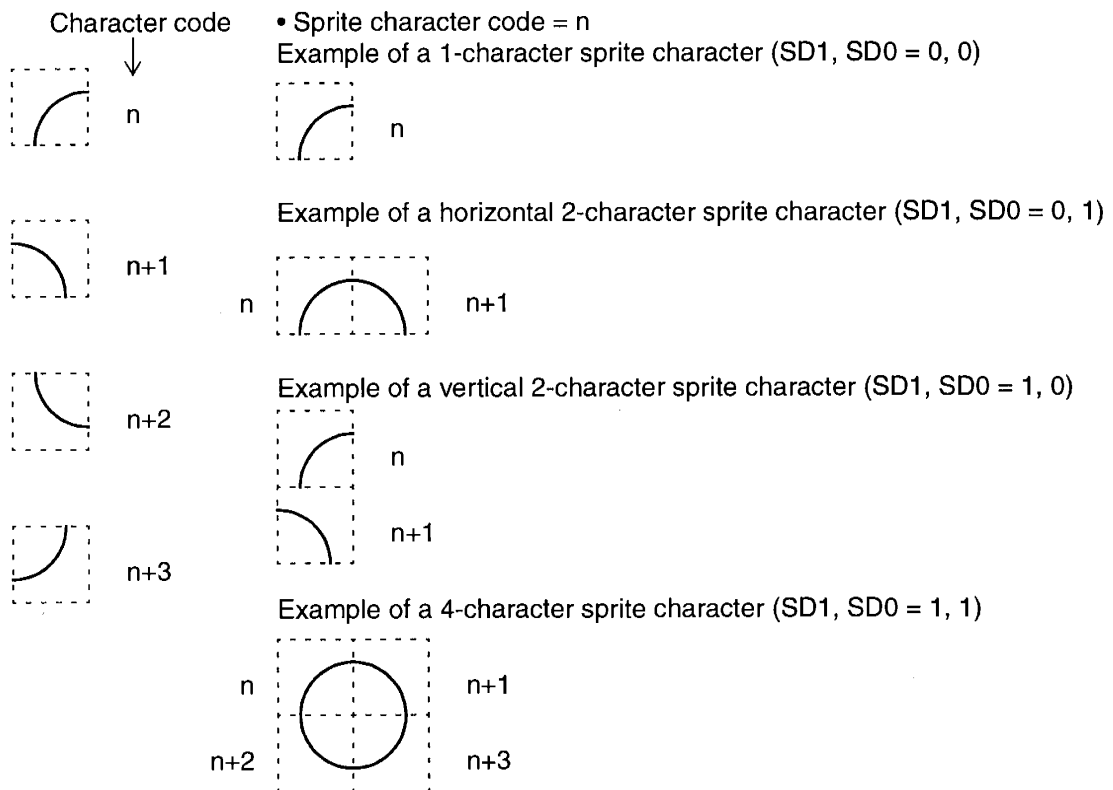
SH2	SH1	SH0	Display vertical size
0	0	0	18 dots
0	0	1	20 dots
0	1	0	22 dots
0	1	1	24 dots
1	0	0	26 dots
1	0	1	28 dots
1	1	0	30 dots
1	1	1	32 dots

- Sprite character configuration control

Sprite character control 2 (Command 8-1): Bits SD1 and SD0

SD1	SD0	Configuration
0	0	1 character
0	1	Horizontal set of 2 characters
1	0	Vertical set of 2 characters
1	1	2 characters × 2 characters

Sprite character configuration example



3.9 Command ROM Transfer Control

- Command ROM transfer

The OSDC can execute command ROM transfer to write commands at a higher speed for faster display than by normal serial command write.

Command ROM can register up to 16Kbytes of command data in advance.

- Command ROM transfer start address 1 (Command 14-0): TSD to TS8

For data transfer from command ROM, set command ROM transfer start address 1.

TSD to TS8	Transfer start address 1. Set the upper six bits in the 16-Kbyte space.
------------	---

- Command ROM transfer start address 2 (Command 14-1): TS7 to TS1

For data transfer from command ROM, set command ROM transfer start address 2.

TS7 to TS1	Transfer start address 2. Set the lower seven bits in the 16-Kbyte space.
------------	---

- Command ROM transfer end address 1 (Command 14-2): TED to TE8

For data transfer from command ROM, set command ROM transfer end address 1.

TED to TE8	Transfer end address 1. Set the upper six bits in the 16-Kbyte space.
------------	---

- Command ROM transfer end address 2 (Command 14-3): TE7 to TE1

For data transfer from command ROM, set command ROM transfer end address 2.

TE7 to TE1	Transfer end address 2. Set the lower six bits in the 16-Kbyte space. Issuing this command starts command ROM transfer.
------------	--

- Command ROM transfer synchronization control (Command 14-3): TSV

TSV	Transfer synchronization
0	Start transfer upon issuance of transfer end address 2 (command 14-3), regardless of display operation.
1	Start transfer at the falling edge of the first VSYNC input after the issuance of transfer end address 2 (command 14-3).

The command transfer execution time depends on the dot clock frequency. The reference value for transfer (of command-1 and command-2 data) to an entire screen (all of 32 columns × 16 rows) is as follows:

- With display-asynchronous setting [TSV = 0]
 - Dot clock 10 MHz: Approx. 2 ms
 - Dot clock 20 MHz: Approx. 1 ms
 - Dot clock 40 MHz: Approx. 0.5 ms
- With VSYNC-synchronous setting [TSV = 1]
 - Dot clock 10 MHz: Approx. 2 ms + Time from the issuance of transfer end address 2 to the first VSYNC input
 - Dot clock 20 MHz: Approx. 1 ms + Time from the issuance of transfer end address 2 to the first VSYNC input
 - Dot clock 40 MHz: Approx. 0.5 ms + Time from the issuance of transfer end address 2 to the first VSYNC input

Note1: Command ROM can register commands 0 to 9-1.

Note2: The FIL bit can be set as command ROM data.

Note3: During command ROM transfer, keep the \overline{CS} pin at the High level.
Setting the \overline{CS} pin to the Low level forces command ROM transfer to terminate.

Note4: The signal (TRE pin) indicating transfer in process goes active (High) upon issuance of transfer end address 2 and inactive (Low) upon termination of transfer, regardless of transfer synchronization control (TSV).

Note5: A malfunction caused by, for example, external noise may fix the TRE pin at the High level even after termination of command transfer or FIL operation. To prevent this, take two VSYNC periods as the maximum monitor time for the TRE pin when command transfer or FIL operation is executed. If the TRE pin remains High for more than two VSYNC periods after command transfer or FIL operation is started, clear the FIL bit to '0' to force command 0 to be issued.

- Normally, command transfer or FIL operation terminates within one VSYNC period after it is started.
- Writing '0' to the FIL bit forces FIL operation to terminate.
- Issuing any command (setting the \overline{CS} pin to the Low level) forces command transfer to terminate.

4 CONTROL FUNCTIONS

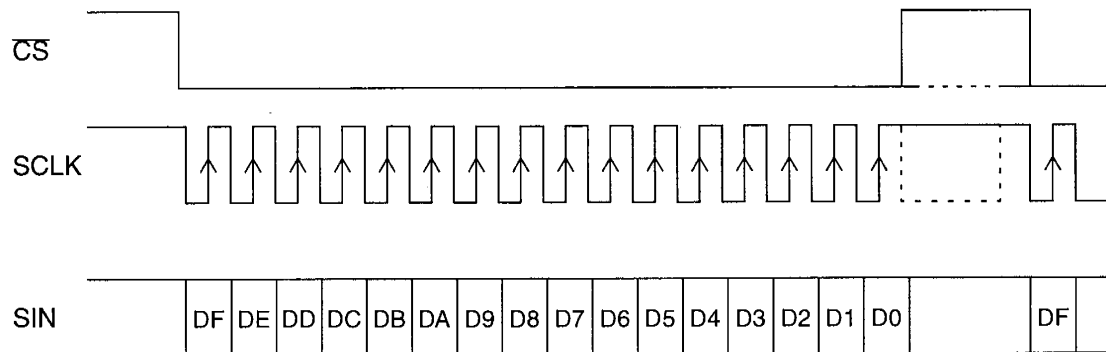
4.1 Serial Command Control

The MB90096 executes a serial command data write using the chip select (\overline{CS}), serial clock (SCLK), and serial data input (SIN) pins. The data length is 16 bits, which are shifted serially to be input to the SIN pin in MSB-first transfer mode.

If the \overline{CS} pin goes HIGH during transfer with data less than 16 bits, a command write is not guaranteed. Keeping the \overline{CS} pin LOW allows multiple items of command data to be written continuously. (It is however recommended to set the \overline{CS} pin to the HIGH level at intervals of tens of words for word synchronization.)

The SCLK clock frequency is 4 MHz at maximum. Set it such that: VRAM write cycle (a minimum of 16 clock pulses) > input horizontal sync pulse width. If this condition is not satisfied, VRAM write may fail.

- Serial command control timing



4.2 Dot Clock Control

- Dot clock selection control

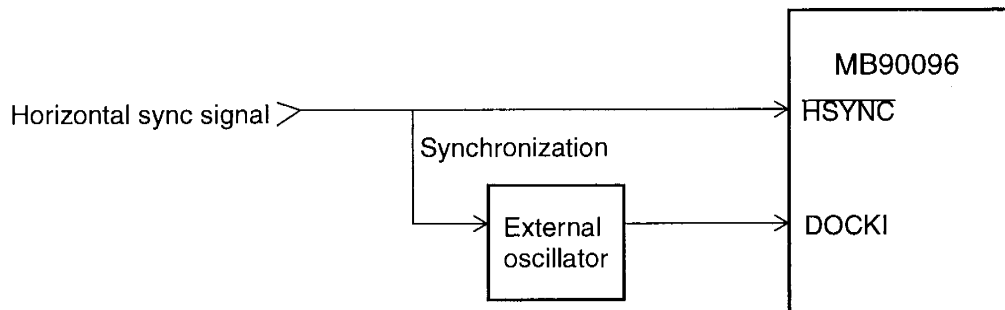
Dot clock control 1 (Command 11-2: Bit DC0)

DC0	Dot clock control
0 (Default value after reset)	External clock input (Internal VCO oscillation off)
1	Internal VCO generation

(1) External clock input

The MB90096 inputs a clock signal from an external oscillator.

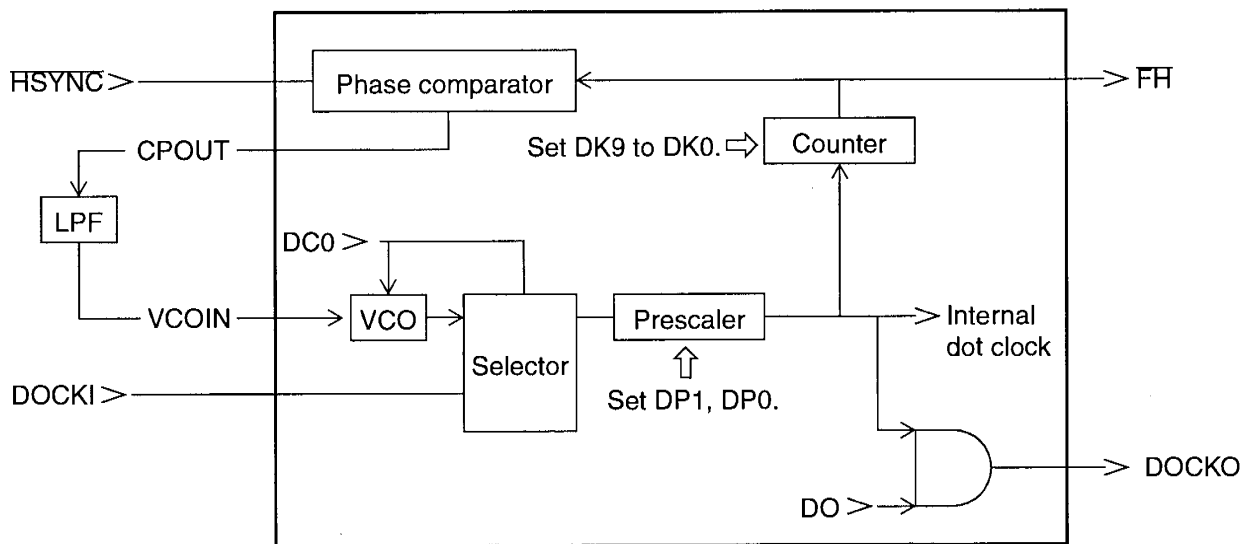
The clock signal is presumed to be synchronized with the input horizontal sync signal.



Note: For interlaced display with external signal input selected, supply the MB90096 with an external field signal (to the EVEN pin).

(2) Internal VCO generation

The MB90096 uses the clock generated by the internal VCO (PLL) as a dot clock through the internal prescaler.



Dot clock circuit configuration

- Dot clock prescaler control

Dot clock control 1 (Command 11-2: Bits DP1 to DP0)

DP1	DP0	Dot clock frequency
0	0	(Oscillation/1) 50 MHz to *
0	1	(Oscillation/2) 25 to 60 MHz
1	0	(Oscillation/4) 12.5 to 30 MHz
1	1	(Oscillation/8) 6.8 to 15 MHz

*: The value depends on the upper operation limit (currently being evaluated).

The prescaler can be set whether internal VCO generation or external clock input is selected.

- Dot clock control

Dot clock control 2 (Command 11-3: Bits DK9 to DK0)

The input horizontal sync signal (HSYNC) is frequency-divided to generate a desired dot clock frequency.

■ Example of setting dot clock control 2 (Bits DK9 to DK0)

This example assumes:

- NTSC system (horizontal frequency: 15.734 kHz)
- Dot clock frequency: 15 MHz

$$\text{Horizontal frequency/Dot clock frequency} = 15 \text{ MHz}/15.734 \text{ kHz} \doteq 953$$

DK9 to DK0 must be set in 4-dot units.

$$953/4 \doteq 238$$

Subtract 1 from 238 and set DK9 to DK0 to the binary equivalent of the result as follows:

$$\text{DK9 to DK0} = 238 - 1 = 237 = (0, 0, 1, 1, 1, 0, 1, 1, 0, 1)$$

$$[\quad = (\text{DK9}, \text{DK8}, \text{DK7}, \text{DK6}, \text{DK5}, \text{DK4}, \text{DK3}, \text{DK2}, \text{DK1}, \text{DK0})]$$

The actual dot clock frequency is obtained as follows:

$$\begin{aligned} \text{Dot clock frequency} &= 15.734 \text{ kHz} \times (237 + 1) \times 4 \\ &\doteq 14.979 \text{ MHz} \end{aligned}$$

4.3 Sync Signal Input

4.3.1 Vertical synchronization detection

Vertical synchronization is detected by sensing the level of the vertical sync signal at the leading or trailing edge of the horizontal sync pulse to detect the transition. The vertical display position on the screen depends on the vertical synchronization detection position.

Use I/O pin control (command 13-0) to select operation control.

- Selecting a vertical synchronization detection HSYNC edge

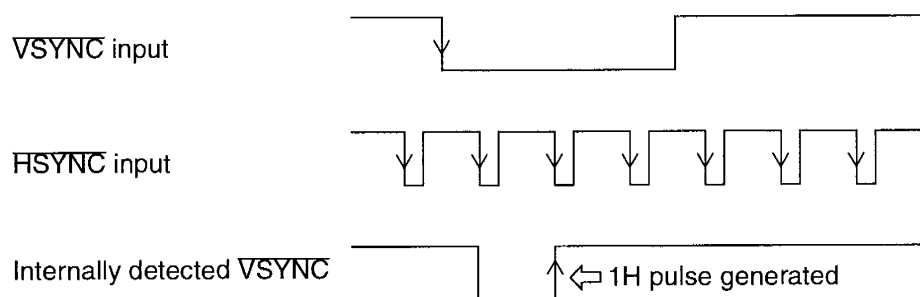
VHE	Vertical synchronization detection HSYNC edge
0	Detect vertical synchronization at the rising edge of HSYNC.
1	Detect vertical synchronization at the falling edge of HSYNC.

SIX: Sync signal input logic control

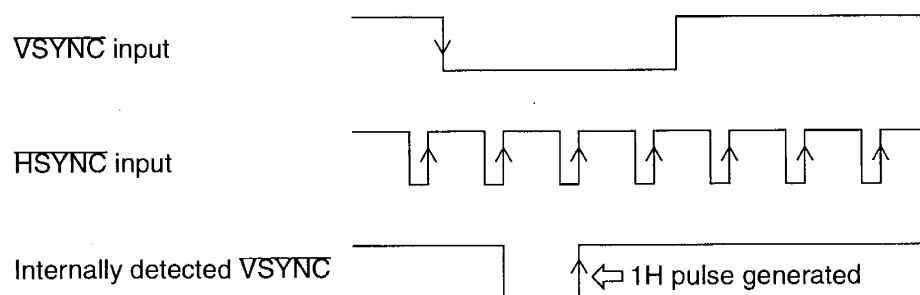
SIX	Sync signal input logic
0	The HSYNC and VSYNC pins are active low inputs.
1	The HSYNC and VSYNC pins are active high inputs.

- Operation examples of vertical synchronization detection

- (1) Detecting vertical synchronization at the rising edge of the horizontal sync pulse (VHE = 0)



- (2) Detecting vertical synchronization at the falling edge of the horizontal sync pulse (VHE = 1)



4.3.2 Field detection

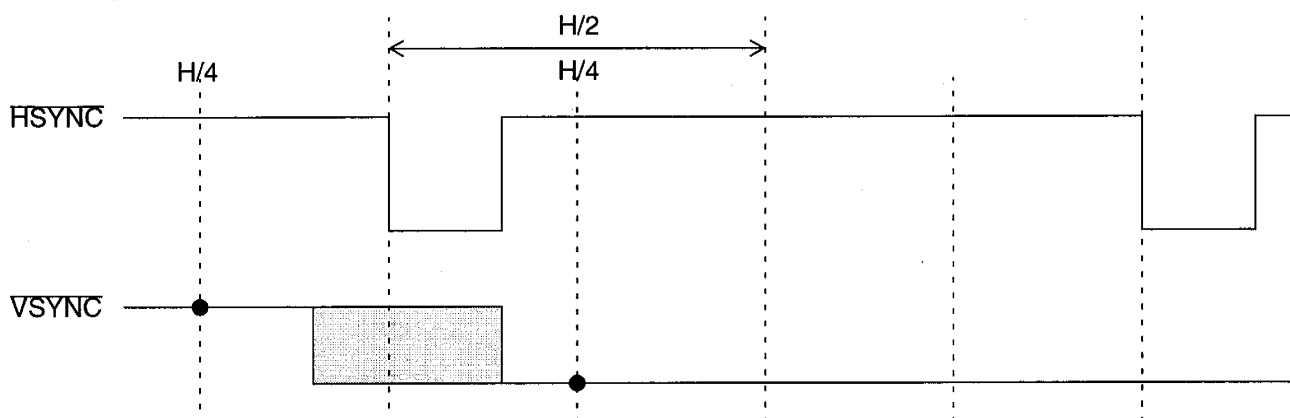
Information in this section applies to field signals used for interlaced display on NTSC systems. The information is not required for noninterlaced display.

This section describes the $\overline{\text{VSYNC}}$ - $\overline{\text{HSYNC}}$ relationship in the vicinity of the rising edge of $\overline{\text{VSYNC}}$ in interlaced display mode.

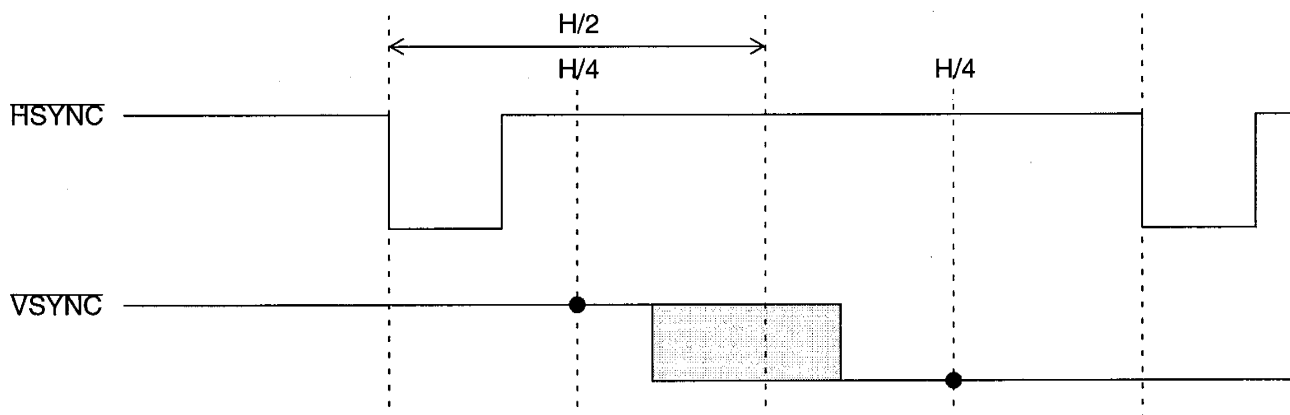
The internally generated field signal (set by command 11-0 with bit FLD = 0) is generated by detecting the level of $\overline{\text{VSYNC}}$ at “●” (H/4 timing) shown in the diagrams below. If the $\overline{\text{VSYNC}}$ signal causes a transition in the vicinity, normal field detection may not be performed.

(The signal level should be fixed for at least 18 dot clocks before and after the H/4 timing. For details, see the relevant electrical specification.)

- (1) Field 1 (Timing at which $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ fall almost at the same time)



- (2) Field 2 (Timing at which $\overline{\text{VSYNC}}$ falls in the vicinity of H/2)



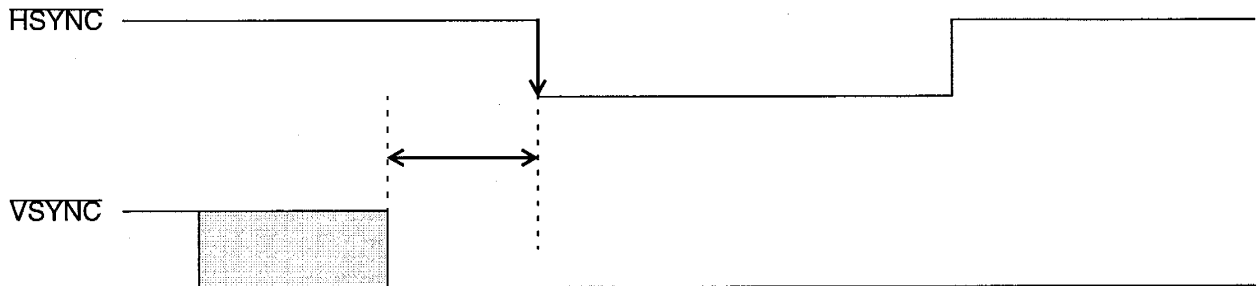
The MB90096 detects $\overline{\text{VSYNC}}$ internally at an edge of $\overline{\text{HSYNC}}$. For field 1 in which their transition timings are almost the same, therefore, the relevant command must be set depending on each of the three cases described below.

Field 2 does not require such specifications for specific cases because the $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ transition timings do not overlap in the field.

Note: The internally generated field signal can be used (set by command 11-0 with bit FLD = 0) only when internal VCO generation is selected (set by command 11-2 with bit DC0 = 1).

[Case 1]

The $\overline{\text{VSYNC}}$ signal causes a high-to-low transition sufficiently (at least four dot clocks) before the fall of the $\overline{\text{HSYNC}}$ signal.



Set command 13-0: $\text{VHE} = 0$ (to detect vertical synchronization at the leading edge of $\overline{\text{HSYNC}}$).

■ To use the internally generated field signal (set by command 11-0 with bit $\text{FLD} = 0$)

- Set command 11-0: $\text{FC0} = 0$ (no field correction).

Note that the EVEN pin input is ignored.

■ To use the external input field signal (set by command 11-0 with bit $\text{FLD} = 1$)

- Command 11-0: $\text{FC0} = 0$ (no field correction)

For field 1, input the Low level to the EVEN pin.

For field 2, input the High level to the EVEN pin.

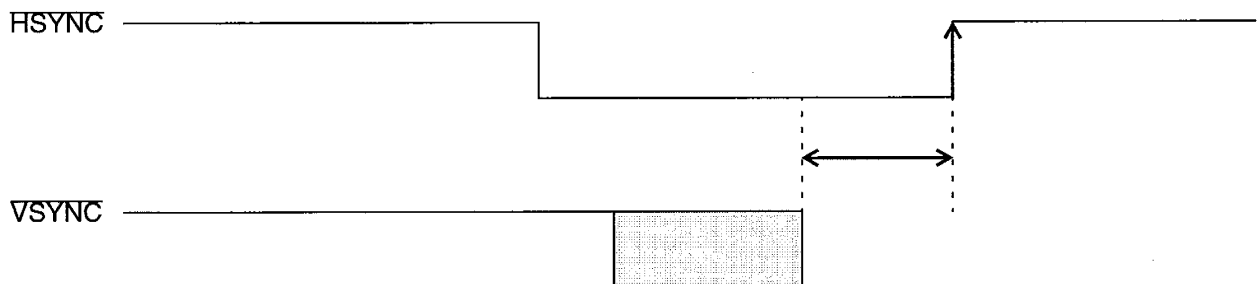
- Command 11-0: $\text{FC0} = 1$ (field correction)

For field 1, input the High level to the EVEN pin.

For field 2, input the Low level to the EVEN pin.

[Case 2]

The $\overline{\text{VSYNC}}$ signal causes a high-to-low transition after the fall of the $\overline{\text{HSYNC}}$ signal and sufficiently (at least two dot clocks) before the rise.



Set command 13-0: $\text{VHE} = 1$ (to detect vertical synchronization at the trailing edge of $\overline{\text{HSYNC}}$).

■ To use the internally generated field signal (set by command 11-0 with bit $\text{FLD} = 0$)

- Set command 11-0: $\text{FC0} = 0$ (no field correction).

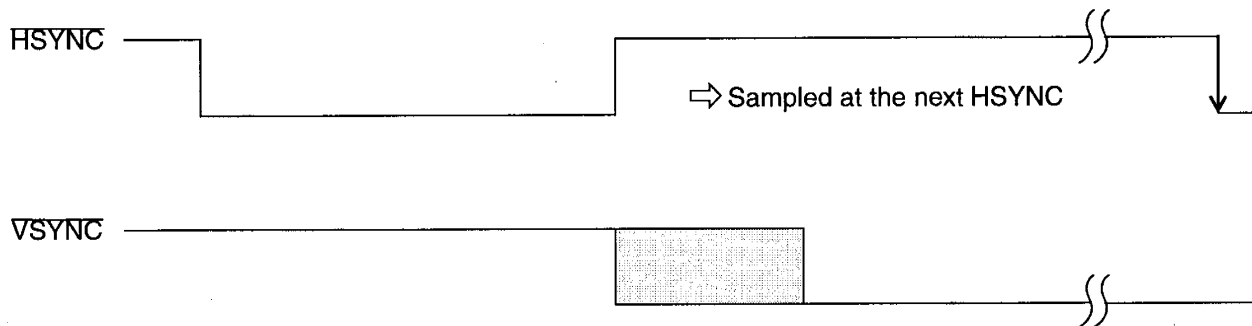
Note that the EVENT pin input is ignored.

■ To use the external input field signal (set by command 11-0 with bit FLD = 1)

- Command 11-0: FC0 = 0 (no field correction)
For field 1, input the Low level to the EVEN pin.
For field 2, input the High level to the EVEN pin.
- Command 11-0: FC0 = 1 (field correction)
For field 1, input the High level to the EVEN pin.
For field 2, input the Low level to the EVEN pin.

[Case 3]

The $\overline{\text{VSYNC}}$ signal causes a high-to-low transition after the fall of the $\overline{\text{HSYNC}}$ signal.



Set command 13-0: VHE = 0 (to detect vertical synchronization at the leading edge of $\overline{\text{HSYNC}}$).

■ To use the internally generated field signal (set by command 11-0 with bit FLD = 0)

- Set command 11-0: FC0 = 1 (field correction).
Note that the EVEN pin input is ignored.

■ To use the external input field signal (set by command 11-0 with bit FLD = 1)

- Command 11-0: FC0 = 1 (field correction)
For field 1, input the Low level to the EVEN pin.
For field 2, input the High level to the EVEN pin.
- Command 11-0: FC0 = 0 (no field correction)
For field 1, input the High level to the EVEN pin.
For field 2, input the Low level to the EVEN pin.

4.4 Display Signal Output

4.4.1 Display signal output timing

Display signals (outputs)

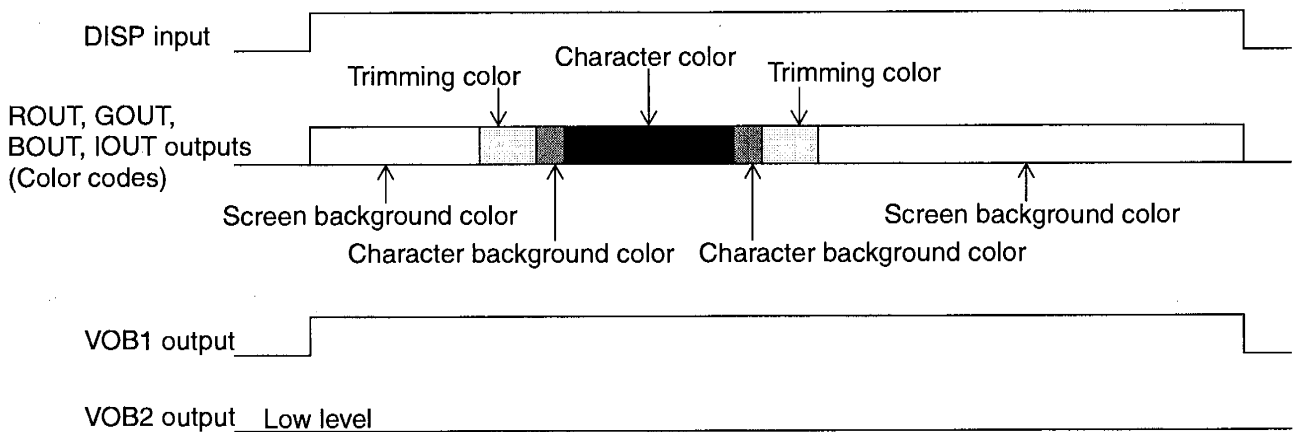
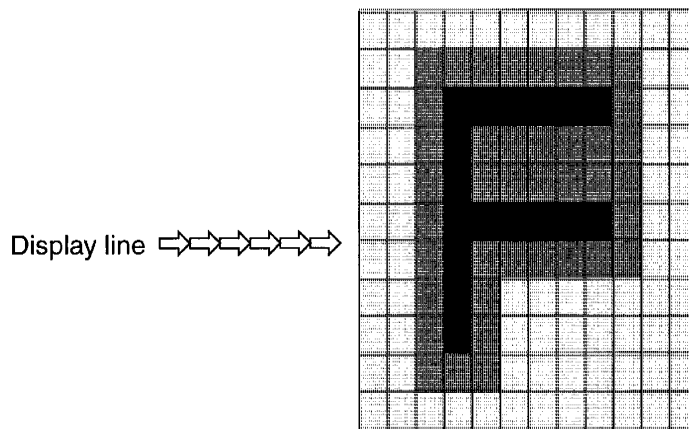
- Output display period signal: VOB1 pin
- Translucent color display period signal: VOB2 pin
- Color code signals: ROUT, GOUT, BOUT, IOUT pins

Display signal control signal (input)

- DISP pin

(1) **Example of normal color signal output (screen background output control ON, line background output control OFF, translucent color control OFF)**

Sample display

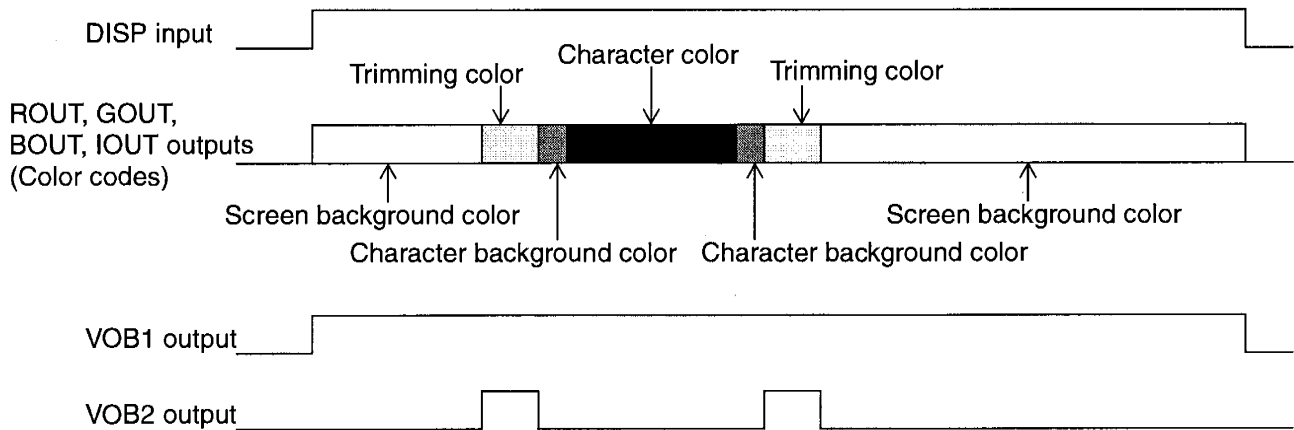
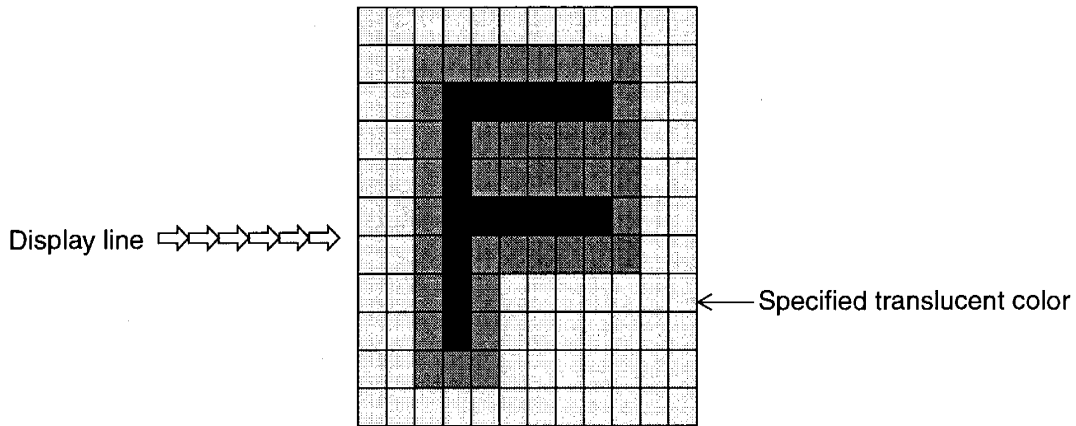


Note: In the above diagram, signals are active High.

(2) Output example of translucent color (for halftone output) 1

(Screen background output control ON, line background output control OFF, translucent color control ON, translucent color code = character background color code)

Sample display

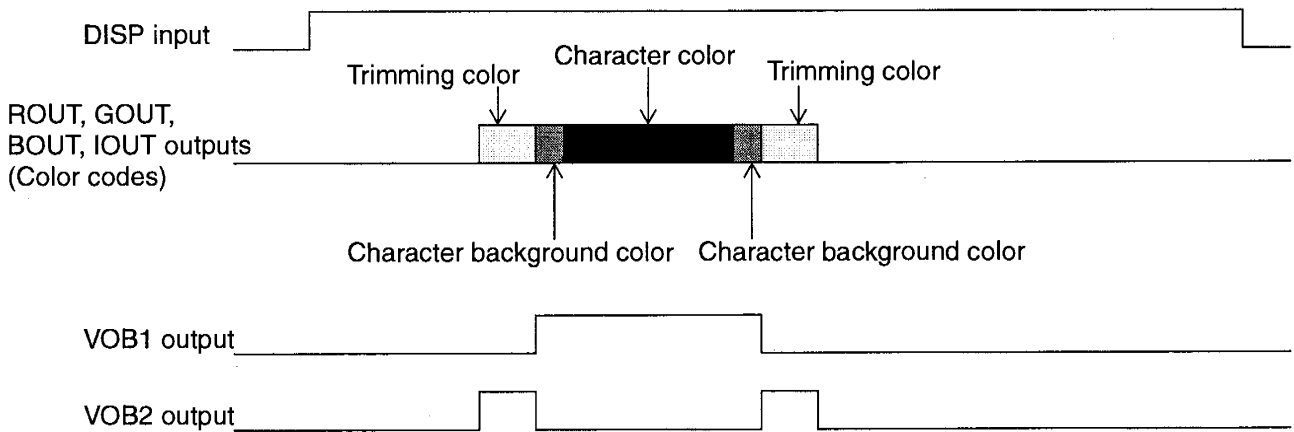
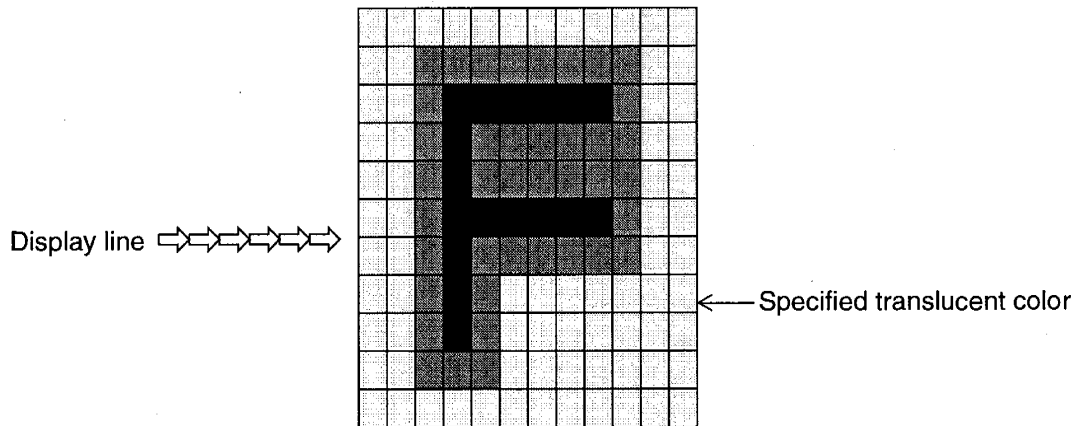


Note: In the above diagram, signals are active High.

(3) Output example of translucent color (for halftone output) 2

(Screen background output control OFF, line background output control OFF, translucent color control ON, translucent color code = character background color code)

Sample display



Note: In the above diagram, signals are active High.

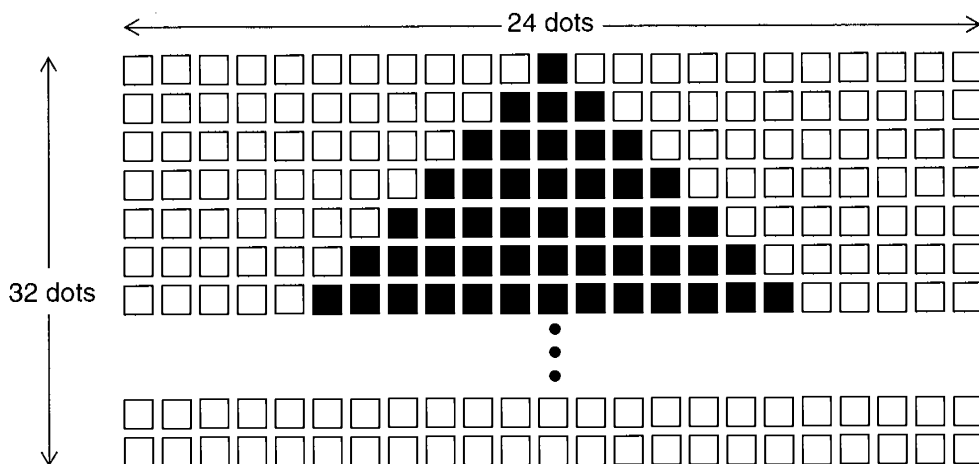
4.5 Scan Methods

You can adjust the OSD vertical display area relative to the entire screen by setting bits EG1 and EG0 to the number of rasters making up each dot of the MB90096.

Note: This setting affects the vertical display start position and line spacing control.

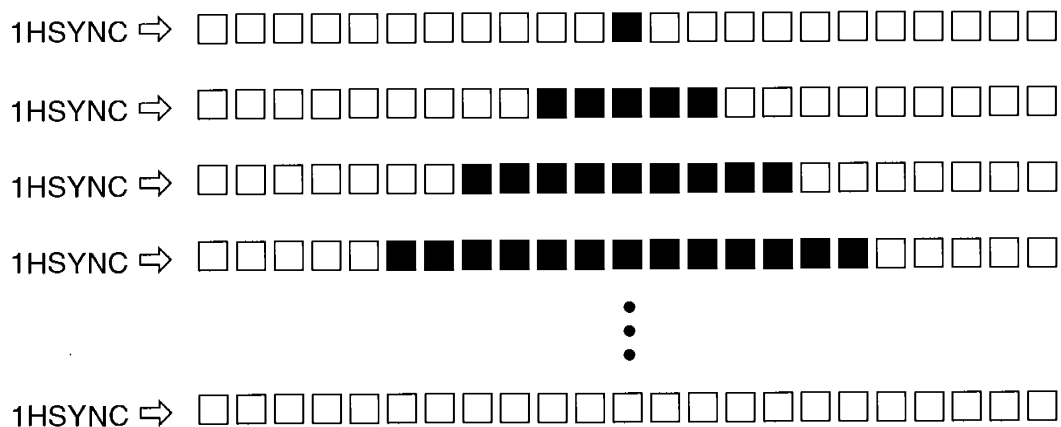
● Display example

Font ROM original data

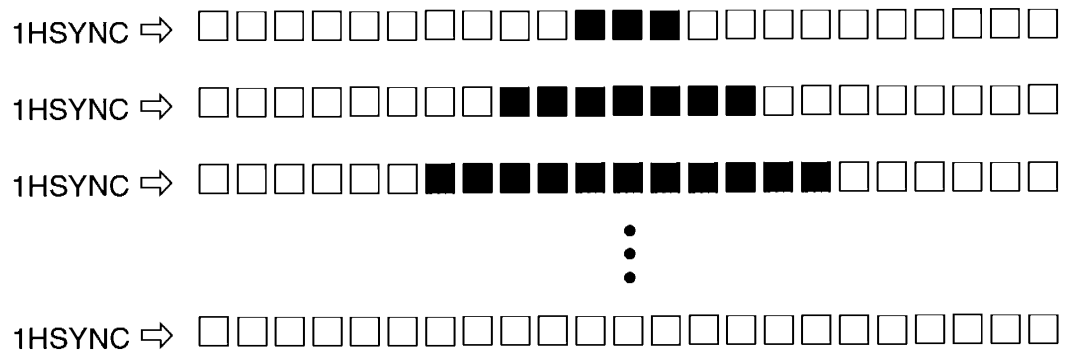


(1) Display with EG1 = 0, EG0 = 0, and each vertical dot consisting of one HSYNC signal (depending on the field signal) (Assuming interlaced display on TV)

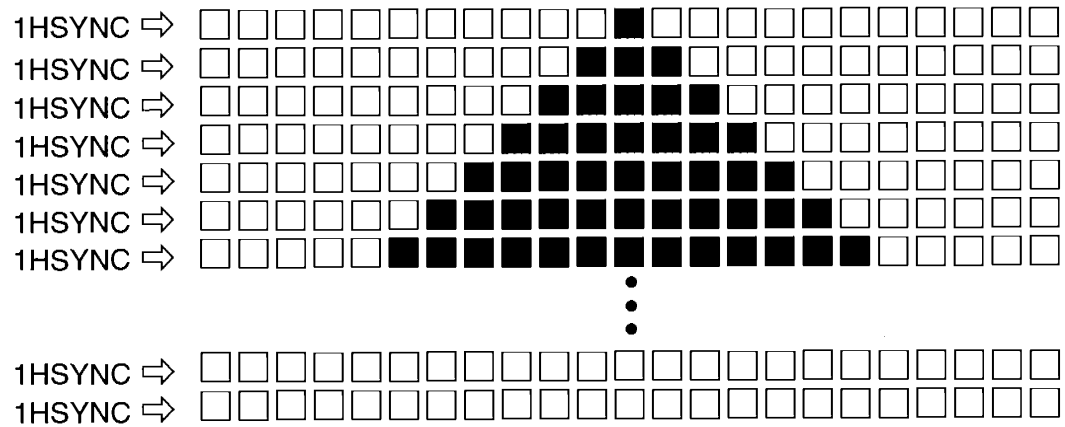
- EVEN = 0 (even-numbered fields)



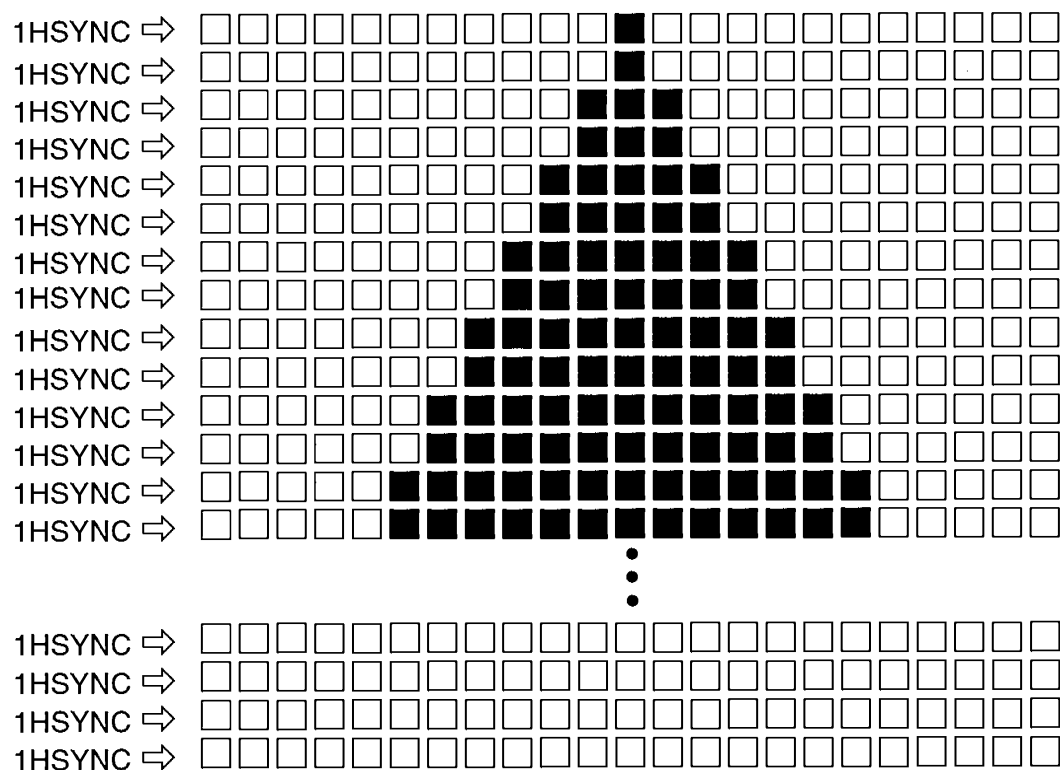
- EVEN = 1 (odd-numbered fields)



- (2) Display with EG1 = 0, EG0 = 1, and each vertical dot consisting of one HSYNC signal (independent of the field signal) (Assuming NTSC/PAL double-speed scan, almost equivalent to VGA)



- (3) Display with $EG1 = 1$, $EG0 = 0$, and each vertical dot consisting of two HSYNC signals (independent of the field signal) (Assuming VGA-class (640) or more horizontal scan lines at a higher vertical display ratio of the OSDC)



Note: It is prohibited to set “ $EG1 = 1$, $EG0 = 0$ ”.

5 DISPLAY CONTROL COMMANDS

5.1 Command List

Command No.	Command code/data													Function
	15-12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0000	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0	VRAM write address set
1	0001	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0	Character data set 1
2	0010	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0	Character data set 2
3	0011	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0	Line control data set 1
4	0100	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0	Line control data set 2
5 - 0	0101	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0	Screen output control 1
5 - 1	0101	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0	Screen output control 2
5 - 2	0101	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Vertical display position control
5 - 3	0101	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0	Horizontal display position control
6 - 0	0110	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0	Character vertical size control
6 - 1	0110	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0	Shaded back-ground frame color control
6 - 2	0110	1	0	TC	HC	TC3	TC2	TC1	TC0	HC3	HC2	HC1	HC0	Transparent/translucent color control
6 - 3	0110	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0	Graphic color control
7 - 1	0111	0	1	1	1	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0	Screen back-ground character control 1
7 - 3	0111	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0	Screen back-ground character control 2
8 - 1	1000	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0	Sprite character control 1
8 - 2	1000	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0	Sprite character control 2

(Continued)

Command No.	Command code/data													Function
	15-12	11	10	9	8	7	6	5	4	3	2	1	0	
9 - 0	1001	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	Sprite character control 3
9 - 1	1001	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	Sprite character control 4
11 - 0	1011	0	0	0	0	EG1	EG0	0	FC0	FLD	0	0	0	Synchronization control
11 - 2	1011	1	0	DO	0	0	0	DP1	DP0	0	0	0	DC0	Dot clock control 1
11 - 3	1011	1	1	DK9	DK8	DK7	DK6	DK5	DK4	DK3	DK2	DK1	DK0	Dot clock control 2
13 - 0	1101	0	0	0	VHE	0	0	SIX	0	0	DHX	DBX	DCX	I/O pin control
14 - 0	1110	0	0	0	0	0	0	TSD	TSC	TSB	TSA	TS9	TS8	CROM transfer start address 1
14 - 1	1110	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0	CROM transfer start address 2
14 - 2	1110	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8	CROM transfer end address 1
14 - 3	1110	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1	CROM transfer end address 2

5.2 Command Description

■ Command 0 (VRAM write address set)

This command specifies the write location in VRAM.

For the write location, set the row and column addresses.

Executing command 2 (character data set 2) starts actual VRAM fill operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0

AY3 to AY0 : Row address (0-F_H)

FL : Specify VRAM fill (0: OFF, 1: ON)

AX4 to AX0 : Column address (0-1F_H)

[Function]

Command 0 specifies a VRAM write address.

Command 0 specifies row and column addresses before being set by commands 1 and 2 (character data set commands) and row addresses before being set by commands 3 and 4 (line control data set commands).

[Supplement]

- A normal write (writing single-character data or single-line control data) is performed with “VRAM fill” set to OFF (FL = 0).
- After execution of command 2, the VRAM write address is incremented automatically. (The last column is incremented to the first column of the next line by line feed; the last row is incremented to the first row.)
- Turning “VRAM fill” on (FL = 1) writes the same character data (specified by commands 1 and 2) to the area from the row/column address specified by command 0 to the last column (column 32) on the last row (row 16). “VRAM fill” is activated by issuing ‘character data set 2’ (command 2). When “VRAM fill” is active, the TRE pin maintains High-level output.

- Notes:**
- When commands 3 and 4 (line control data set) are set, column addresses (AX4 to AX0) are ignored.
 - Execution of command 3 or 4 (line control set command) does not automatically increment the address.
 - “VRAM fill” is valid only to commands 1 and 2 (character data set commands).
 - During execution of “VRAM fill,” commands 1 to 4 cannot be issued normally.

■ Command 1 (Character data set 1)

This command sets character data. Executing command 2 (character data set 2) sets VRAM to reflect it on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0

MC3 to MC0 : Character color (From among 16 colors)	MS1, MS0 : Character horizontal size control 0, 0: 12 dots 0, 1: 18 dots 1, 0: 24 dots 1, 1: –
MB3 to MB0 : Character background color (From among 16 colors)	
MM1, MM0 : Character background control (0, 0: OFF) (0, 1: Solid-fill display) (1, 0: Concaved, shaded display) (1, 1: Convexed, shaded display)	

[Function]

Command 1 sets character data. Executing command 2 (character data set 2) sets VRAM to reflect it on the screen.

[Supplement]

- The character color, character background color, character background type, and character horizontal size can be set in an arbitrary combination for each character.
- Shaded display enables vertical or horizontal merge display depending on the combination of bit MB of command 2 and bits LD and LE of command 4.
- The shaded background frame color is set by command 6-1.

Note: The M size cannot be specified for graphic characters.

■ Command 2 (Character data set 2)

This command sets additional character data to be written to VRAM as specified by command 0 (VRAM write address set), along with the character data set by command 1 (character data set 1).

After this command is executed, the VRAM write address is incremented automatically.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0

MR:	Shaded background succeeding character merge control (0: Do not merge) (1: Merge with the character to the right)	MG:	Character/graphic character control (0: Character, 1: Graphic character)
		MBL:	Blink control (0: OFF, 1: ON)
M8 to M0:	Character code		

[Function]

Command 2 writes the above setting data to the area of VRAM specified by command 0 (VRAM write address set 1), along with the character data set by command 1 (character data set 1). After this command is executed, the VRAM write address is incremented automatically.

[Supplement]

- Turning blink control on (MBL = 1) causes characters to blink depending on the settings of bits BT1, BT0, BD1, and BD0 of command 5-1.
- The shaded background succeeding character merge control bit (MR) has an effect only on the character specified as being shaded by command 1 (MM1 = 1).

Notes:

- Since reset input makes the contents of the entire area of VRAM undefined, be sure to set VRAM before display.
- The M size cannot be specified for graphic characters.

■ Command 3 (Line control data set 1)

This command sets line control data. Executing command 4 (line control data set 2) sets VRAM to reflect it on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0

LHS:	Line character vertical size type control (0: Character vertical size A) (1: Character vertical size B)	LFD, LFC:	Trimming output control (0, 0: All OFF) (0, 1: Trimming ON for character with no character background) (1, 0: Trimming ON for character with no or solid-filled character background) (1, 1: Trimming output ON)
LW2 to LW0:	Line spacing control (0 to 14 dots in 2-dot units)	LFB, LFA:	Trimming control (0, 0: Trimming OFF) (0, 1: Right trimming) (1, 0: Left trimming) (1, 1: Both-side trimming)
LF3 to LF0:	Trimming color (From among 16 colors)		

[Function]

Command 3 sets line control data. Executing command 4 (line control data set 2) sets line VRAM to reflect it on the screen.

[Supplement]

- The actual size, whose type is specified by the line character vertical size type control bit (LHS), is specified by command 6-0 (character vertical size control).
- The trimming mode is specified by command 5-1 (trimming mode control bits FM1 and FM0).

■ Command 4 (Line control data set 2)

Set additional line control data to be written to the row address in line VRAM specified by command 0 (VRAM write address set), along with the line control data set by command 3 (line control data set 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0

LDS:	Line character output control (0: Off, 1: ON)	LD:	Shaded background succeeding line merge control (0: Independent, 1: Merge with the next line)
LG1, LG0:	Line enlargement control (0, 0: Normal) (0, 1: Double width) (1, 0: Double height) (1, 1: Double width/height)	LM1, LM0:	Line background control (0, 0: OFF) (0, 1: Solid-fill display) (1, 0: Concaved, shaded display) (1, 1: Convexed, shaded display)
LE:	Character background extension control (0: Normal, 1: Extended)	L3 to L0:	Line background color (From among 16 colors)

[Function]

Command 4 writes the above setting data to the area of line VRAM specified by command 0 (VRAM write address set 1), along with the line control data set by command 3 (line control data set 1).

[Supplement]

- The shaded background succeeding line merge control bit (LD) has different effects on the character shaded backgrounds and line shaded backgrounds. For details, see Section 3.6.2 "Shaded background succeeding line merge display."

- Notes:**
- Since reset input makes the contents of the entire area of VRAM undefined, be sure to set VRAM before display.
 - Issuing this command does not automatically increment the VRAM write address. For each line to be set, set the address using command 0.

■ Command 5-0 (Screen output control 1)

This command controls screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0

SDS:	Sprite character output control (0: OFF, 1: ON)	PDS:	Screen background character output control (0: OFF, 1: ON)
UDS:	Screen background output control (0: OFF, 1: ON)	DSP:	Display output control (Control of character + trimming + character background + line background) (0: OFF, 1: ON)

[Function]

Command 5-0 controls screen display output.

- Note:**
- When one or more of bits SDS, PDS, UDS, and DSP are ON, setting any of the rest to ON from OFF may display the corresponding screen (or character) with only the first field shifted vertically. For workarounds, see Section 6.4 "Notes on Use."

■ Command 5-1 (Screen output control 2)

This command controls screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0

BT1, BT0: Blink cycle control
 (0, 0 : 16V)
 (0, 1 : 32V)
 (1, 0 : 48V)
 (1, 1 : 64V)

FM1, FM0: Trimming type control
 (0, 0: 1-dot horizontal trimming)
 (0, 1: 2-dot horizontal trimming)
 (1, 0: Pattern background 1)
 (1, 1: Pattern background 2)

BD1, BD0: Blink duty ratio control
 (0, 0 : 1/0)
 (0, 1 : 1/1)
 (1, 0 : 1/3)
 (1, 1 : 3/1)

[Function]

Command 5-1 controls screen display output.

[Supplement]

- The blink control bits of this command control blinking of the character for which blink control has been turned on (MBL = 1) by command 2 and of the sprite character for which sprite character blink control has been turned on (SBL = 1) by command 8-2.

■ Command 5-2 (Vertical display position control)

This command controls the vertical display position of the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y8 to Y0: Vertical display position control
 (0-2044 in 4-dot units)

[Function]

Command 5-2 controls the vertical display position of the screen.

■ Command 5-3 (Horizontal display position control)

This command controls the horizontal display position of the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0

X8 to X0: Horizontal display position control
(0-2044 in 4-dot units)

[Function]

Command 5-3 controls the horizontal display position of the screen.

■ Command 6-0 (Character vertical size control)

This command controls the vertical display size A/B of each character.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0

HB2 to HB0: Character vertical size control B
(18 to 32 dots in 2-dot units)

HA2 to HA0: Character vertical size control A
(18 to 32 dots in 2-dot units)

[Function]

Command 6-0 controls the vertical display size A or B of each character.

[Supplement]

- This command sets the actual value of the vertical size (LHS = 0: Size A, LHZ = 1: Size B) set for each line by command 3.

■ Command 6-1 (Shaded background frame color control)

This command controls the frame color of a shaded background.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0

BH3 to BH0: Shaded background frame high-light color
(From among 16 colors)

BS3 to BS0: Shaded background frame shadow color
(From among 16 colors)

[Function]

Command 6-1 controls the frame color of a shaded background.

[Supplement]

- This command sets the frame colors of the character for which shaded character

background display has been specified (MM1 = 1) by command 1 and of the shaded background for which shaded background display has been specified (LM1 = 1) by command 4.

- The highlight color indicates the color of the left and top edges of the character area in the shaded character background convex display mode or the color of the top edge of the line area in the shaded line background convex display mode.
- Shadow color indicates the color of the right and bottom edges of the character area in the shaded character background convex display mode or the color of the bottom edge of the line area in the shaded line background convex display mode.
- In the shaded character background or shaded line background concave display mode, the highlight and shadow colors used in the convex mode are replaced with each other.

■ Command 6-2 (Transparent/translucent color control)

This command controls transparent and translucent colors.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	0	TC	HC	TC3	TC2	TC1	TC0	HC3	HC2	HC1	HC0

TC: Transparent color control
(0: OFF, 1: ON)

TC3 to TC0: Transparent color code
(From among 16 colors)

HC: Translucent color control
(0: OFF, 1: ON)

HC3 to HC0: Translucent color code
(From among 16 colors)

[Function]

Command 6-2 controls transparent and translucent colors.

[Supplement]

- Setting bit TC to 1 allows the areas in the color specified as a transparent color (by TC3 to TC0) to be made void (displaying the screen on the lower layer in those areas instead).
- Setting bit HC to 1 makes those areas void which have the color specified as a translucent color (by HC3 to HC0) and outputs the translucent color display period signal from the VOB2 pin at the same timing. The signal is used for an external circuit to perform processing such as decreasing the intensity.

- Notes:**
- When turning on both of transparent and translucent color controls, set different colors as the transparent and translucent colors.
 - The translucent color display period signal from the VOB2 pin is output for areas other than the characters, trimming, and graphics on the main screen.

■ Command 6-3 (Graphic color control)

This command replaces the code-specified graphic color by the character color or character trimming color.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0

GF: Graphic color/trimming color replace control
(0: OFF, 1: ON)

GF3 to GF0: Code of character to be replaced by trimming color
(From among 16 colors)

GC: Graphic color/character color replace control
(0: OFF, 1: ON)

GC3 to GC0: Code of character to be replaced by character color
(From among 16 colors)

[Function]

Command 6-3 replaces the specified color of graphic characters by the character color or character trimming color.

[Supplement]

- Graphic characters are registered in font ROM with fixed colors. This command can be used to replace two of 16 colors with the specified trimming and character colors.
- Setting bit GF to 1 allows the color, which has been set as the color to be replaced by a trimming color, to be replaced by the trimming color specified for that line (by command 3).
- Setting bit GC to 1 allows the color, which has been set as the color to be replaced by a character color, to be replaced by the trimming color specified for that character (by command 1).

- Notes:**
- This command applies only to the colors of graphic characters on the main screen.
 - When turning on both of trimming color and character color replace controls, set different colors as those to be replaced by the trimming and character colors.
 - The transparent and translucent colors apply to the colors after replacement.

■ Command 7-1 (Screen background character control 1)

This command controls screen background characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	1	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

PM7 to PM0: Screen background character code
(000H to 0FFH for 256 different characters)

[Function]

Command 7-1 controls screen background characters.

[Supplement]

- Turning on screen background character output control (PDS = 1) in command 5-0 starts displaying screen background characters.

- The screen background character vertical size control bits (PH2 to PH0) of command 7-3 can specify the vertical size.

- Notes:**
- Of 256 characters in the first half of a set of 512 characters, only those character codes which are multiples of 4 can be set (PM1 = 0, PM0 = 0) for screen background characters.
 - Screen background characters are fixed in a graphic character display configuration of “2 columns x 2 rows”.
 - Graphic color/trimming color replace control (command 6-3) is not available to screen background characters.

■ Command 7-3 (Screen background character control 2)

This command controls screen background characters and the screen background color.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0

PH3 to PH0: Screen background character vertical size control
(18-32 dots in 2-dot units)

U3 to U0: Screen background color
(From among 16 colors)

[Function]

Command 7-3 controls screen background characters and the screen background color.

[Supplement]

- Turning on screen background output control (UDS = 1) in command 5-0 starts displaying the screen background color.
- Turning on screen background character output control (PDS = 1) in command 5-0 starts displaying screen background characters.

■ Command 8-1 (Sprite character control 1)

This command controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SD1, SD0: Sprite character configuration control
(0, 0: 1 character)
(0, 1: Horizontal set of 2 characters)
(1, 0: Vertical set of 2 characters)
(1, 1: 2 × 2 characters)

SM7 to SM0: Sprite character code
(000H to 0FFH for 256 different characters)

[Function]

Command 8-1 controls sprite characters.

[Supplement]

- Turning on sprite character output control (SDS = 1) in command 5-0 starts displaying sprite characters.
- The sprite character vertical and horizontal start positions are set by commands 9-0 and 9-1.
- The vertical size can be specified by the sprite character vertical size control bits (SH2 to SH0) of command 8-2. The sprite character blink control bit is used for blink control.
- The sprite character blink cycle and blink duty ratio depend on the settings of bits BT1, BT0, BD1, and BD0 of command 5-1.

Notes:

- Only 256 characters in the first half of a set of 512 characters can be set as sprite characters.
- For a sprite character consisting of two characters, only a character code (SM1 = 0, SM0 = 0) which is a multiple of 4 can be set.
- Sprite characters are fixed in graphic character display mode.
- Graphic color/trimming color replace control (command 6-3) is not available to sprite characters.

■ Command 8-2 (Sprite character control 2)

This command controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0

SBL: Sprite character blink control
(0: OFF, 1: ON)

SH3 to SH0: Sprite character vertical size control
(18-32 dots in 2-dot units)

[Function]

Command 8-2 controls sprite characters.

[Supplement]

- For sprite settings, see [Supplement] for command 8-1.

■ Command 9-0 (Sprite character control 3)

This command controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0

SY9 to SY0: Sprite character vertical display position control
(0 to 2046 in 2-dot units)

[Function]

Command 9-0 controls the sprite character vertical display position.

[Supplement]

- For sprite settings, see [Supplement] for command 8-1.

■ Command 9-1 (Sprite character control 4)

This command controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX9 to SX0: Sprite character horizontal display position control
(0 to 2046 in 2-dot units)

[Function]

Command 9-1 controls the sprite character horizontal display position.

[Supplement]

- For sprite settings, see [Supplement] for command 8-1.

■ Command 11-0 (Synchronization control)

This command controls synchronization.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	EG1	EG0	0	FC0	FLD	0	0	0

EG1, EG0: Vertical enlargement control
(0, 0: Interlaced)
(0, 1: Noninterlaced)
(1, 0: Setting prohibited)
(1, 1: Double height)

FC0: Field 0 correction control
Field E-0 replacement
(0: No correction, 1: Correction)
FLD: Field 0 signal input control
(0: Internally divided clock generation, 1: External input)

[Function]

Command 11-0 controls synchronization.

[Supplement]

- The vertical enlargement control bits (EG1, EG0) adjusts the display area in the vertical direction according to the display scan method. This setting applies to all of vertical counts (display position and dot size).
- For interlaced display (EG1 = 0, EG0 = 0), use the field 0 signal input control bit (FLD) to select either internal generation or external input of field signals. For the external input, input the field signal through the EVEN pin.
- For interlaced display (EG1 = 0, EG0 = 0), use the field 0 signal correction control bit (FC0) to correct field signals. For details, see Section 4.3.2 “Field detection.”

■ Command 11-2 (Dot clock control 1)

This command controls dot clocks.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	DO	0	0	0	DP1	DP0	0	0	0	DC0

DO: Dot clock pin output control
(0: OFF, 1: ON)

DC0: Dot clock selection control
(0: External input, 1: Internal VCO (H-PLL))

DP1, DP0: Dot clock prescaler control
(0, 0 : 1/1)
(0, 1 : 1/2)
(1, 0 : 1/4)
(1, 1 : 1/8)

[Function]

Command 11-2 controls dot clocks

[Supplement]

- Turning on dot clock pin output control (DO = 1) allows the internal dot clock to be output to the DOCKO pin.
- The dot clock prescaler control bits (DP1, DP0) are used to specified the frequency range of the dot clock. For details, see Section 4.2 “Dot Clock Control.”

Note: • If any external device does not require the dot clock, you should turn off dot clock pin output control (DO = 0) to minimize generation of noise.

■ Command 11-3 (Dot clock control 2)

This command control dot clocks.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	1	DK9	DK8	DK7	DK6	DK5	DK4	DK3	DK2	DK1	DK0

DK9 to DK0: Number of dot clock frequency-divisions
(In 4-dot units)

[Function]

Command 11-3 adjusts the frequency of the dot clock used.

[Supplement]

This command sets the value (in 4-dot units) to divide the frequency of the dot clock generated by the prescaler to the horizontal sync signal cycle.

Note: • A value of 040H or less cannot be set.
• This setting is required only when the internal VCO is used.

■ Command 13-0 (I/O pin control)

This command controls input/output pins.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	0	0	VHE	0	0	SIX	0	0	DHX	DBX	DCX

VHE: HSYNC edge selection for vertical synchronization detection
(0: Leading edge, 1: Trailing edge)

SIX: Logic control for sync signal input
(0: Negative logic, 1: Positive logic)

DCX: Logic control for display color signal output
(0: Positive logic, 1: Negative logic)

DBX: Logic control for display output period signal output
(0: Positive logic, 1: Negative logic)

DHX: Logic control for translucent period signal output
(0: Positive logic, 1: Negative logic)

[Function]

Command 13-0 controls input/output pins.

[Supplement]

- The HSYNC edge selection bit for vertical synchronization detection (VHE) can avoid vertical dancing due to the input timing of vertical and horizontal sync signals. For details, see Section 4.3 “Sync Signal Input.”

Note: • The sync signal input logic control bit (SIX) applies to both of vertical and horizontal sync signals.

■ Command 14-0 (Command ROM transfer start address 1)

This command sets command ROM transfer start address 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	TDS	TSC	TSB	TSA	TS9	TS8

TSD to TS8: Command ROM transfer start address 1
(Upper address)

[Function]

Command 14-0 sets command ROM transfer start address 1.

[Supplement]

This command sets the upper address for starting command ROM transfer.

■ Command 14-1 (Command ROM transfer start address 2)

This command sets command ROM transfer start address 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0

TS7 to TS1: Command ROM transfer start address 2
(Lower address)

[Function]

Command 14-1 sets command ROM transfer start address 2.

[Supplement]

This command sets the lower address for starting command ROM transfer.

■ Command 14-2 (Command ROM transfer end address 1)

This command sets command ROM transfer end address 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8

TED to TE8: Command ROM transfer end address 1
(Upper address)

[Function]

Command 14-2 sets command ROM transfer end address 1.

[Supplement]

This command sets the upper address for terminating command ROM transfer.

■ Command 14-3 (Command ROM transfer end address 2)

This command sets command ROM transfer end address 2.

Setting the command starts command transfer operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1

TSV: Command ROM transfer synchronization control
(0: Asynchronous, 1: Synchronous)

TE7 to TE1: Command ROM transfer end address 2
(Lower address)

[Function]

Command 14-3 sets command ROM transfer end address 2.

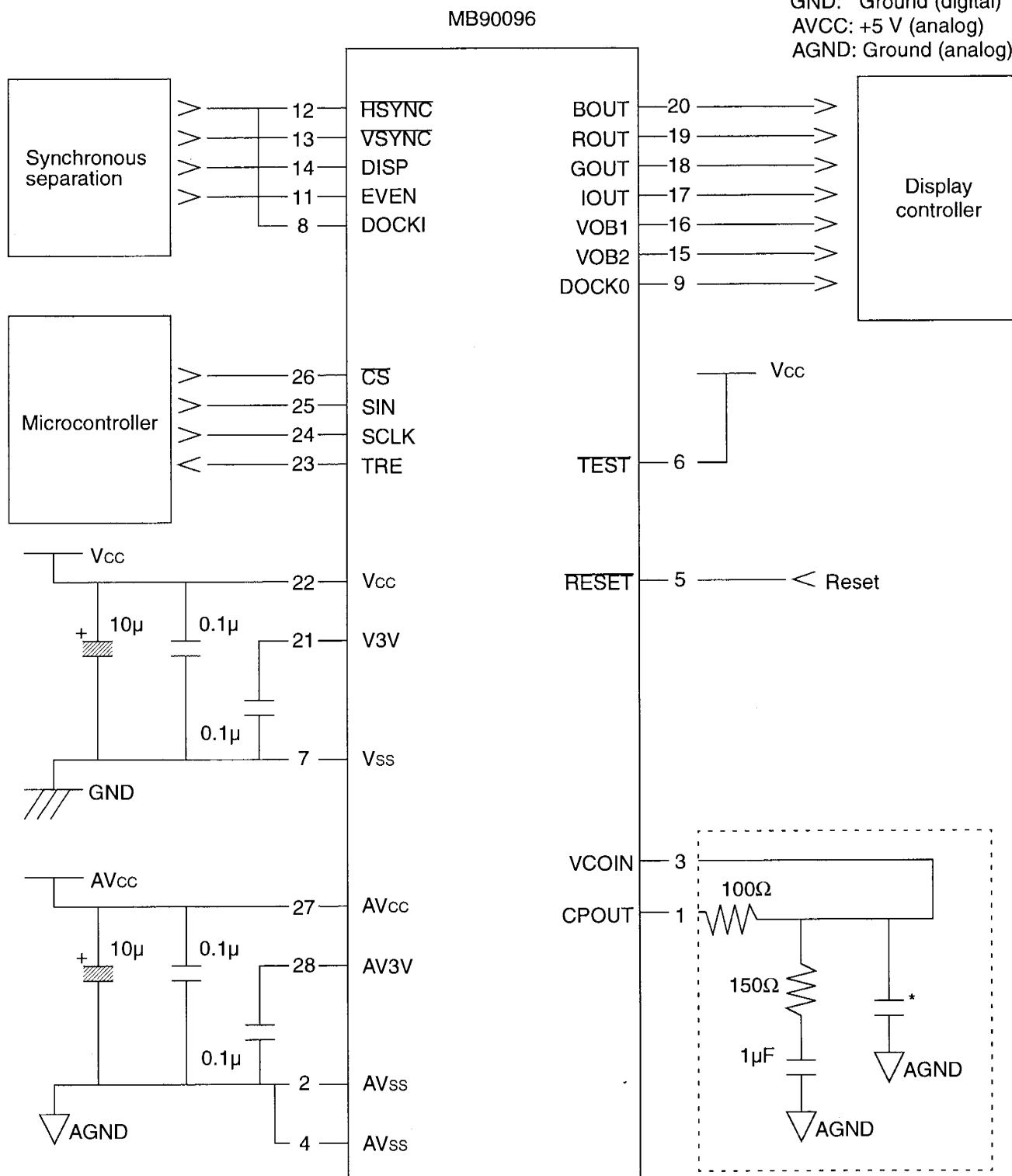
[Supplement]

- This command sets the lower address for terminating command ROM transfer.
- Turning command ROM transfer synchronization control on (TSV = 1) starts transfer at the rising edge of the vertical sync signal.
- Issuing this command with command ROM transfer synchronization control off (TSV = 0) starts command ROM transfer immediately.

6 APPLICATIONS

6.1 Application Circuit Example

VCC: +5 V (digital)
 GND: Ground (digital)
 AVCC: +5 V (analog)
 AGND: Ground (analog)



*: Requires adjustment depending on the operating conditions.

6.2 Power Supplies

The MB90096 has pairs of digital (V_{cc} , V_{ss}) and analog (AV_{cc} , AV_{ss}) power-supply and ground pins. The V_{cc}/AV_{cc} power-supply pins and the V_{ss}/AV_{ss} ground pins are independent of each other.

■ Notes on using an analog power supply

Since the analog power supply supplies power to the internal VCO, it requires special consideration separately from the digital power supply.

In general, pay attention to the following points:

- Design the system so that the ground and power supply impedances are suppressed. In addition, the ground line should be laid out on a ground plane including peripheral analog circuits.
- The digital (V_{cc} , V_{ss}) and analog (AV_{cc} , AV_{ss}) power supplies must be separated from each other. The V_{cc} and AV_{cc} pins, and the V_{ss} and AV_{ss} pins must not have a potential different in between.
- To supply digital and analog power from the same power source, separately route the wires from the source and use a choke coil to prevent digital noise from interfering with the analog subsystem via the power source.
- Insert a relatively high-capacity (10 to 100 μF) electrolytic capacitor as a bypass capacitor between the power supply and ground, separately between the digital and analog subsystems.

6.3 Treatment of Unused Pins

Pins unused on the MB90096 must be treated as follows.

Pin name	Pin No.	Input/output	Treatment
CPOUT	1	Output	Leave the pin open.
VCOIN	3	Input	Connect the pin to Vss.
DOCKI	8	Input	Input horizontal sync signal (connect the pin to HSYNC pin).
DOCKO	9	Output	Leave the pin open.
FH	10	Output	Leave the pin open.
EVEN	11	Input	Connect the pin to Vcc or leave it open.
HSYNC	12	Input	–
VSNC	13	Input	–
DISP	14	Input	Connect the pin to Vcc or leave it open.
IOUT(C3)	17	Output	Leave the pin open.
GOUT(C2)	18	Output	Leave the pin open.
ROUT(C1)	19	Output	Leave the pin open.
BOUT(C0)	20	Output	Leave the pin open.
VOB1	16	Output	Leave the pin open.
VOB2	15	Output	Leave the pin open.
SCLK	24	Input	–
SIN	25	Input	–
CS	26	Input	–
TRE	23	Output	Leave the pin open.
RESET	5	Input	–
TEST	6	Input	Connect the pin to Vcc.

6.4 Notes on Use

This section summarizes notes on using the MB90096.

(1) Initial state after reset input

- Commands for initialization

The MB90096 enters the display-off state upon reset input (input of a LOW-level signal to the **RESET** pin). The contents of VRAM (character RAM and line RAM) are undefined them. When the MB90096 is released from the reset input, issue the following commands to initialize control operation:

- Synchronization control (Command 11-0)
- Dot clock control 1 (Command 11-2)
- Dot clock control 2 (Command 11-3)
- I/O pin control (Command 13-0)

After that, set other items of command data.

VRAM setting (by commands 1 to 4) require normal dot clock and sync signal inputs.

- Display output pins

When the MB90096 is released from the reset input, all I/O pin control bits are set to "0" (display output pins are positive logic) and the display signal pins (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) start signal output at LOW level.

To use these display signal pins for output using negative logic, use an external circuit for masking until command initialization is completed.

(2) Command refresh

Command data and VRAM data set by serial transfer remain held in the MB90096 as long as it is powered. You should still refresh display data periodically to correct data corrupted, for example, by external noise during serial transfer or eliminate display errors caused for some reason.

Display data is refreshed by repeat writing data to VRAM (all data including blank characters) and setting all command data at intervals of tens of milliseconds to several seconds.

For writing data to VRAM, it is also recommended to set the write address for each line (using command 0).

(3) Prevention of malfunction after command transfer or FIL operation

A malfunction caused by, for example, external noise may fix the TRE pin at the High level even after termination of command transfer or FIL operation. If the microcomputer detects the High level at the TRE pin and keeps on waiting, the entire system hangs up.

To prevent the above situation, take about two VSYNC periods as the maximum monitor/wait time for the TRE pin after command transfer or FIL operation is executed.

If the TRE pin remains High for more than two VSYNC periods after command transfer or FIL operation is started, clear the FIL bit to '0' and issue command 0 by serial transfer.

(Issuing command 0 by serial transfer forces command transfer and FIL operation to terminate while setting the TRE pin to the Low level).

(4) Setting the display on/off control bits (DSP, SDS, PDS, UDS)

Assume that one or more of bits DSP, SDS, PDS, and UDS in command 5-0 are on. If you set the other bits from off to on, the corresponding screen (character) may appear vertically distorted (shifted) only for the first field.

[Solution]

Use either of the following methods to solve this problem.

- Use the command transfer function to turn display on or off in synchronization with VSYNC. Register the on/off combination of DSP, SDS, PDS, and UDS in command ROM in advance. The following 32 bytes can register all combinations. Register the combination you want to use.

[5000, 5010, 5020, 5030, 5040, 5050, 5060, 5070, 5080, 5090, 50A0, 50B0, 50C0, 50D0, 50E0, 50F0]

Select a command string (2 bytes) for turning display on, set VSYNC synchronization (using command 14-3 with bit TSV = 1), then transfer the command.

This setting enables command transfer automatically in synchronization with the leading edge of the VSYNC pulse.

- Use serial transfer of command setting for turning display on or off in synchronization with VSYNC.

Have the OSD control microcomputer recognize VSYNC to execute serial write in synchronization with VSYNC.

This assumes bit control to turn on each of bits DSP, SDS, PDS, and UDS within two H periods from the leading edge of the VSYNC pulse.

Other workarounds by manipulating individual bits

(Workaround specific to bit DSP) Turning character, character background, and line background display on/off

- You can turn display on/off using bits LDS, LM1, and LM0 instead of bit DSP. To turn on/off display of the character, character background, and line background, use line control bits LDS, LM1, and LM0 with bit DSP set to on.

(Workaround specific to bit SDS) Turning sprite display on/off

- Using blank characters

To turn on/off display of a sprite character, set the blank character code to turn the display off or the desired character code to turn it on, with bit SDS set to on.

- Setting the display position

To turn off display of a sprite character, set the horizontal display position to a position outside the screen, with bit SDS set to on.

(Workaround specific to bit PDS) Turning screen background character display on/off

- Using blank characters to turn display on/off

To turn on/off display of screen background characters, set the blank character code to turn the display off or the desired character code to turn it on, with bit PDS set to on.

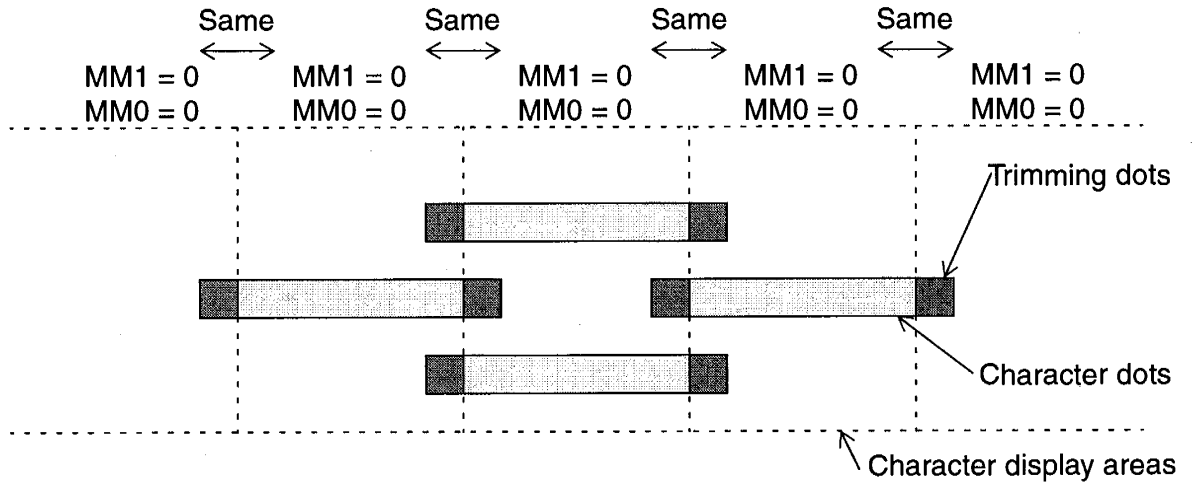
Blank character: In graphic display mode, a character displayed in a single color of the specified transparent or translucent color

(5) Code setting for sprite characters

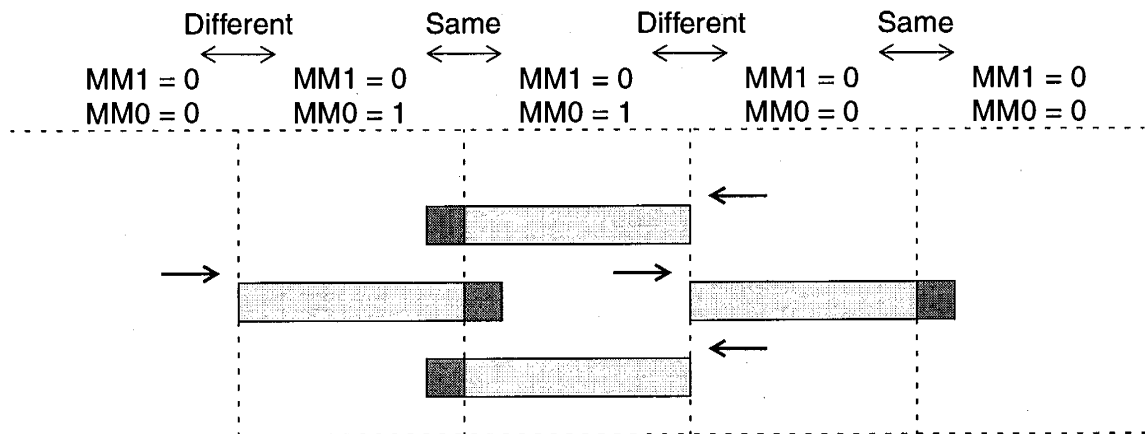
- For a sprite character consisting of one character, a character code can be selected from among character codes 00H to FFH for 256 different characters.
- For a sprite character consisting of two or four characters, use a character code (00H, 04H, 08H, 0CH, ... F8H, FCH) which is a multiple of 4 as the start code.

(6) Displaying character trimming dots in the adjacent character areas (extended display)

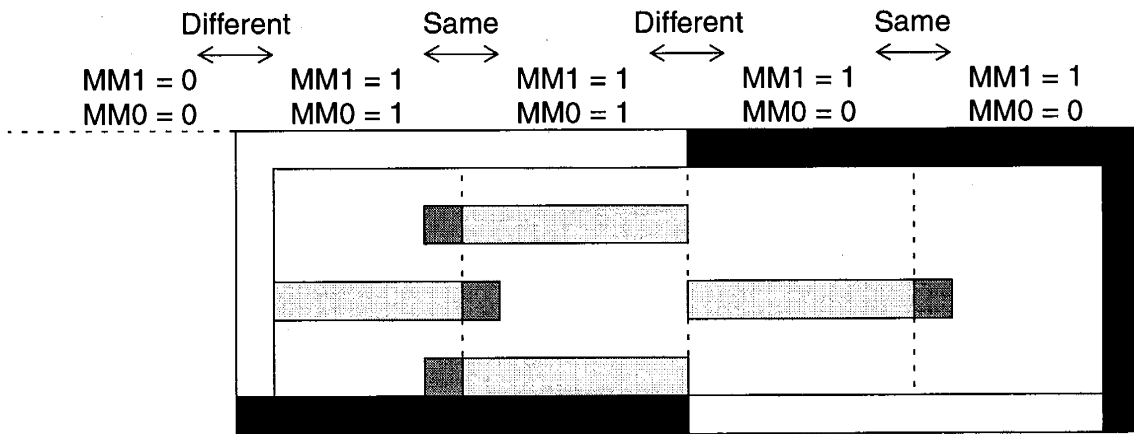
- Trimming dots for a character are extended beyond the character area, displayed in the right-side or left-side adjacent character area only when the character background types of the adjacent characters are the same.



- Trimming dots for a character are not extended to the right-side or left-side adjacent character area when the character background types of the adjacent characters are different.



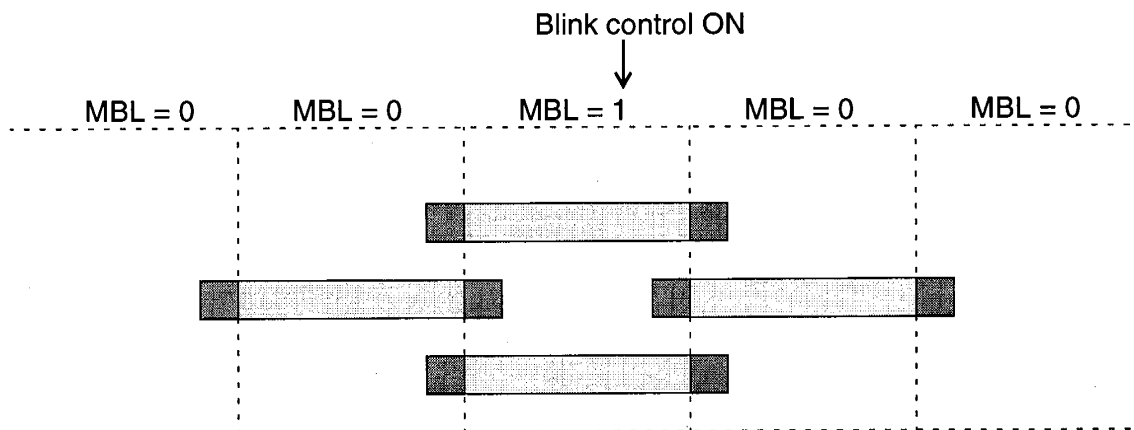
- The above rule applies also to character trimming dots in shaded background display mode. (Since shadow frames are displayed preferentially, the above rule applies to the boundary between two characters, at which the shadow frame is removed by succeeding character merge display.)



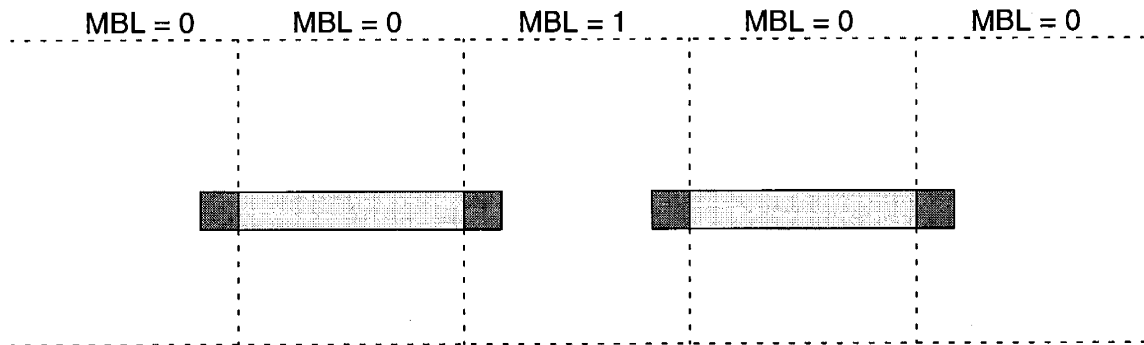
- Extended dot display in blink display mode

When dots for a character are extended to the adjacent character area, the dots blink if the character has been set as a blinking character. (The illustrations below assume the same type of character backgrounds.)

- On during blinking



■ Off during blinking



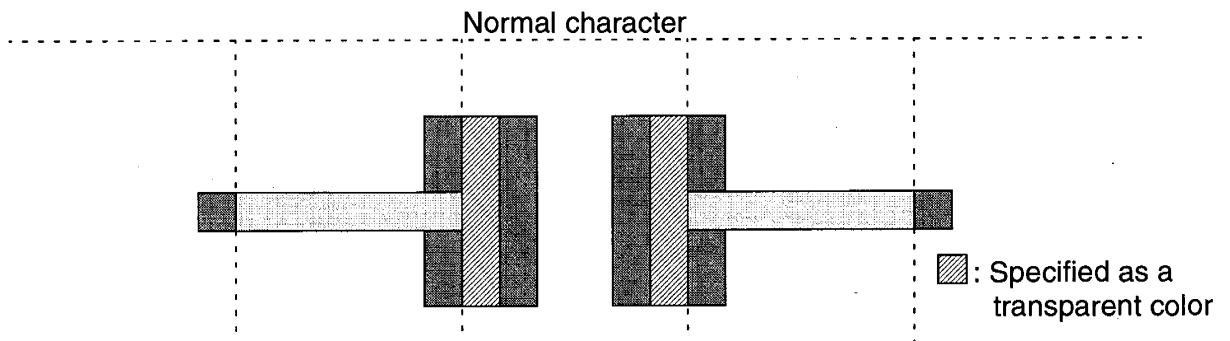
• Extended dot display in transparent/translucent color display mode

(Since transparent color display and translucent color display are the same in operation except the VOB2 pin, the description below covers only transparent color display for convenience.)

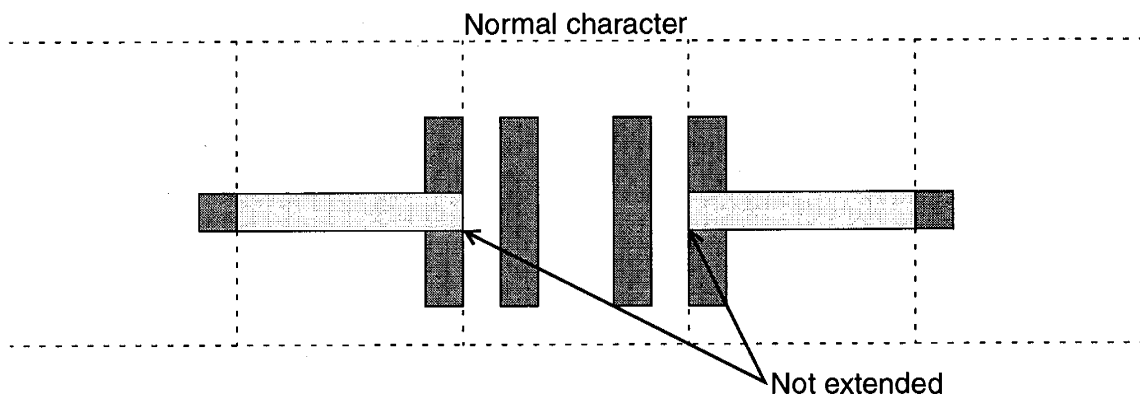
When normal character dots or graphic character dots exist at extended dots, usually, the character dots are displayed preferentially. If the color of these displayed dots (positions) is specified as a transparent color, the extended dots are handled as shown below.

(The illustrations below assume the same type of character backgrounds.)

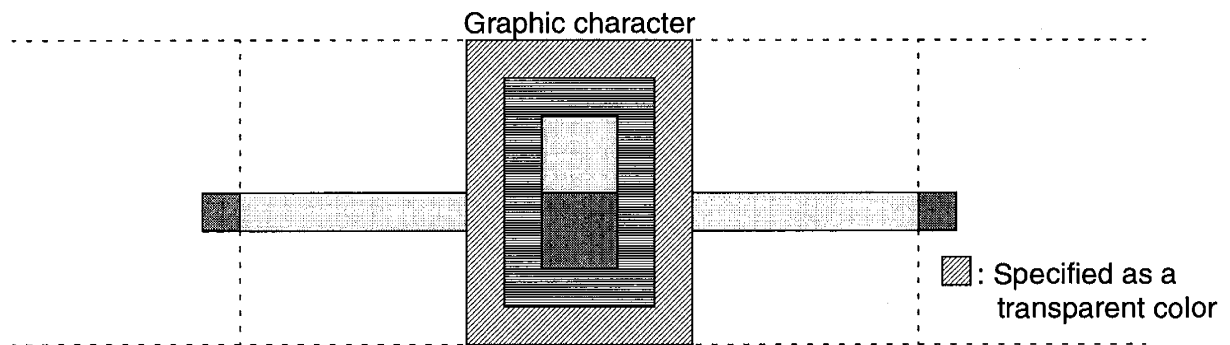
■ Specifying the color of preferentially displayed normal character dots as a transparent color



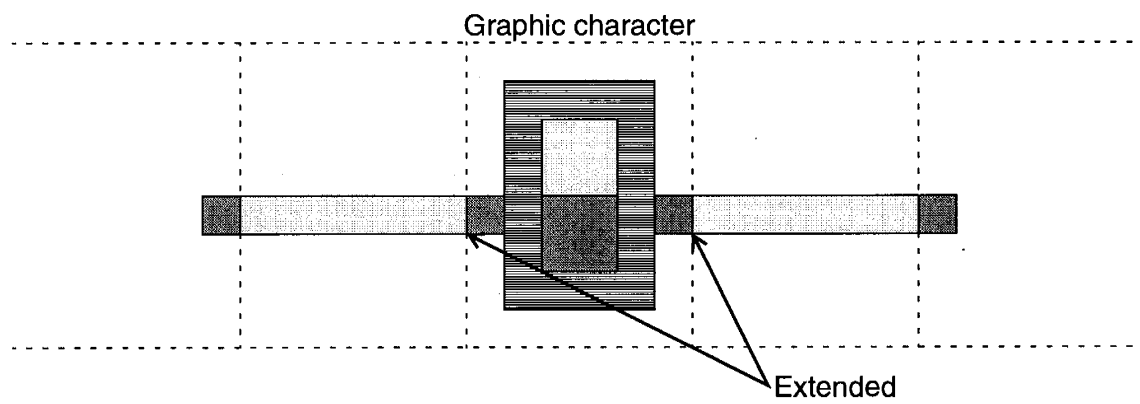
↓ Transparent color control ON



- Specifying the color of preferentially displayed graphic character dots dots as a transparent color



↓ Transparent color control ON



6.5 Notes on Graphic Character Design

This section summarizes notes on designing graphic characters.

(1) Setting a transparent color

To display an arbitrary shape of a graphic, design the graphic taking account of the use of one of 16 colors as a transparent color.

When a normal character is displayed with no character background specified, the dot-less portions of the character area appear transparent automatically (with a void background), requiring no special attention to the transparent color.

If you omit specifying a transparent color when handling a graphic character, however, the entire rectangle used as the character area is filled with dots, completely masking the background.

When designing a graphic character, therefore, determine a transparent color in advance and specify that color for those portions which you want look transparent.

The transparent color is set for each screen; it takes effect on the main screen, screen background characters, screen background color, and all colors in sprite characters.

(2) Setting a blank character as a graphic character

By setting a blank character as a graphic character, you can turn sprite display off with bit SDS (sprite display on/off control bit) set to on or turn screen background character display off with bit PDS (screen background character display on/off control bit) set to on.

To create a blank character as a graphic character, set the color specified in advance as a transparent color for the entire rectangular character area.

(3) Graphic character size

- Graphic characters which can be displayed on the main screen are limited to the L or S size. It is prohibited to display those in the M size.
- Sprite characters and screen background characters can be displayed only in the L size.

6.6 Notes on Loop Filter Design

6.6.1 Notes on designing a loop filter

(1) Notes on board design

The wiring for connecting the CPOUT pin, loop filter, and VCOIN pin must be minimized. The loop filter must be enclosed by analog lands to isolate it from digital circuits as possible to prevent it from being affected by digital noise.

(2) Input HSYNC

The PLL in this IC generates a dot clock based on the leading edge of the input HSYNC pulse. Pay attention to the following points:

- The input HSYNC cycle must be equalized even in the vicinity of the VSYNC pulse interval. Otherwise, synchronization cannot be maintained, causing distortion in display.
- The undershoot and overshoot of the input HSYNC pulse must be minimized for smooth transition.

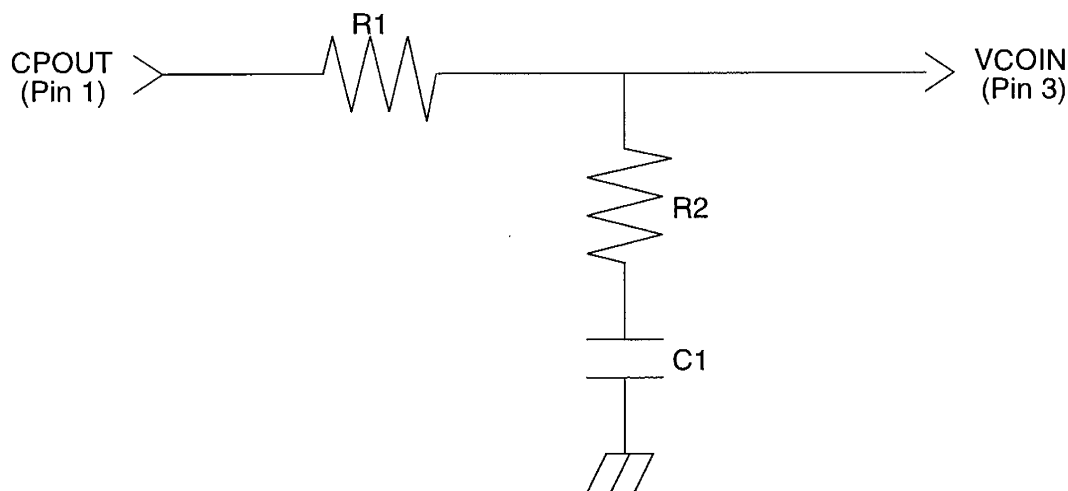
(3) Tips for better loop filter design

When designing the loop filter for a PLL, follow the following typical key points:

- Stable PLL loop
- Short lock-up time
- Low phase noise

Note that decreasing the time constant of the loop filter increases phase noise while shortening the lock-up time. This is because it widens the band of the loop filter. In contrast, increasing the time constant of the loop filter increases the lock-up time while reducing phase noise. These two opposite characteristics must be reconciled to implement the target specification. Use the following examples for your reference to determine the filter constant. You will need fine adjustment with your set.

6.6.2 Obtaining the time constant of the loop filter (lag-lead filter) for the MB90096



The filter constant can be obtained generally from the following equations:

$$R1 = \frac{1}{C1} \left\langle \frac{K\phi K_v}{N\omega_n^2} - \frac{2\zeta}{\omega_n} + \frac{N}{K\phi K_v} \right\rangle$$

$$R2 = \frac{1}{C1} \left\langle \frac{2\zeta}{\omega_n} - \frac{N}{K\phi K_v} \right\rangle$$

- Conversion gain ($K\phi$) of the phase comparator of the MB90096

$$K\phi = \frac{1}{2\pi} \times \frac{(V_{OH} - V_{OL})}{2} \div \frac{3 - 0}{4\pi} \div 0.24$$

- VCO conversion gain (K_v)

The VCO characteristic of the MB90096 is approximately:

$$K_v = 2\pi \times 100 \text{ (MHz/V)} \div 6.28 \times 10^8$$

- Divide ratio (N)

$$N = \frac{\text{Dot clock frequency}}{\text{HSYNC frequency}} \times (\text{Prescaler set value})$$

- Example for NTSC: HSYNC frequency = 15.7 kHz

$$\text{Dot clock frequency} = 15 \text{ MHz}$$

$$N = \frac{15 \text{ MHz}}{15.7 \text{ kHz}} \times [\text{Prescaler set value: DP0} = 1, \text{DP1} = 1] \\ \div 7.6 \times 10^3$$

- Example for VGA: HSYNC frequency = 31.5 kHz

$$\text{Dot clock frequency} = 30 \text{ MHz}$$

$$N = \frac{30 \text{ MHz}}{31.5 \text{ kHz}} \times [\text{Prescaler set value: DP0} = 0, \text{DP1} = 1] \\ \div 3.8 \times 10^3$$

- Natural angular frequency (ω_n), attenuation constant (ζ)

Select ω_n and ζ from the indicial response of the PLL.

Typically, select: $\zeta = 0.7$, $\omega_n \times t = 4.5$ (t: Lock-up time)

The lock-up time assumes the vertical blanking interval for each scan as about 10 H.

- Example for NTSC

$$10 \times 63.5 \mu\text{s} = 0.635 \text{ ms} > 0.5 \text{ ms} = t \\ \omega_n = 4.5/0.5 \text{ ms} = 9.0 \times 10^3$$

- Example for VGA

$$10 \times 31.7 \mu\text{s} = 0.317 \text{ ms} > 0.3 \text{ ms} = t \\ \omega_n = 4.5/0.3 \text{ ms} = 15.0 \times 10^3$$

■ Actual calculation examples (for NTSC)

$$R1 = \frac{1}{C1} \left\langle \frac{K\phi K_V}{N\omega n^2} - \frac{2\zeta}{\omega n} + \frac{N}{K\phi K_V} \right\rangle$$

(Assume C1 = 1 μ.)

$$= \frac{1}{1\mu} \left\langle \frac{0.24 \times 6.28 \times 10^8}{7.6 \times 10^3 \times (9.0 \times 10^3)^2} - \frac{2 \times 0.7}{9.0 \times 10^3} + \frac{7.6 \times 10^3}{0.24 \times 6.28 \times 10^8} \right\rangle$$

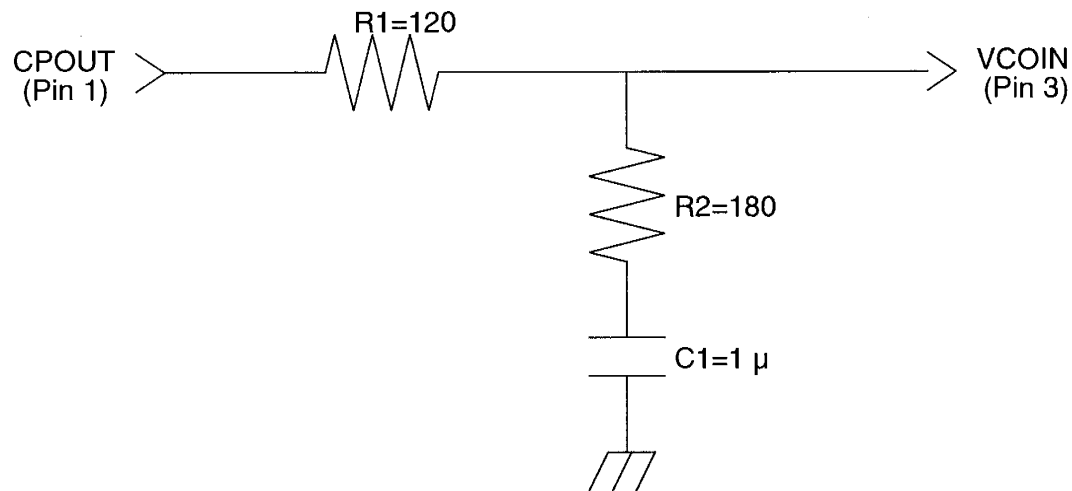
$$\approx 10^6 \times \langle 2.45 \times 10^{-4} - 1.56 \times 10^{-4} + 5.04 \times 10^{-5} \rangle \approx 139$$

$$R2 = \frac{1}{C1} \left\langle \frac{2\zeta}{\omega n} - \frac{N}{K\phi K_V} \right\rangle$$

$$\approx 10^6 \times \langle 2.45 \times 10^{-4} - 5.04 \times 10^{-5} \rangle \approx 195$$

From the series of E criterion numerals, R1 and R2 are approximately as follows:

R1 = 139 Ω ⇒ 120 Ω, R2 = 195 Ω ⇒ 180 Ω



■ Actual calculation examples (for VGA)

$$R1 = \frac{1}{C1} \left\langle \frac{K\phi K_v}{N\omega_n^2} - \frac{2\zeta}{\omega_n} + \frac{N}{K\phi K_v} \right\rangle$$

(Assume C1 = 1 μ.)

$$= \frac{1}{1\mu} \left\langle \frac{0.24 \times 6.28 \times 10^8}{3.8 \times 10^3 \times (15 \times 10^3)^2} - \frac{2 \times 0.7}{15 \times 10^3} + \frac{3.8 \times 10^3}{0.24 \times 6.28 \times 10^8} \right\rangle$$

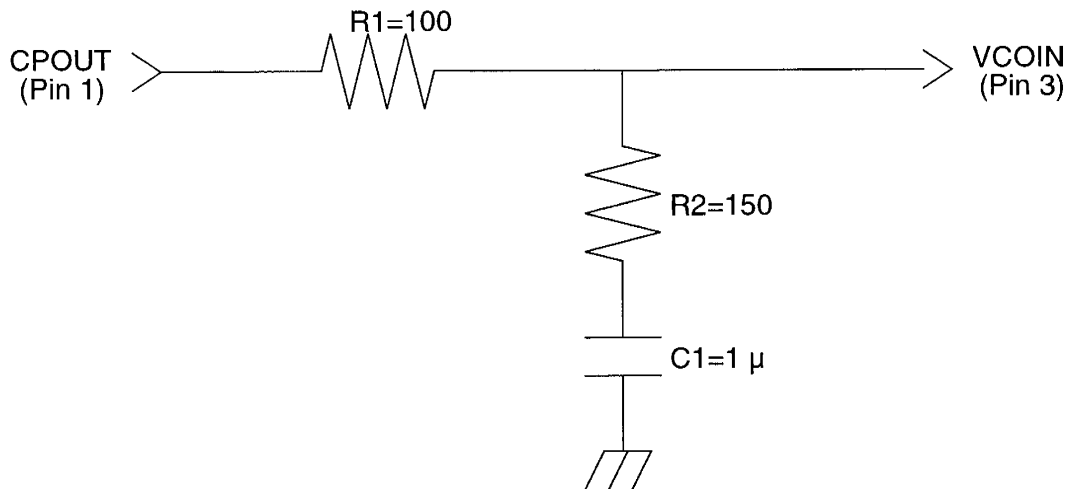
$$\approx 10^6 \times \langle 1.76 \times 10^{-4} - 9.33 \times 10^{-5} + 2.52 \times 10^{-5} \rangle \approx 108$$

$$R2 = \frac{1}{C1} \left\langle \frac{2\zeta}{\omega_n} - \frac{N}{K\phi K_v} \right\rangle$$

$$\approx 10^6 \times \langle 1.76 \times 10^{-4} - 2.52 \times 10^{-5} \rangle \approx 151$$

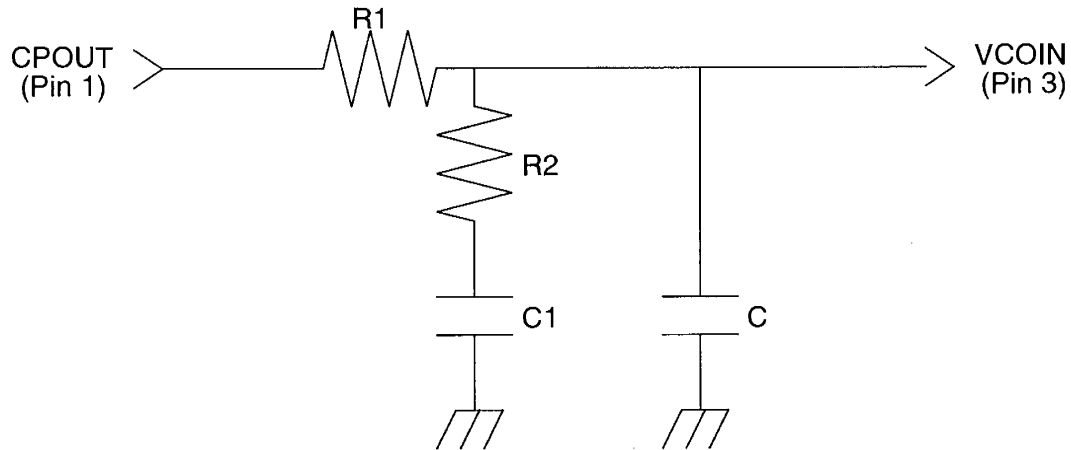
From the series of E criterion numerals, R1 and R2 are approximately as follows:

$$R1 = 108 \, \Omega \Rightarrow 100 \, \Omega, \quad R2 = 151 \, \Omega \Rightarrow 150 \, \Omega$$

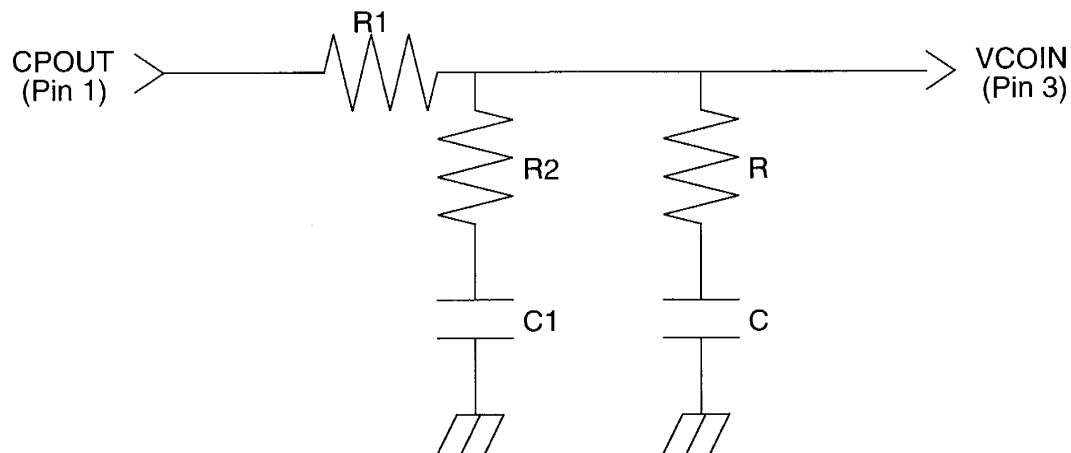


From the above calculation, determine the basic filter configuration. If distortion or jitter occurs, adding a CR as shown on the next page may suppress it.

(1) Attach capacitor C.



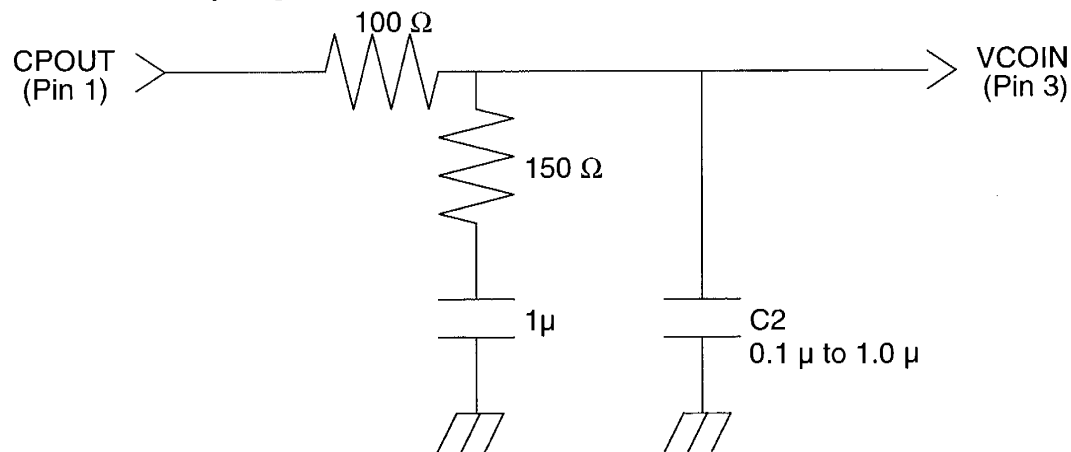
(2) Attach C and R.



The combination of (1) and (2) may be effective.

[Reference]

By adjusting the C2 value with the RC value fixed as shown below, the Fujitsu evaluation board can also support horizontal sync signals between about 15 kHz (NTSC) and about 80 kHz (SVGA mode on the PC).



Perform adjustment as above until desired display is implemented in a typical environment (root temperature, $V_{cc} = 5\text{ V}$). After that, follow Section 6.6.3 “Evaluating the loop filter” on the next page to evaluate and adjust the production set for margin operation.

6.6.3 Evaluating the loop filter

After determining the basic loop filter configuration in the previous section, evaluate and adjust the actual user set.

Check the following items during evaluation and adjustment:

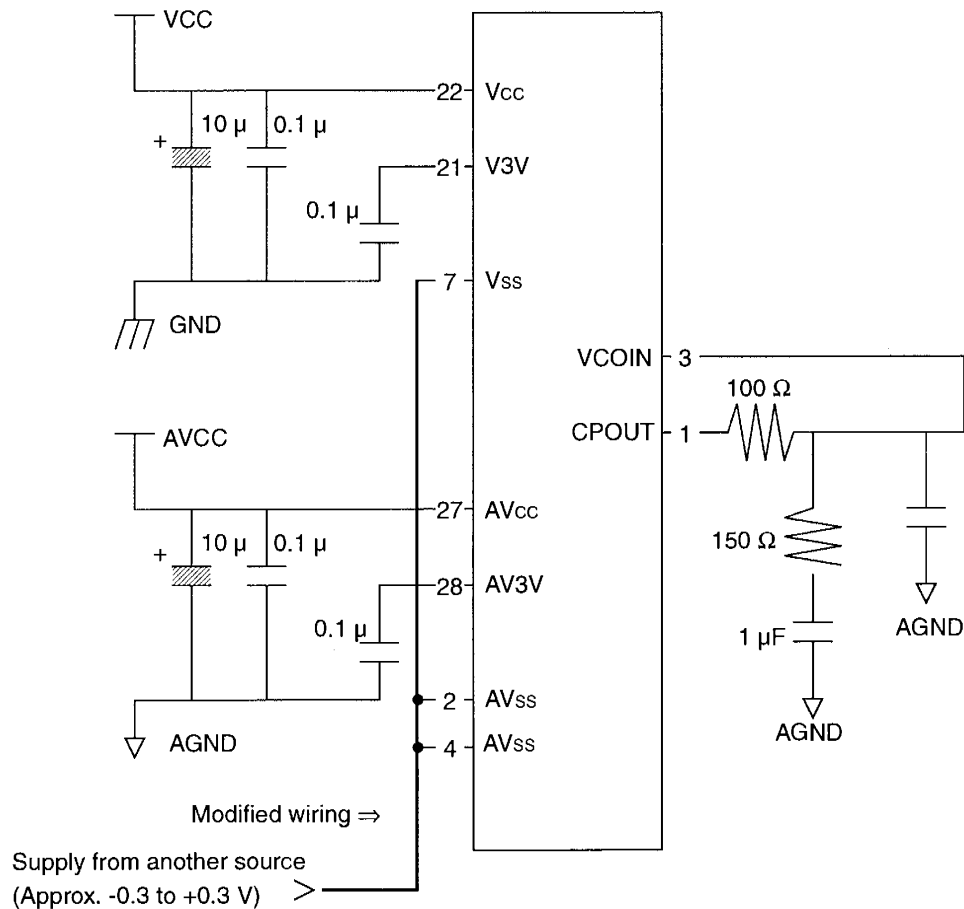
- (1) Manufacturing dispersion of the MB90096
- (2) User set environment (voltage and temperature) ranges

(1) Evaluating the loop filter considering the manufacturing dispersion of the MB90096

The manufacturing dispersion of the MB90096 can be simulated by changing the voltage applied to the Vss and AVss pins on the current sample available to you.

Only for this evaluation, modify your set so that the voltage (Vss voltage) applied to the Vss and AVss pins on the MB90096.

MB90096 (Power supply circuit)



Circuit for evaluating MB90096 manufacturing variation

[Evaluation procedure]

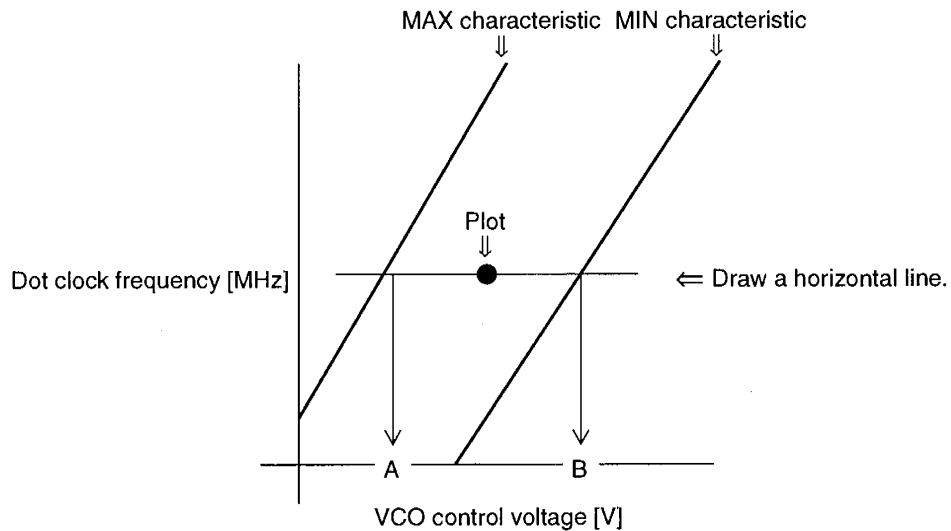
- (1) Use the MB90096 provided as a sample to measure the dot clock frequency (at the DOCKO pin) and the VCO control voltage (at the VCOIN pin) during display operation in the standard environment ($T_a = 25\text{ }^{\circ}\text{C}$, $V_{cc} = AV_{cc} = 5.0\text{ V}$, V_{ss} voltage = 0 V).

For dot clock output, set the DO bit of command 11-2 to "1".

Plot the results of measurement as on the graph (VCO-MIN/MAX characteristics) as shown in step 2) below.

Note that the values on the vertical axis vary depending on the prescaler settings (command 11-2: bits DP1 and DP0).

- (2) Draw a horizontal line from the point plotted on the graph to the two bold lines (MAX/MIN characteristics) to obtain the control voltages (A, B).



- (3) Change the V_{ss} voltage to the negative side to measure the V_{ss} voltage at the point at which the VCOIN pin voltage becomes "A". The measured voltage is the V_{ss} voltage at which the simulated MAX characteristic of VCO can be obtained.
- (4) Change the V_{ss} voltage to the positive side to measure the V_{ss} voltage at the point at which the VCOIN pin voltage becomes "B". The measured voltage is the V_{ss} voltage at which the simulated MIN characteristic of VCO can be obtained.

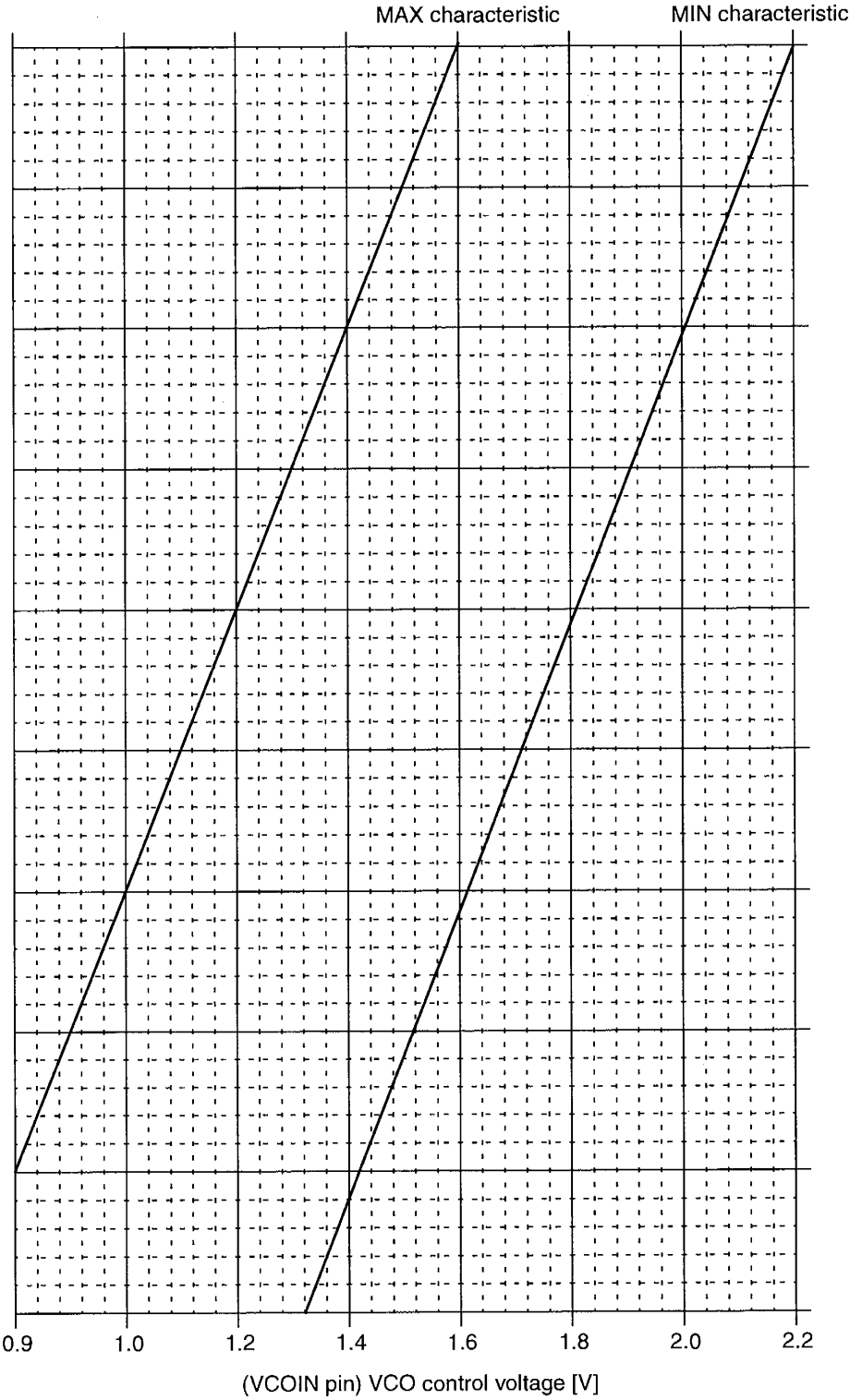
* Usually, the V_{ss} voltage can be measured almost between -0.4 to $+0.4\text{ V}$. If the voltage at the VCOIN pin remains the same when the V_{ss} voltage is changed in that range, The modified wiring may be erroneous. Check the modified wiring.

VCO-MIN/MAX Characteristics

Dot clock frequency [MHz]
(DOCKO pin)

Prescaler set value

DP1	0	0	1	1
DP0	0	1	0	1
	—	60	30	15
	—	56	28	14
	—	52	26	13
	96	48	24	12
	88	44	22	11
	80	40	20	10
	72	36	18	9
	64	32	16	8
	56	28	14	7
	48	24	12	6

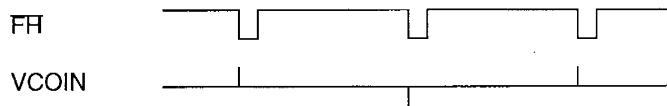


Adjust the loop filter value by combining the simulated MAX/MIN characteristics and the environmental condition ranges of your set so that the best display state can be obtained.

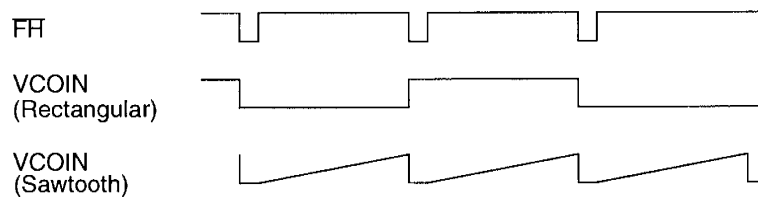
Before evaluating the display state, remove instruments such as a probe connected to measure the VCOIN voltage.

Check whether the VCOIN pin waveform is as follows to make sure that the PLL has been locked normally in the best display state.

- When the PLL has been locked normally, a very narrow pulse (several nanoseconds) is generated in synchronization with the rise of the $\overline{\text{FH}}$ pin output and becomes stable at almost a constant voltage level.



- If the PLL is abnormal, a rectangular or sawtooth waveform appears in the *FH cycle.

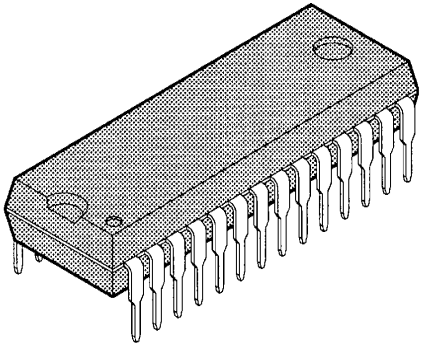


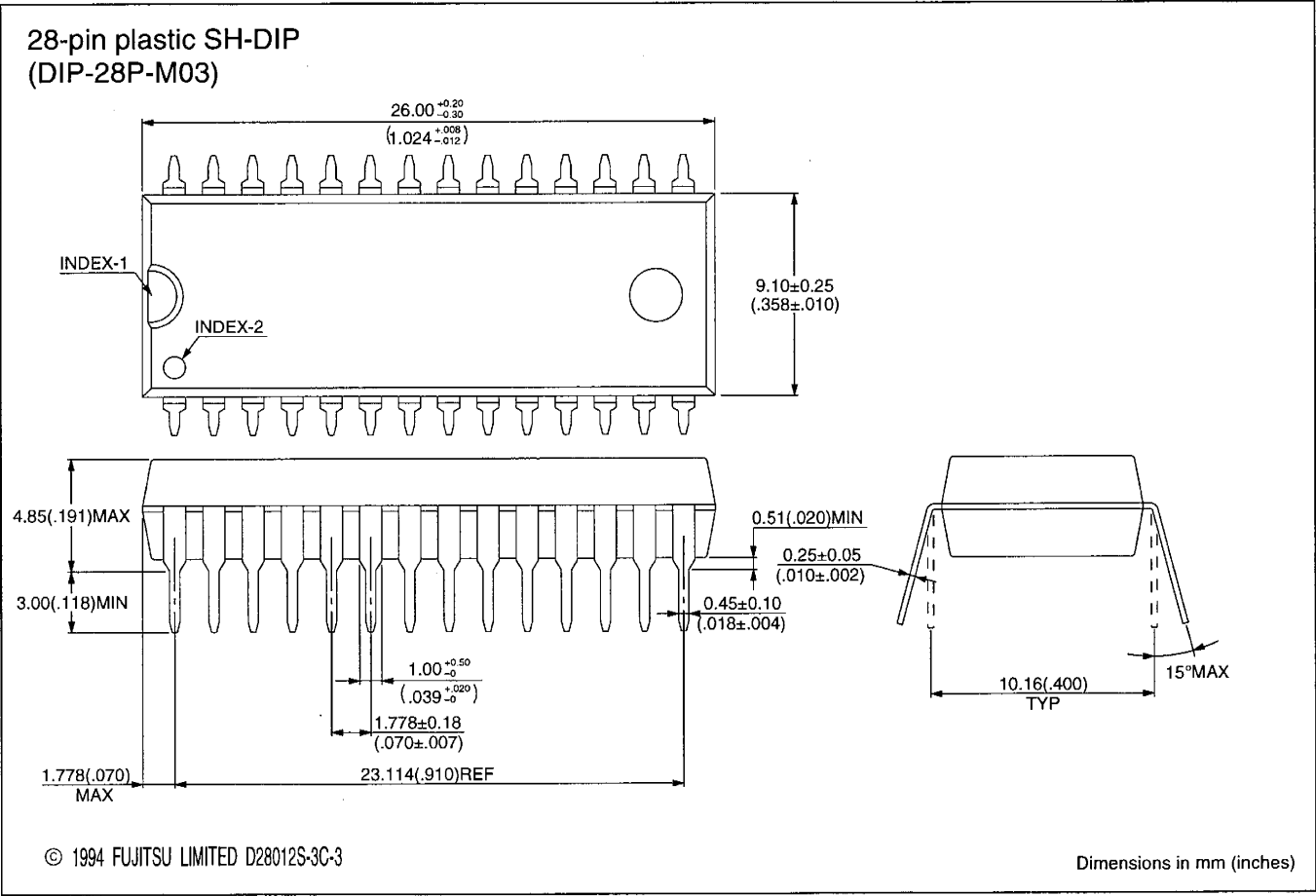
APPENDIX

Shrink dual in-line package28 pin plastic

DIP-28P-M03

EIAJ code: SDIP028-P-0400-1

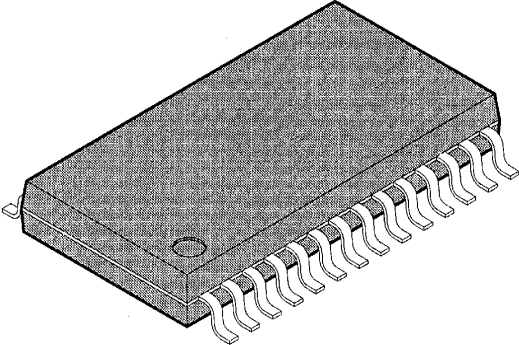
<div>28-pin plastic SH-DIP</div>  <div>(DIP-28P-M03)</div>	Lead pitch	70 mil
	Low profile	400 mil
	Sealing type	Plastic molding



Shrink dual in-line package28 pin plastic

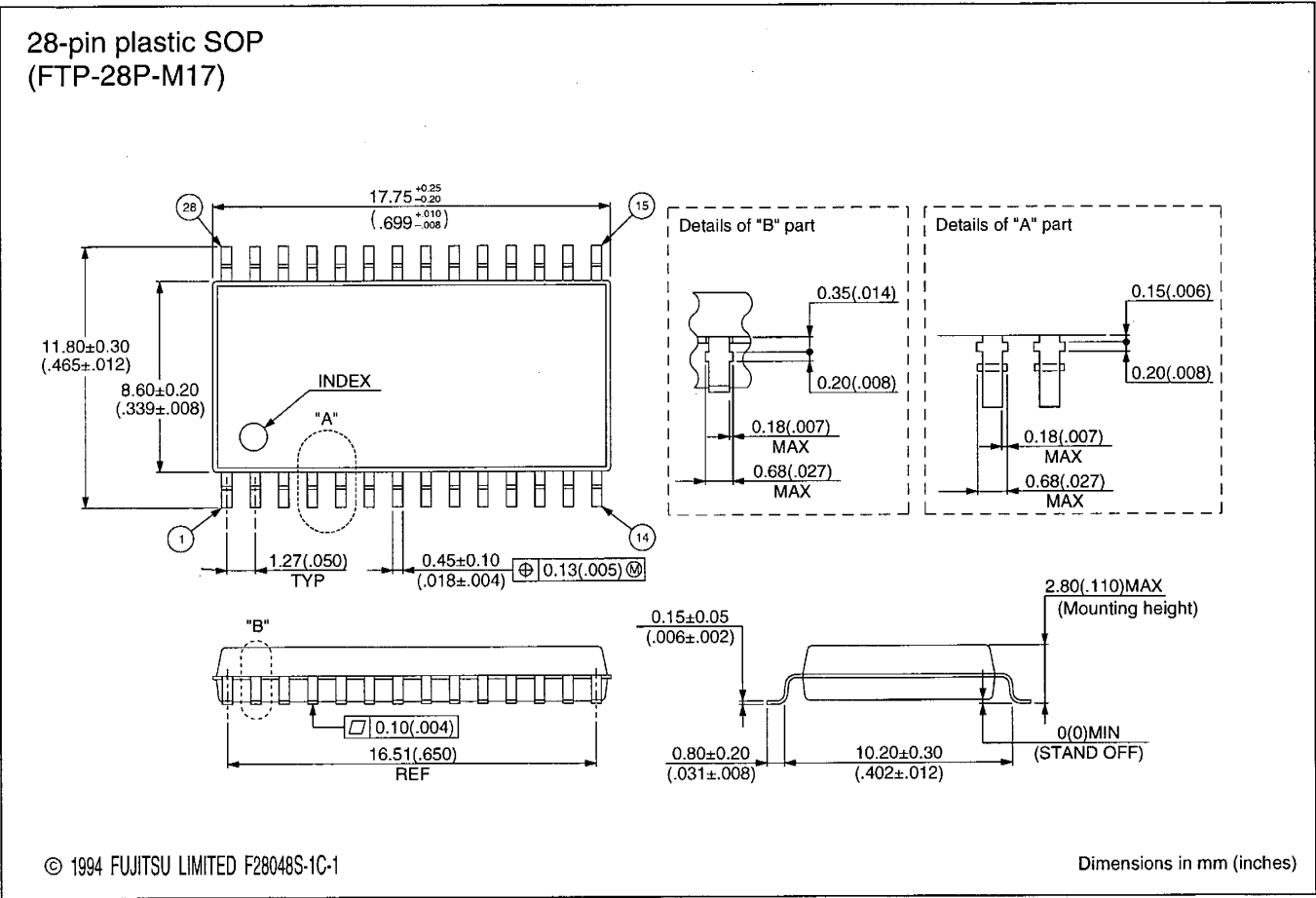
FTP-28P-M17

28-pin plastic SOP



(FTP-28P-M17)






























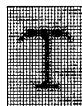








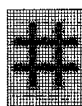

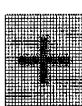
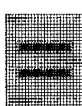









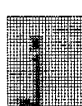

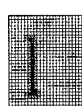







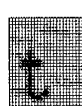


Lead pitch	50 mil
Nominal dimension	450 mil
Lead shape	Gull-wing
Sealing type	Plastic molding



_mb9001 - MB90096





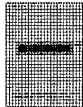
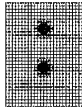


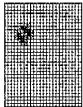
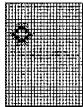

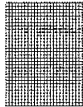







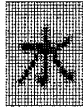






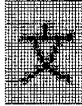



















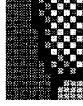
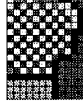



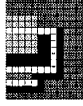

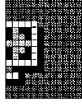
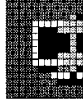

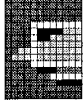
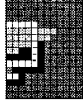
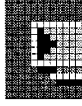
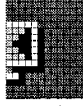
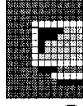
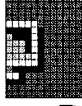


[Standard font (002)]

The characters shown below are actually displayed in color.

							
000	001	002	003	004	005	006	007
							
008	009	00A	00B	00C	00D	00E	00F
							
010	011	012	013	014	015	016	017
							
018	019	01A	01B	01C	01D	01E	01F
							
020	021	022	023	024	025	026	027
							
028	029	02A	02B	02C	02D	02E	02F
							
030	031	032	033	034	035	036	037
							
038	039	03A	03B	03C	03D	03E	03F

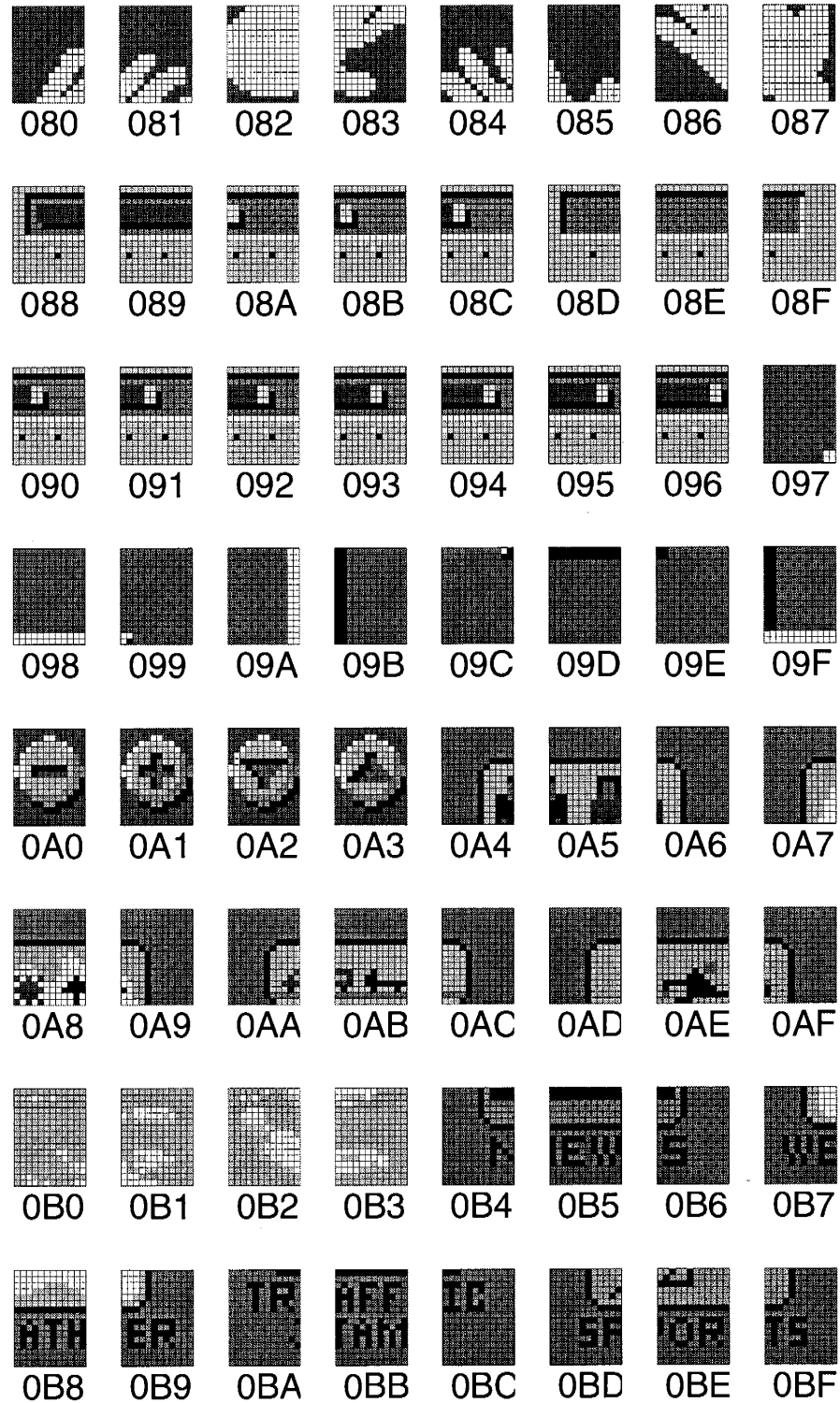
Printed character format 2

_mb900`1 - MB90096
[Standard font (002)]

							
040	041	042	043	044	045	046	047
							
048	049	04A	04B	04C	04D	04E	04F
							
050	051	052	053	054	055	056	057
							
058	059	05A	05B	05C	05D	05E	05F
							
060	061	062	063	064	065	066	067
							
068	069	06A	06B	06C	06D	06E	06F
							
070	071	072	073	074	075	076	077
							
078	079	07A	07B	07C	07D	07E	07F

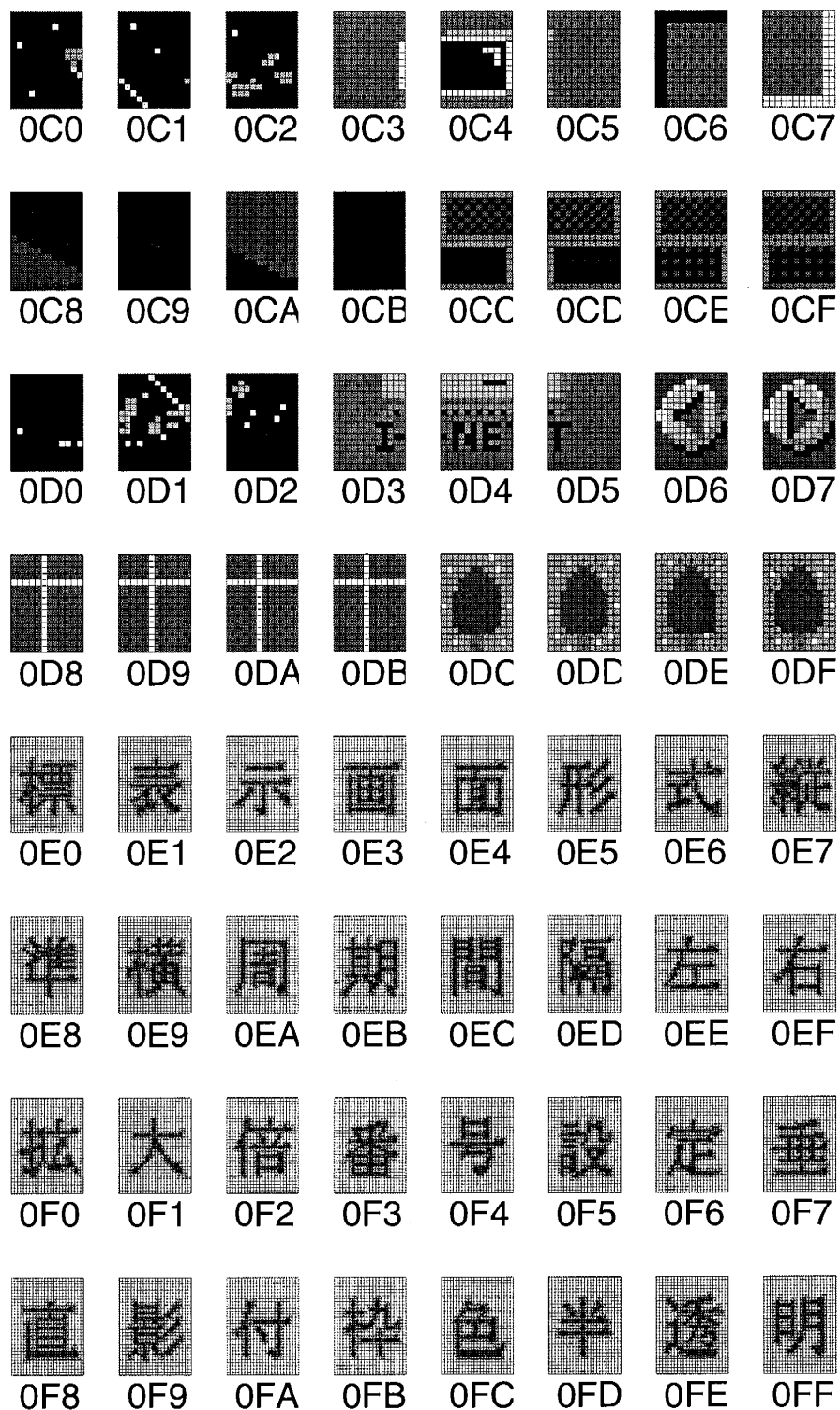
Printed character format 2

_mb9001 - MB90096
[Standard font (002)]



Printed character format 2

_mb900⁻1 - MB90096
[Standard font (002)]





















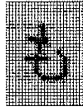










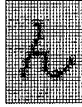



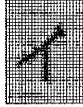


















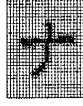

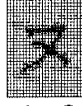
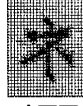








Printed character format 2

_mb900-1 - MB90096
[Standard font (002)]

0	1	2	3	4	5	6	7
100	101	102	103	104	105	106	107
8	9	A	B	C	D	E	F
108	109	10A	10B	10C	10D	10E	10F
G	H	I	J	K	L	M	N
110	111	112	113	114	115	116	117
O	P	Q	R	S	T	U	V
118	119	11A	11B	11C	11D	11E	11F
W	X	Y	Z	[]	x	+
120	121	122	123	124	125	126	127
-	/	:	AM	PM	-	.	*
128	129	12A	12B	12C	12D	12E	12F
あ	い	う	え	お	か	き	く
130	131	132	133	134	135	136	137
け	こ	さ	し	す	せ	そ	た
138	139	13A	13B	13C	13D	13E	13F











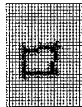

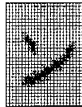






























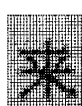








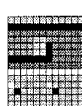
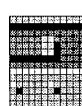


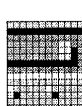



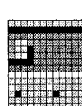


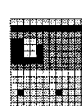
Printed character format 2

_mb900`1 - MB90096
[Standard font (002)]

							
140	141	142	143	144	145	146	147
							
148	149	14A	14B	14C	14D	14E	14F
							
150	151	152	153	154	155	156	157
							
158	159	15A	15B	15C	15D	15E	15F
							
160	161	162	163	164	165	166	167
							
168	169	16A	16B	16C	16D	16E	16F
							
170	171	172	173	174	175	176	177
							
178	179	17A	17B	17C	17D	17E	17F









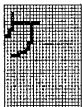
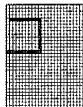



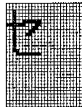






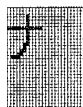

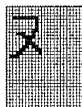





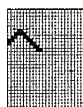


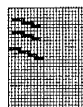




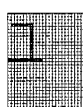
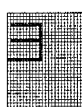



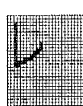
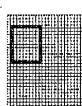
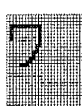

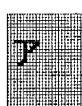
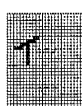

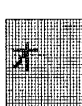
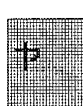

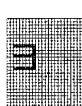

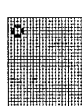
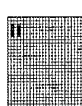

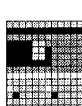

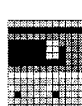
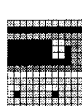


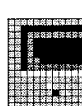

Printed character format 2

_mb900-1 - MB90096
[Standard font (002)]

							
180	181	182	183	184	185	186	187
							
188	189	18A	18B	18C	18D	18E	18F
							
190	191	192	193	194	195	196	197
							
198	199	19A	19B	19C	19D	19E	19F
							
1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7
							
1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF
							
1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7
							
1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF

Printed character

_mb900⁻1 - MB90096
[Standard font (002)]

							
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7
							
1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF
							
1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7
							
1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
							
1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7
							
1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF
							
1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7
							
1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF

Printed character format 2

AM32-10825-1E

FUJITSU SEMICONDUCTOR • ASSP MANUAL

On-screen Display Controller

ASSP for Screen Display Controller

MB90096

User's Manual

May 1998 the first edition

Published **FUJITSU LIMITED** Electronic Devices

Edited Technical Communication Dept.
