TC2xx hardware design guide

TriCore™ AURIX™ 32-bit microcontrollers

About this document

Scope and purpose

AURIX™ is an Infineon family of microcontrollers that focus on the needs of the automotive industry in terms of performance and safety. Its innovative multi-core architecture, based on up to three independent 32-bit TriCore™ CPUs, has been designed to meet the highest safety standards, while simultaneously significantly increasing performance.

This document explains basic hardware features and functions of the TC2xx devices in the AURIX™ family, and provides related hardware design guidelines for reaching the best performance.

Intended audience

Engineers who need to become familiar with the hardware design principles of TC2xx AURIX™ devices.

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1 Introduction

The AURIX™ TriCore™ enables systems to achieve the highest safety level up to ASIL-D. The multi-core architecture is designed to meet the highest safety standards (IEC61508/ISO26262), while scaling from low-cost to high performance devices.

The best cost-performance fit is offered by the wide range of flash, performance, and peripheral options available within the AURIX™ family. With performance of 133 MHz-6x300 MHz, advanced timer unit, totally flexible PWM generation and hardware input capture, Infineon SafeTcore library safety software, and many other features, the system benefits include:

- Scalability over flash, RAM and peripherals, offering an excellent cost-performance ratio.
- Flexible power supply concept to select from various power topologies to reduce power consumption and hardware system costs.
- The latest diverse lockstep technology.
- Secured high-speed communication: CAN FD, FlexRay, SPI and Ethernet.

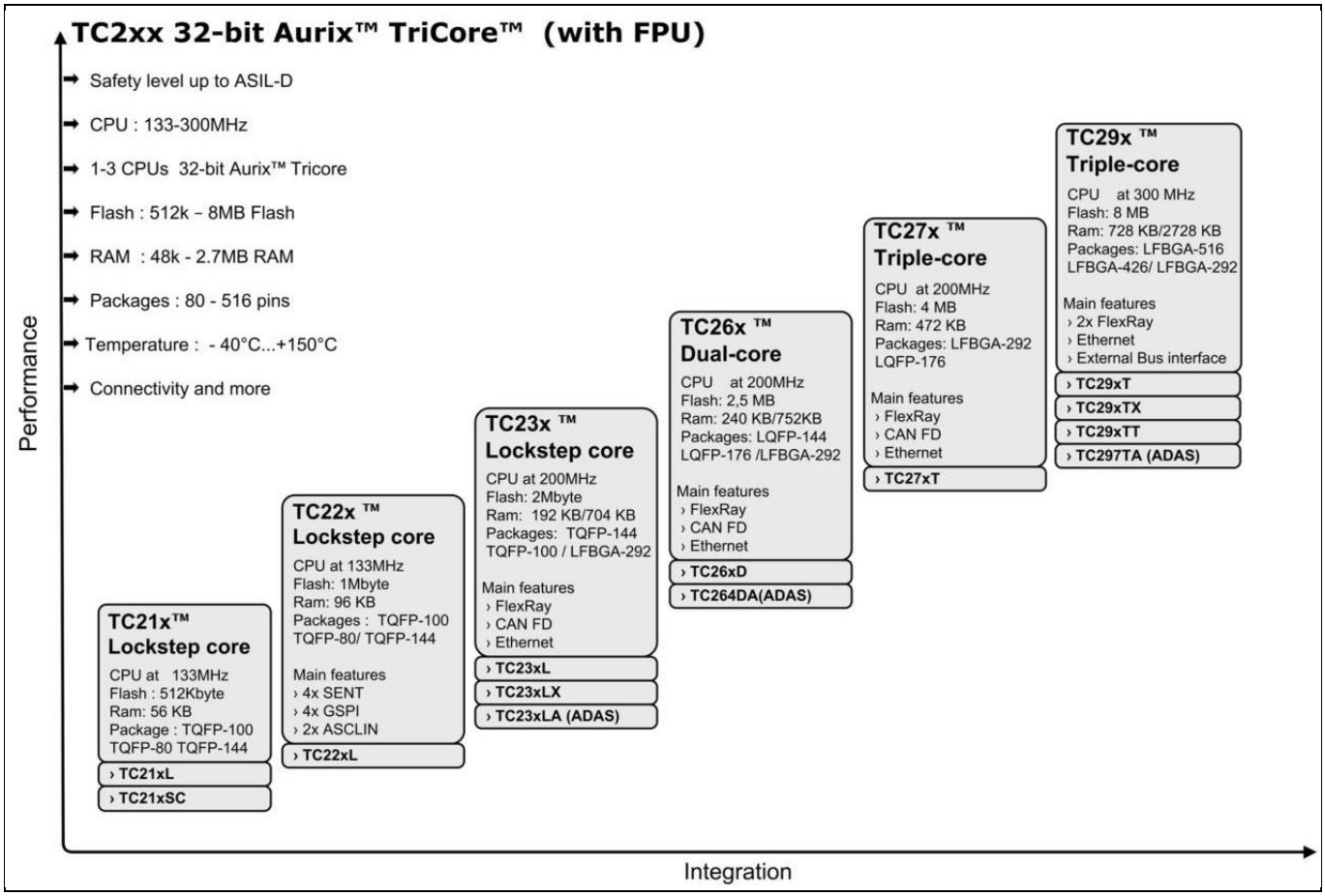


Figure 1 Overview of scalability in the AURIX™ TC2xx platform

2 Supply schemes

2.1 Single power supply

The AURIX™ products need only a single supply from which all internal voltages are generated by means of embedded voltage regulators EVR33 and EVR13.

The TLF35584 is a monolithic multi-voltage regulator for the AURIX™ product family. A nominal battery voltage is regulated to V_{LDO_QUC} = 5.0 or 3.3 Volts with a precision of ±2% through a buck boost pre-regulator and a LDO post-regulator for µC load currents up to 600 mA.

The ADC is supplied with a dedicated accurate reference supply V_{REF_QVR} = 5.0 Volts with a precision of ±1% for ADC load currents up to 150 mA.

The TLF35584 stand-by regulator V_{LDO_QST} = 5.0 or 3.3 Volts with a precision of ±2% supports standby current from 20 µA up to 10 mA. Therefore the combination may be used in applications which are permanently connected to V_{BAT}.

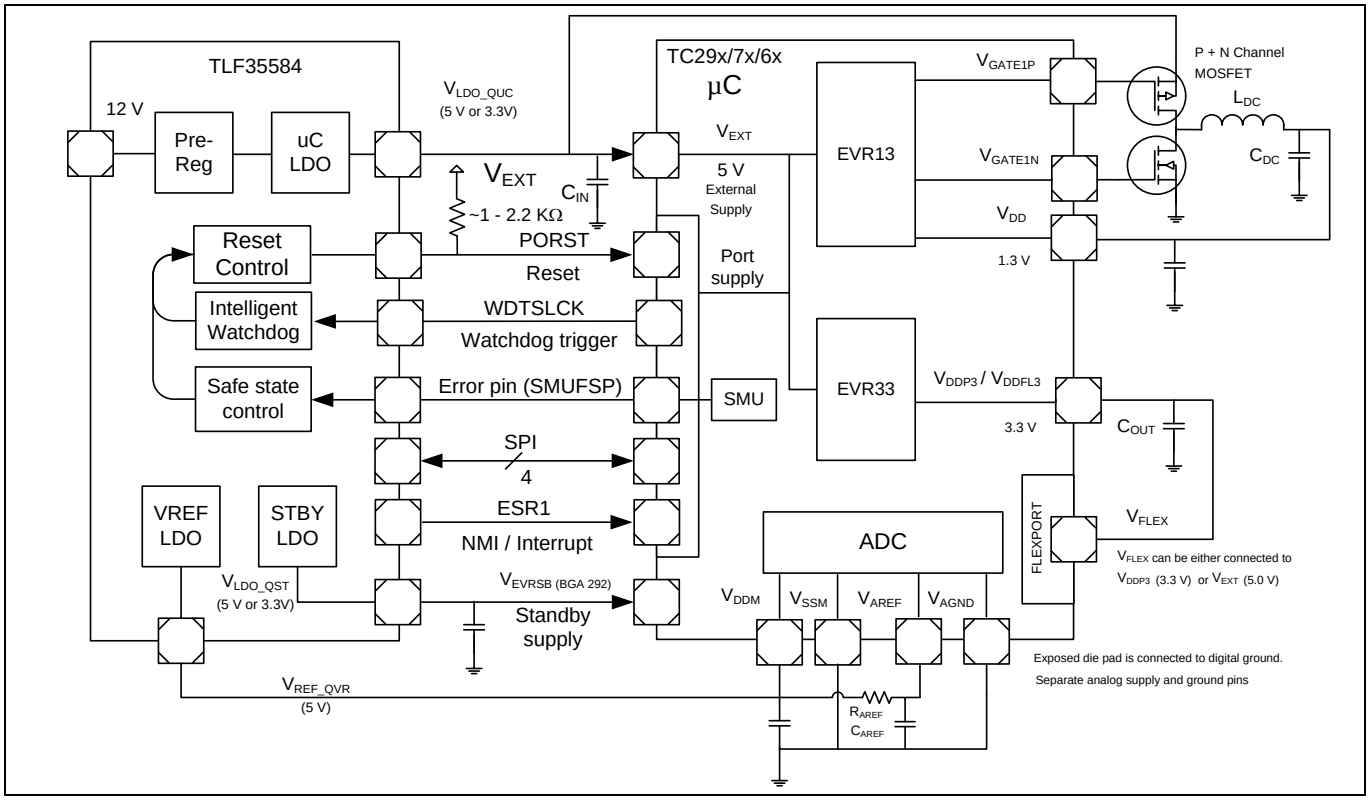


Figure 2 Single source power supply with TLF35584

Note: The ADC low noise supply regulator is standalone in most applications because of stricter noise filtering requirements. Generally it may not be present in the system, and therefore the V_{DDM} domain is supplied from the same supply source as the V_{EXT} domain with reduced ADC performance.

2.2 Dual power supply or multi-rail power supply schemes

It is possible to connect an additional switch-mode post regulator at pre-regulator output to realize an external 1.3V core supply voltage using TLF35584 dual-rail supply mode portrayed in the figure below.

Multi-rail topology is supported as well allowing all three voltage rails to be generated from external supply components. The voltage rails are:

- V_{EXT}=5V
- V_{DDP3}=3.3V
- V_{DD}=1.3V

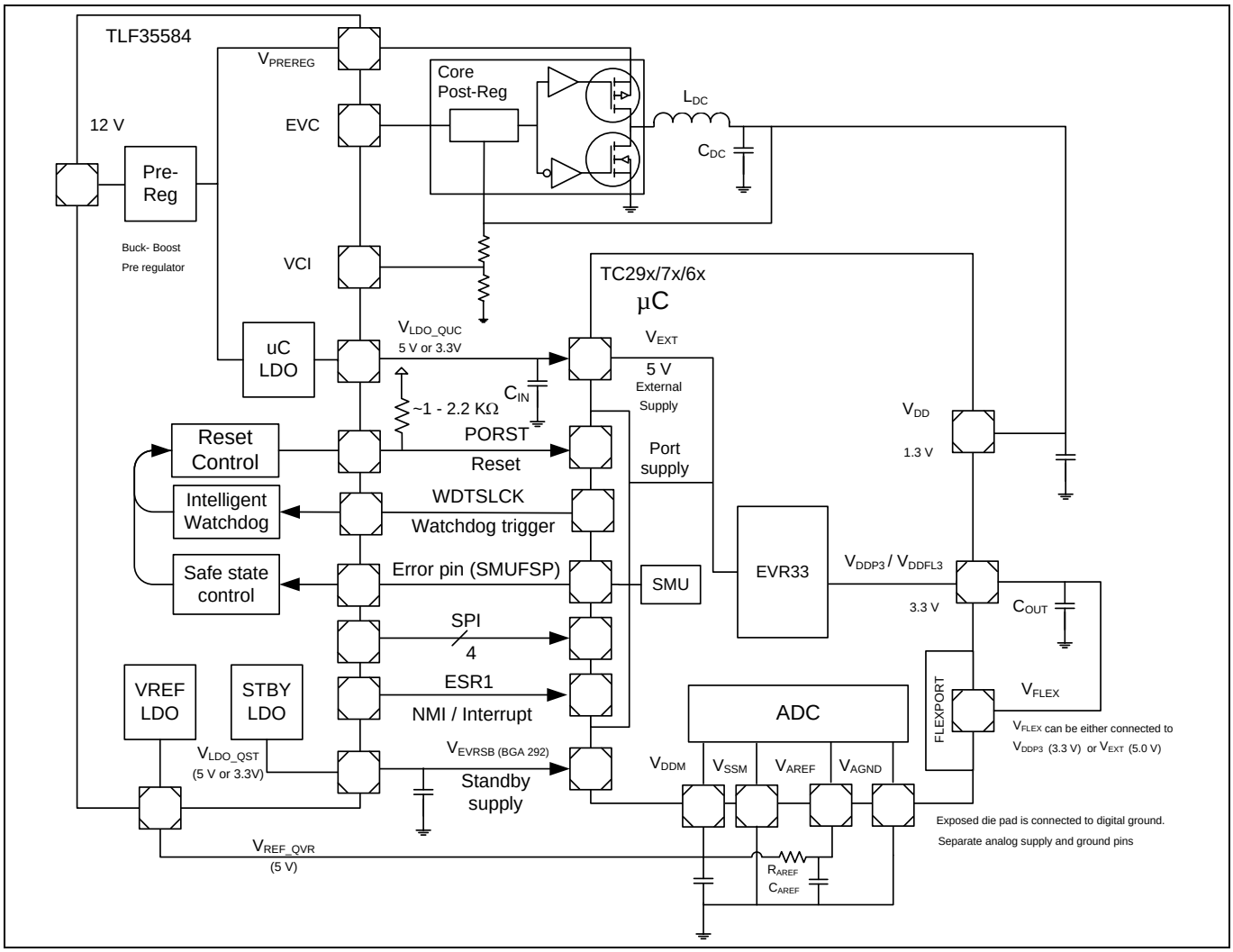


Figure 3 Dual source power supply with TLF35584

3 Basic pin configuration

For correct device operation care must be taken to connect the following pins correctly:

- Test pin (/TESTMODE)
- Debug pins (/TRST, TCK, TMS, TDO, TDI)
- Hardware configuration pins (HWCFG0, HWCFG1, HWCFG2, HWCFG3, HWCFG6, V_{GATExP})
- Reset / NMI pins (/PORST, /ESR0, /ESR1)
- Power supply pins (V_{EXT}, V_{DDP3}, V_{DDFL3}, V_{DD}, V_{DDM}, V_{AREF}, V_{SS}, V_{SSM}, V_{AGND})

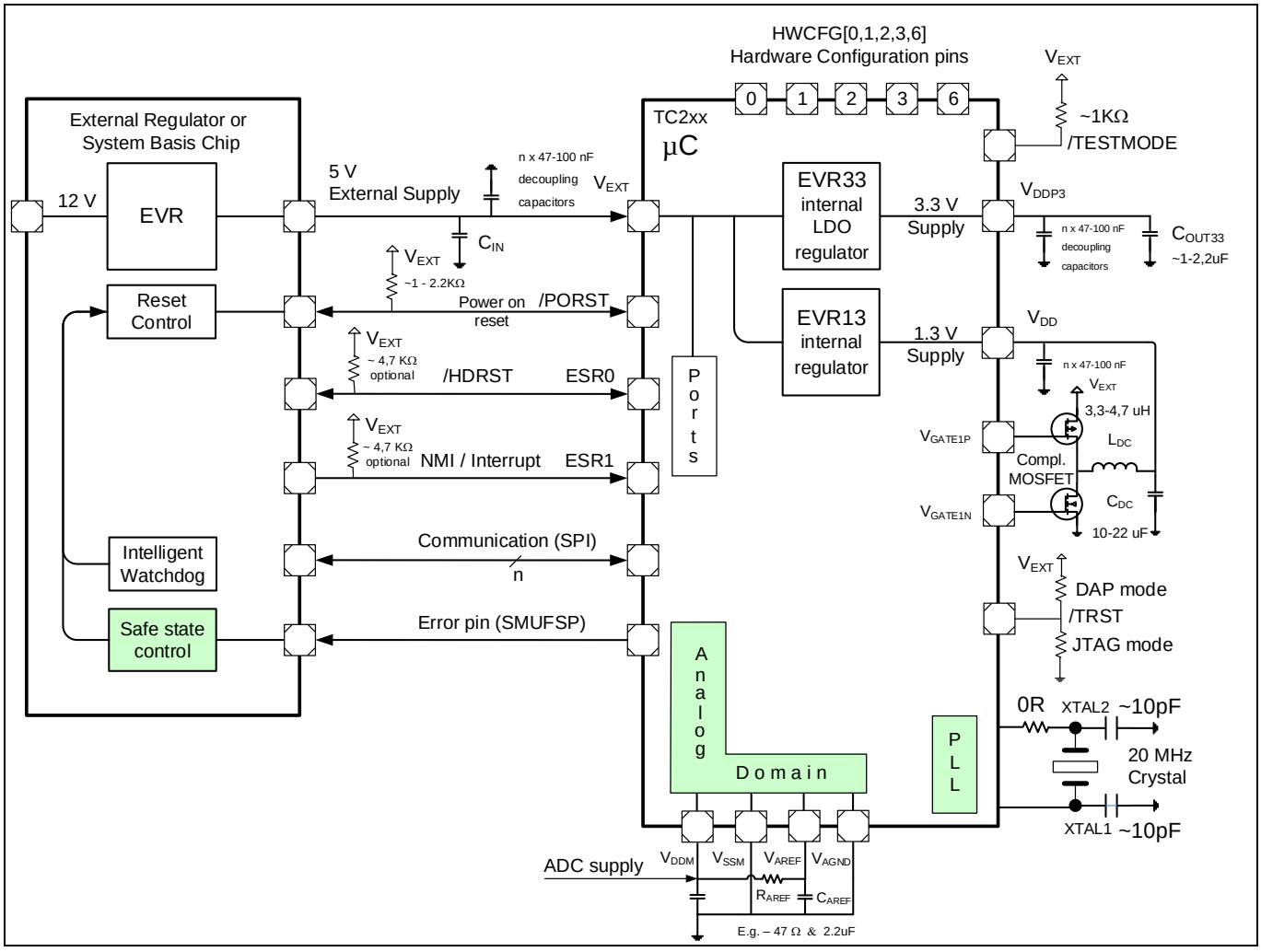


Figure 4 An example configuration; TC29x, TC27x, TC26x with 5V single supply

3.1 Supply pins and ranges

The table below lists all supply pins grouped by acceptable operational voltages ranges.

Note: It is important to note that not all supply pins are available in each device variant.

Table 1 Supply pins and ranges

Supply pin	Operational voltage range	Main functions
V_{EXT} V_{EVRSB} V_{FLEX} V_{DDM} V_{AREFx} V_{FLEXE}	2.97–5.50	• Source voltage for EVR13 & EVR33 regulators in 29x, 27x, 26x. I/O supplies which decides the I/O level in 29x, 27x, 26x. • Common standby supply pin • ADC supply and reference
V_{DDP3} V_{DDOSC3} V_{DDFL3} V_{EBU} V_{AGBT3}	2.97–3.63	• Source voltage for EVR13 regulator and I/O supply in 23x, 22x, 21x. • Flash, JTAG & P21 supply in case of 29x,27x,26x • HSCT and DTS supply Oscillator and PLL supply • Flash sense amplifier supply.
V_{DD} V_{DDOSC} V_{DDSB} V_{AGBT}	1.17– 1.43	• Main core supply. • Oscillator and PLL supply. • Emulation Device EMEM (Emulation memory) supply. • Supply for AGBT.

3.2 Hardware configuration pins

The Hardware configuration (HWCFG) pin functions are shown in the figure below.

Note: Not all of the listed HWCFG pins are present in the lower-end devices of the TC2xx family.

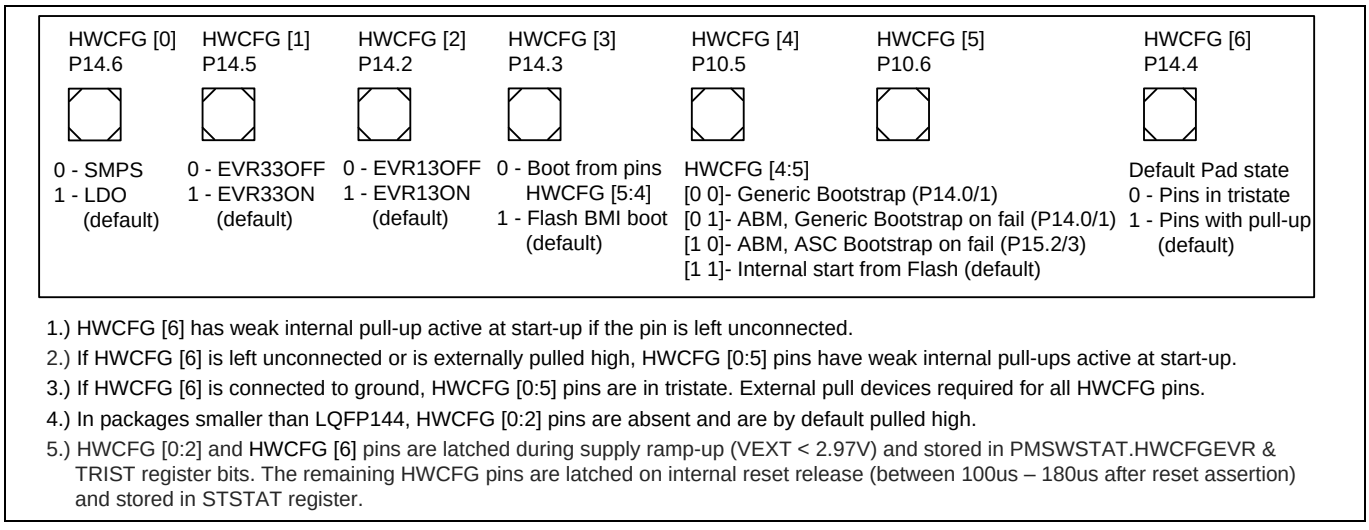


Figure 5 HWCFG pins and functions

These pins have weak internal pull-ups with a range of 30 – 105 µA.

In case an external pull-down is required, it is recommended that the value at the pin is lower than 0,8V or a resistor of ≤ 4.7K Ohm is used.

Table 2 HWCFGx example configuration

HWCFG pins	Example configuration
HWCFG [0:2]	• Tied to external pull-ups or pull-downs corresponding to supply mode
HWCFG [3]	• Pin may be used for application as Flash BMI boot is used. • Pin is ignored during boot as BMI.PINDIS is set (BMI.PINDIS=1).
HWCFG [4:5]	• Pins may be used for application as BMI index in Flash is used.
HWCFG [6]	• Tied to fixed external pull down (Tristate is selected as default mode)
V_{GATE1P}	• Shall be connected to ground in TC26x to select internal pass devices. • Shall be connected to the P channel MOSFET in case of EVR13 SMPS mode.
V_{GATE1N} /P32.0	• Shall be connected to the N channel MOSFET in case of EVR13 SMPS mode. • Otherwise is by default available as a port pin (P32.0).

3.3 Power supply related pins

The V_{GATEx} or V_{CAPx} pins are used by the EVR13 to drive external power components in either high-end or low-end devices of the AURIX™TC2xx family accordingly. The exact pin configuration and use should be checked in the device user manual.

Table 3 EVR13 output control pins

EVR13 output pins	Pin function
V_{GATE1P}	• Gate drive for P-channel MOSFET for SMPS EVR13 regulator. • Gate drive for P channel MOSFET pass device for LDO EVR13 regulator.
V_{GATE1N}	• Gate drive for N-channel MOSFET for SMPS EVR13 regulator.
V_{CAP0} V_{CAP1}	• Flying capacitor (1uF) terminals in switch capacitor EVR13 SMPS regulator in TC23x.

3.4 Test pin

The /TESTMODE pin is exclusively used for factory test modes after manufacture. In normal operation it shall be connected directly to V_{EXT} (Main external 5V or 3.3V supply) rail.

/TESTMODE pin has a weak internal pull-up which should be sufficient to ensure that the device does not enter the test state when the pin is left open. Nevertheless it is recommended to connect it externally with a stronger pull-up (~1- 4,7 K). No external connection to debug connectors is required.

/TESTMODE pin is present in all devices across all packages without exception.

3.5 Debug pins

The default reset behavior of the debug pins is as described in the table below.

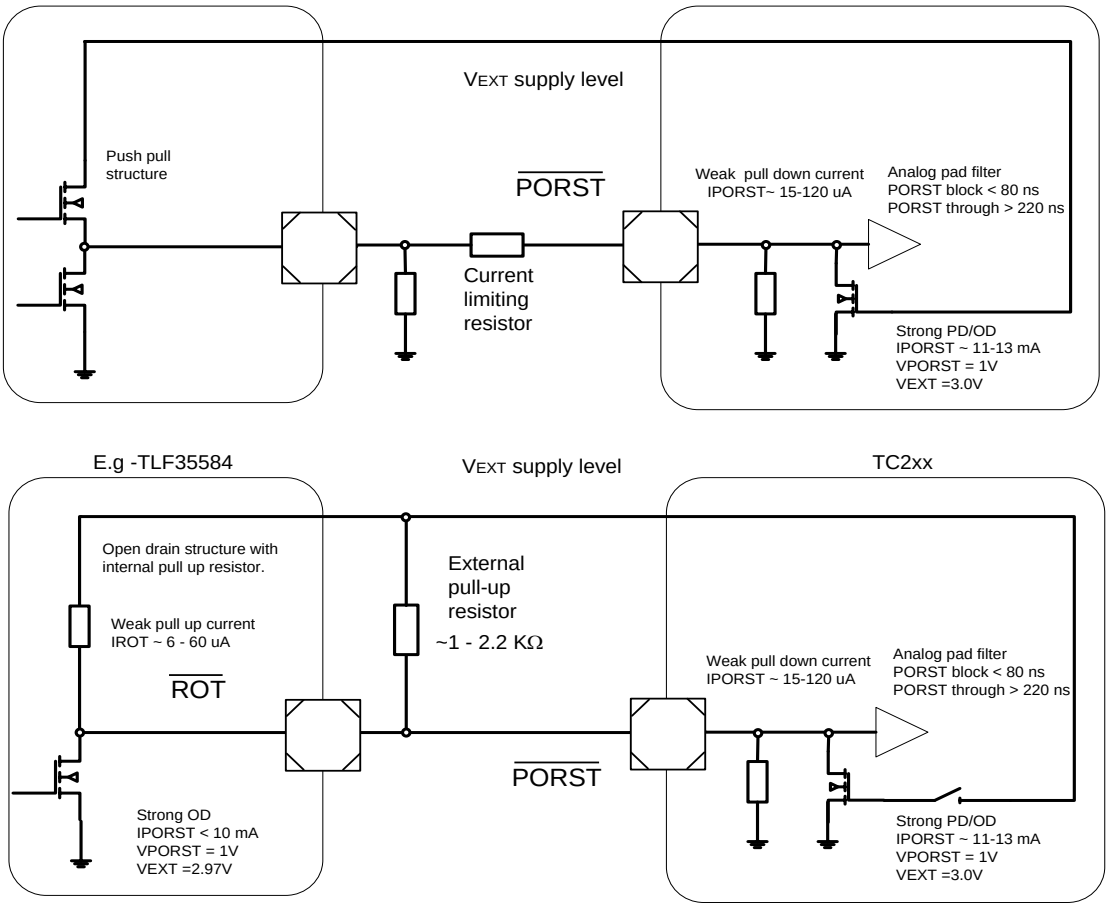
Debug pins are present in all devices across all packages.

Table 4 Debug pins and default state

Debug pins	Reset state / Internal pull devices	JTAG mode IEEE 1149.1	DAP (2 pin)	DAP (3 pin)
/TRST	Weak internal pull-**down** resistor. Test Reset Input	/TRST is asserted low on PORST release to enter Locked mode and later de-asserted by the tool to enter JTAG mode. TRST needs to be held high during JTAG operation phase. External pull-up not necessary as above transition is handled by debug tool.	TRST held high during /PORST release and to enter DAP mode. TRST need to be held high during DAP operation phase. External pull-up may be used but may not be required as the debug tool drives and keeps the /TRST pin high to enter DAP mode.	
TCK	Weak internal pull-**down** resistor.	40 MHz Test Clock Input to µC. External pull-up not necessary as handled by debug tool.	DAP0 160 MHz Clock pin	DAP0 160 MHz Clock pin
TMS	Weak internal pull-**down** resistor.	Test Mode Select Input to µC. External pull-up not necessary as handled by debug tool.	DAP1 bidirectional data	DAP1 Bi-directional
TDO (P21.7)	Weak internal pull-**up** resistor in DAP mode	Test Data Output to µC The pull-up resistor is disabled in JTAG mode	Not used	DAP2 Bi-directional
TDI (P21.6)	Weak internal pull-**up** resistor.	Test Data Input to µC	Not used	Not used
TGIx	Weak internal pull-**up** resistor	/BRKIN	-	-
TGOx	Weak internal pull-**up** resistor	-	-	-

3.6 /PORST pin

The Power-on Reset (PORST) pin has to be held high externally so that the microcontroller is in operational RUN state.



PORST pad	Symbol	Min	Typ	Max	Unit	Condition
Input high voltage, class LP pads CP	V_{IHLP} SR	2.0			V	Hysteresis active; TTL
Input low voltage Class LP pads CP	V_{ILLP} SR			0.8	V	Hysteresis active; TTL
Reset Output ROT						
Reset Output high level	$V_{ROT\ high}$	3.0			V	
Reset Output low level	$V_{ROT\ low}$			0.8	V	

Figure 6 PORST connectivity

The PORST pin is a bi-directional reset pin with 11-13 mA output drive capability in case of supply fail on any of the 5V, 3.3V or 1.3V supply rails. There is a weak internal pull-down (15 – 120µA pull current) on the /PORST pin to ensure that the device is in reset (safe) state if the /PORST pin-to-pad bond-wire breaks.

Usually a strong pull-up is required to keep PORST high during the operational state. The pull-up has to work against the microcontroller pull-down, the regulator pull-down and maybe also an additional pull device.

The PORST pin has default TTL level so that only 2.0V is required on the pin to keep microcontroller out of reset.

3.7 ADC supply

It shall be ensured that the analog reference supply (V_{DDM}*0,9) < V_{AREFX} < (V_{DDM} + 0,05V) shall not deviate far away from the main analog V_{DDM} supply to ensure ADC performance. Similarly, it shall be ensured that the analog reference ground (V_{SSM} - 0,05V) < V_{AGNDX} < (V_{SSM} + 0,05V) shall not deviate far away from the main analog V_{SSM} ground as documented in the datasheet.

Depending on whether the external regulator provides a dedicated analog supply or a common supply, noise de-coupling and monitoring should be appropriately addressed on a system level. Ensure that the ground connection of ADC is decoupled as shown in the figure.

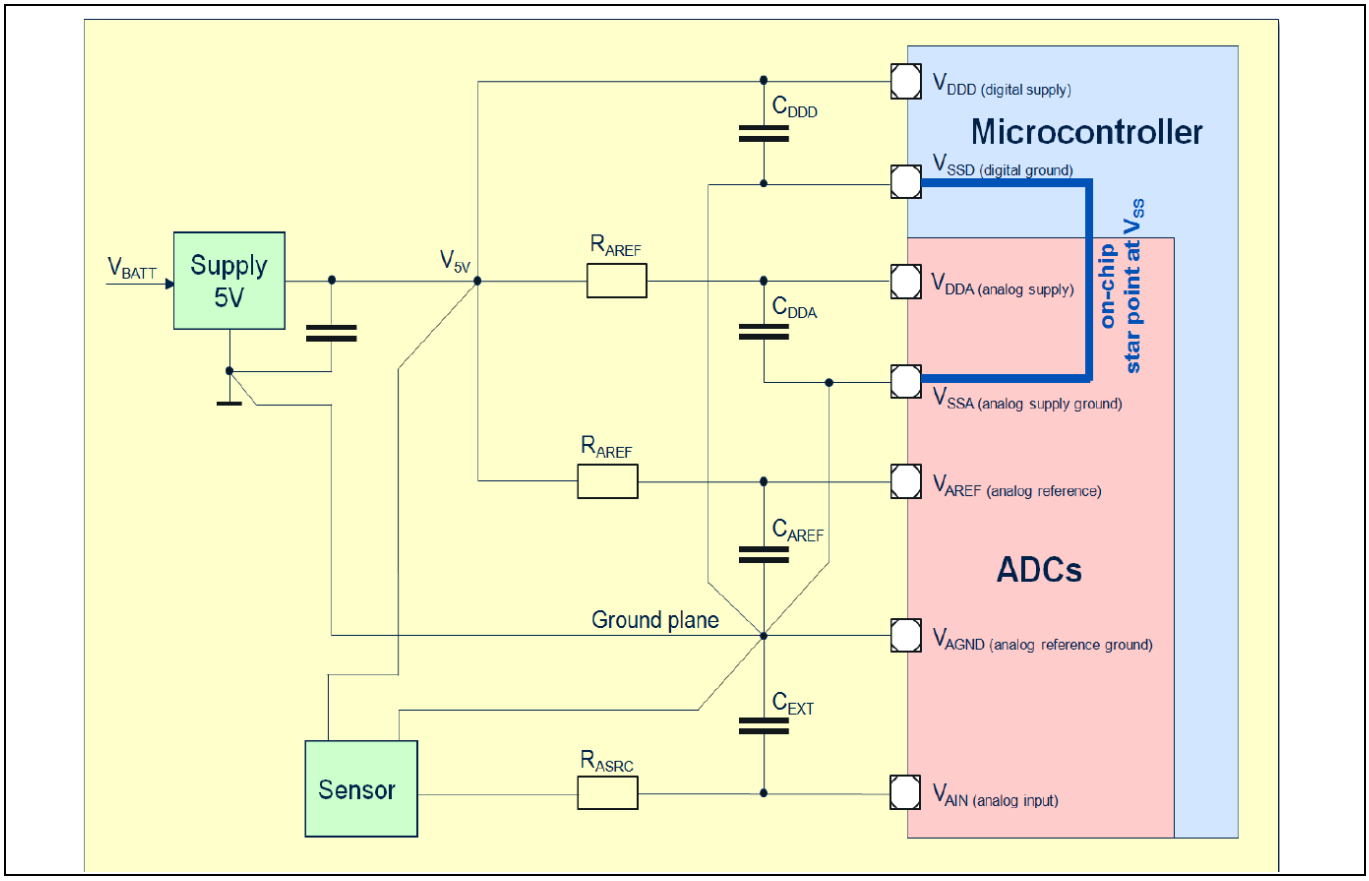


Figure 7 V_{EXT} and ADC supply with a common star ground connection

3.8 Oscillator and Flash supply

The oscillator supply constitutes a 3.3V V_{DDP3} supply and 1.3V V_{DD} supply and the V_{SS} ground pin. The V_{SS} ground pin is the only distinct ground pin in QFP packages.

The flash supply constitutes a 3.3V V_{DDP3} supply and a sensitive 3.3V V_{DDFL3} supply. The V_{DDFL3} supplies the sense amps and supplies the current required for normal read operations.

The important points to be taken care of for the Oscillator supply is the ground connection. This is to be isolated to contain the noise to reduce the radiation and coupling from the oscillator circuit. A separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island.

RC Filters can be inserted in the supply paths at the regulator output and at the branching to other module supply pins such as V_{DD} and V_{DDP3} (for osc.), V_{DDFL3}, and V_{DDM}. Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behavior of the circuit and reduce the radiation up to ~10dBµV on the related supply net.

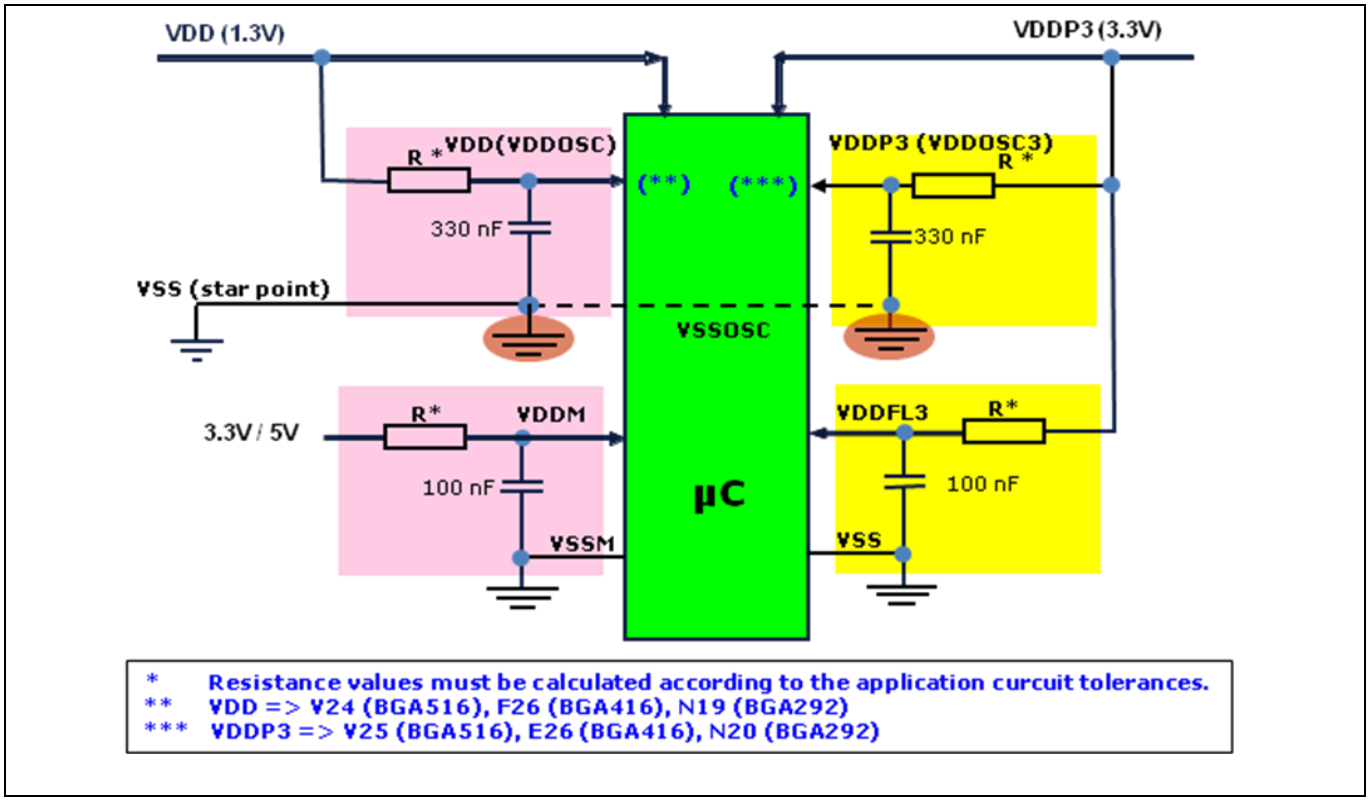


Figure 8 Filtering of V_{DD}, V_{DDP}, V_{DDFL3}, V_{DDM} supply pins for TC29x and TC27x, with optional ferrite bead components

A higher de-coupling capacitor of at least 330nF is recommended on V_{DDOSC3}. Optionally additional filtering may be added to the Flash V_{DDP3}/V_{DDFL3} 3.3V supply node and to the oscillator V_{DDOSC3} 3.3V supply node externally from the V_{DDP3} supply net.

The ground connections of the load capacitors and V_{SSOSC} should also be connected to this island. Traces for the load capacitors and XTAL should be as short as possible.

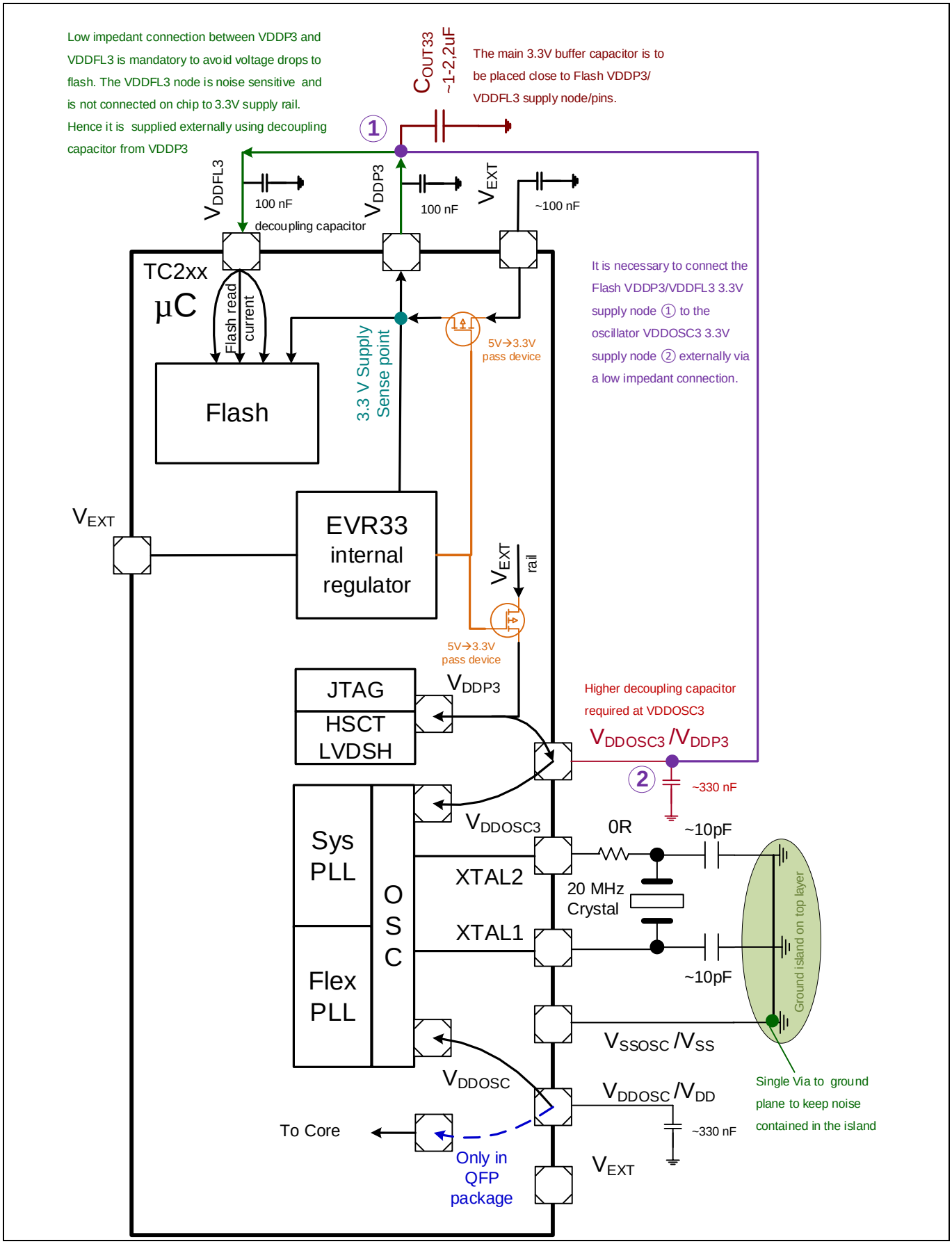


Figure 9 Flash and oscillator supply

3.9 /ESR0 pin

Activation of PORST also activates ESR0 reset output line by default. The ESR0 pin may be used as a reset input, reset output, or as a normal GPIO pin. Some applications require a reset out signal together with a reset out delay after power-up as long the initialization is complete.

For example, memory devices such as external RAM, Flash, and EEPROM devices may require that reset be held longer and released with a delay until after the main microcontroller reset has been released.

3.10 Considerations for unused pins

It is recommended to apply special measures for pins left unused by the application.

Table 5 Considerations for unused Output, Supply, Input and I/O pins

Supply Pins (Modules)	• See the User Manual.
I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pull-up is also possible. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce the number of external pull-up/down devices (keep in mind leakage current).
Input Pins with internal pull device	• For pins with alternate functions, please see the product specification to define the necessary logic level. • Should be configured as pull-down and should be activated static low (Exception: if the User Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solder pad should not be connected to any other net (isolated PCB-pad only for soldering)

4 TC2xx board design

This chapter introduces some ground rules for EMC-friendly PCB layout. This document is recommended as an additional information source.

4.1 Selection of stack-up for high-speed board design

Selection of the correct stack-up for a high-speed board should be made at the beginning of the board design because the selection can have an effect on the routing and impedance control of the traces. Impedance control of the traces is one of the main parameters of the high-speed design.

The following issues must be considered:

- Guarantee that high-speed lines have a solid GND reference without interruption of the impedance continuity.
- Signal lines must have minimum distance to reference the plane layer.
- Ensure, as much as possible, a plane capacitance for the supply domains.
- Avoid vias or layer change on high-speed signals (if possible).

Since the discrete board de-coupling capacitors can only be effective up to 200MHz, the plane de-coupling should be used where possible. The stack-up should be selected so that you can build a power plane capacitance and have the benefit of the high frequency de-coupling effect which could be effective above 200MHz. Below is the example stack-up's of 4-Layer and 6-Layer boards.

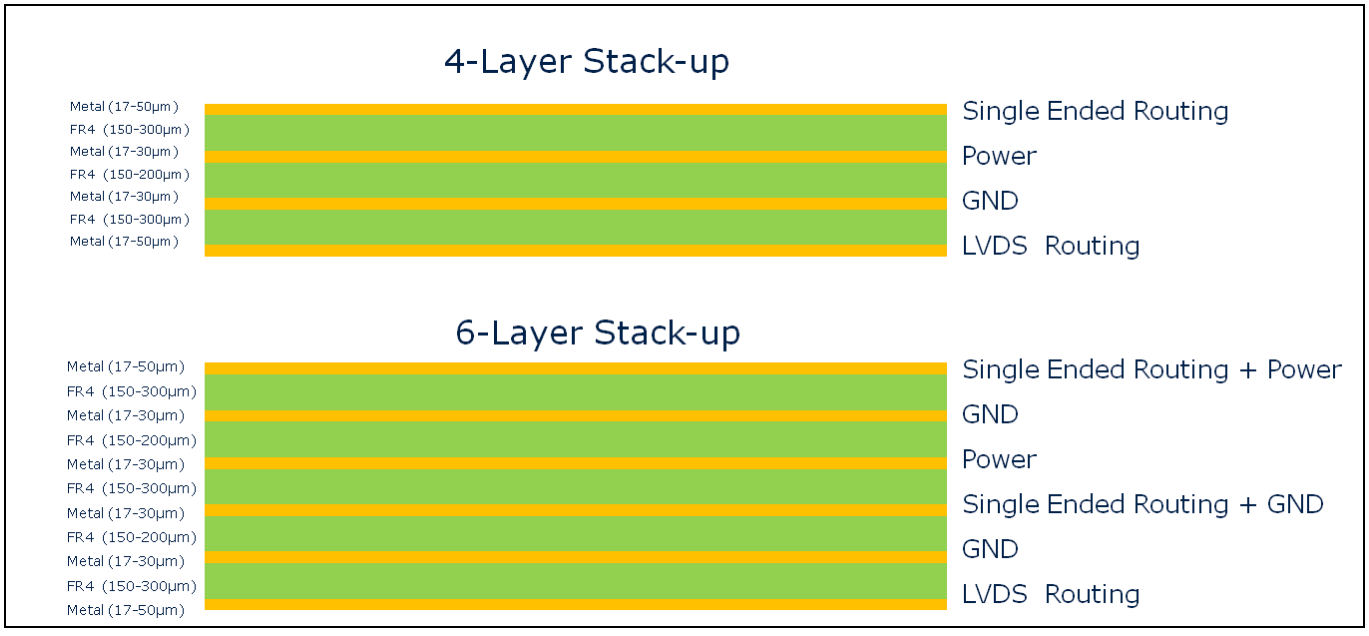


Figure 10 Sample stack-up's for 4 and 6-layer boards

4.2 Component placement

- Place the µC and Connector with high-speed signals first, to ensure minimal length of the traces.
- Do not place other components between these Connectors and the µC.
- Place possible noise sources away from the high-speed signals.
- Components that communicate with devices outside the board should be placed at the edge of the board.

4.3 Board level filtering and de-coupling

De-coupling the Power Distribution Network of the microcontroller IC is critical to the PCB design process, because careful selection of the de-coupling capacitors and placement has a big influence on the high-speed performance of the board, and can reduce the emissions. The on-board de-coupling capacitors have an effective range of 1MHz – 200MHz. The range above 200MHz can be covered by using power plane capacitance.

The effectiveness of the de-coupling capacitors depends on the optimum placement and connection type.

- Place capacitors as close as possible to the µC.
- Keep the interconnection inductance of capacitors to the µC as low as possible.
- Use low effective series resistance and inductance (ESR and ESL) capacitors.
  - Since parasitic inductance is the limiting factor of the capacitor response to high frequency demand of current from the device, the ESL of the capacitor and the connection inductance should be selected so that the optimum value for the design is reached.
- Connect capacitors with vias close to the side of the pads.
  - Use side placement of the vias to reduce the current loop.

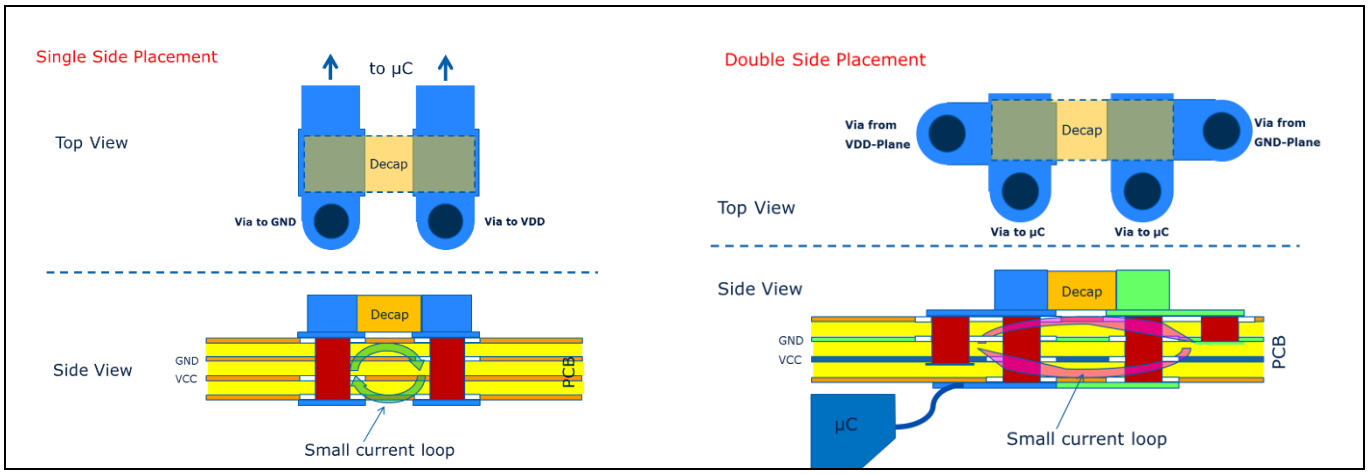


Figure 11 Connection of decaps

- Dual vias can be used to reduce the parasitic inductance.
- Solder lands, traces and vias should be optimized for capacitor placement.
- Select the smallest package available for the capacitors.
  - Select capacitors of type: ceramic multilayer X7R or X5R.
- Do not use long traces to connect capacitors to GND or to V_{DD}.
  - Always keep the return path of the high frequency current (lowest inductance path) small.

4.3.1 Oscillator circuit PCB design

To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer.

- This helps to keep noise generated by the oscillator circuit locally on this separated island.
- The ground connections of the load capacitors and V_{SSOSC} should also be connected to this island.
- Traces for the load capacitors and XTAL should be as short as possible.

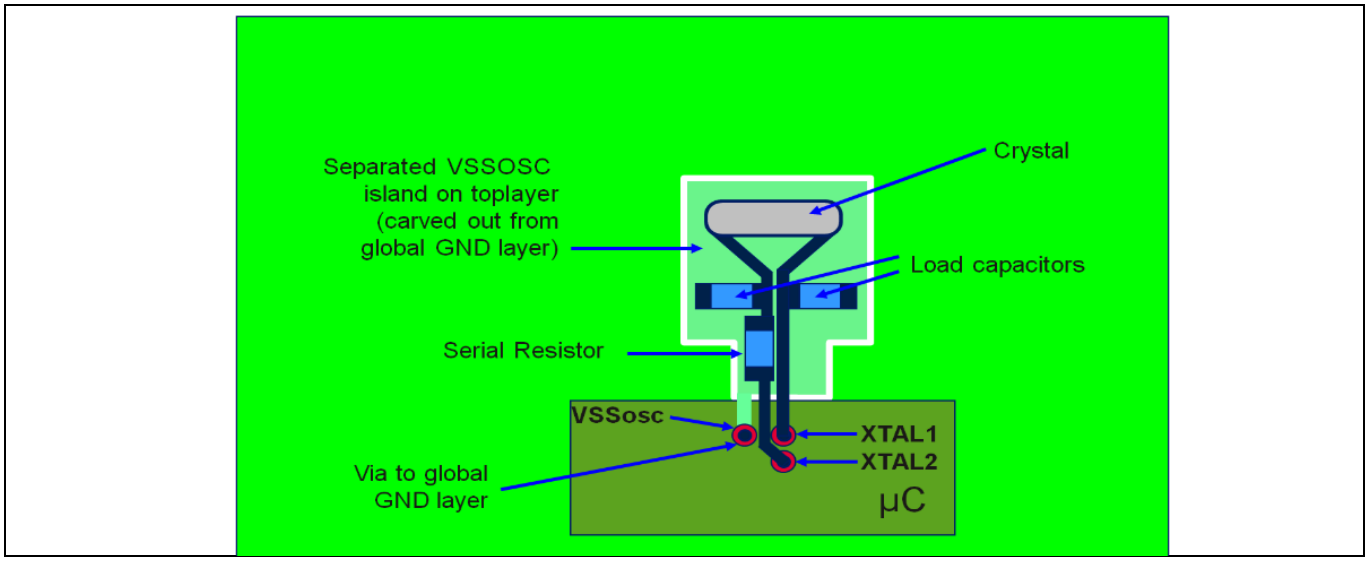


Figure 12 Layout proposals for Oscillator circuit (shown for BGA package)

4.3.2 Recommendations for the supply noise filtering

- Ground for OSC / PLL supply pins should be laid out as a local island.
- Analog and digital grounds are connected inside the microcontroller. Therefore the ground for ADC (V_{SSM} for V_{DDM}) should be routed depending on external noise conditions:
  - Use a common star point when external noise should be prevented from entering the analog domain.
  - Otherwise, use a common ground plane.
- The power distribution from the regulator to each power plane should be made over filters.
- RC Filters can be inserted in the supply paths at the regulator output and at the branching to other module supply pins such as V_{DDOSC} and V_{EXTOSC} (for osc.), V_{AREF} and V_{DDM}.

4.3.3 Recommendations to improve EMI

The following recommendations may improve system EMI performance:

- To minimize the EMI radiation on the PCB, the following signals are to be considered as critical.
  - LVDS Pins (HSCT, MSC, QSPI, AGBT)
  - ERAY Pins
  - Ethernet Pins
  - QSPI Pins
  - MSC Pins
  - External Clock Pins
  - Supply Pins
- Route these signals with adjacent ground reference and avoid signal and reference layer changes.
- Route them as short as possible.
- Routing ground on each side can help to reduce coupling to other signals.
- OCDS must be disabled in production.
- Use lowest possible frequency for SYSCLK output of the PLL still allowing to reach necessary module clock frequencies.

4.4 De-coupling components and layouts

Each device package has its own recommendations for a set of necessary de-coupling capacitors and their optimized placement on the PCB.

The AURIX™ TC2xx microcontroller products are available in the following packages:

- TQFP-80
- TQFP-100
- LQFP-144
- LQFP-176
- BGA-292
- BGA-416
- BGA-516

There are example layouts and decoupling for various packages, given in the Appendix of this document.

5 EVRs: Recommended settings, components and layout

The fully integrated DC/DC buck (step-down) converter generates a regulated 1.3 V nominal power supply out of a 5V or 3.3V external supply, with a high efficiency. The converter modulates an external complementary MOSFET to buffer the energy in an LC filter in order to generate a regulated core supply. In active mode, the step-down converter operates with synchronous rectifying and fixed frequency Pulse Width Modulation (PWM).

The figure below provides a schema for EVR33 LDO and EVR13 in SMPS mode with necessary component set.

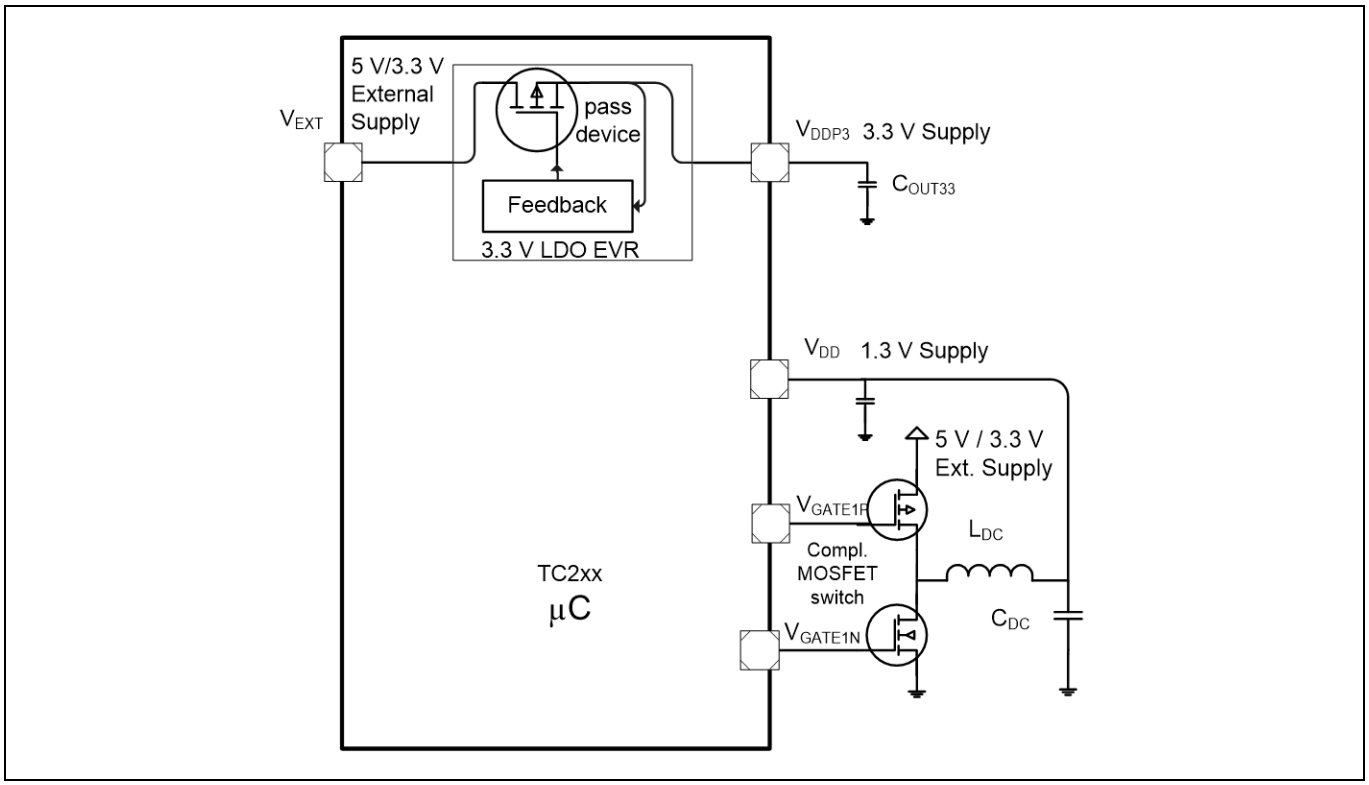


Figure 13 Basic schema of the EVR33 LDO and EVR13 in SMPS mode (TC29x, TC27x, TC26x)

5.1 Recommended settings for components and frequency for EVR13 in SMPS mode for TC29x, TC27x, and TC26x

You must program EVR13 settings during the application start-up to match the chosen hardware configuration. A suitable choice may be made from the 12 parameter sets documented in this section, based on:

- Maximum supported load current for supply dimensioning:
  - 1A IDD current / 22uF output capacitor (TC29x for example)
  - 400mA IDD current /10uF output capacitor (TC27x and TC26x for example)
- Switching Frequency of the SMPS regulator.
  - 1 MHz
  - 1.5 MHz
  - 1.8 MHz
- V_{EXT} Voltage supply range
  - 2.97 V – 5.5 V range : Nominal 5V external single supply application
  - 2.97 V – 3.63 V range : Nominal 3.3V external single supply application

Attention: ***In the following table the capacitance sizes given include a derating of up to 30% with respect to temperature, process, and ageing, as documented in the corresponding datasheets. For higher temperature applications a derating of 50% on the capacitor nominal sizes needs to be additionally considered, which would lead to higher nominal capacitance values.***

Table 6 Component choice, load current, frequency selection and register settings

Set	Condition	Register values	Components
1	I_{DD} < 400 mA f_{DC} = 1.8 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - 0937051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49370002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 153806B8$_H$ EVRSDCTRL3 - 00090A30$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00997E7C$_H$ EVRSDCOEFF2 - 00D9AEBC$_H$ EVRSDCOEFF3 - 009C5A02$_H$ EVRSDCOEFF4 - 00006355$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 0000231C$_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-3R3N-H/D[1] OR • SLF7045T-3R3M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)

[1] If the I_{DD} current ripple needs to be further reduced, a higher inductance (LTFx02yT-4R7N-H/D) can be used.

[2] If 2 output capacitors are preferred instead of a single output capacitor for robustness or safety considerations, then 2x 10uF can be considered instead of a single 10uF. Similarly, instead of a single 22 uF, 2x 10uF can be considered.

2	I_{DD} < 400 mA f_{DC} = 1.8 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - 0937051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49370002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 15240684$_H$ EVRSDCTRL3 - 00090A30$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00997E7C$_H$ EVRSDCOEFF2 - 00D9AEBC$_H$ EVRSDCOEFF3 - 009C5A02$_H$ EVRSDCOEFF4 - 00006355$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 0000231C$_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-3R3N-H/D[1] OR • SLF7045T-3R3M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)
3	I_{DD} < 400 mA f_{DC} = 1.5 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - 0940051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49400002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 153806B8$_H$ EVRSDCTRL3 - 00090A36$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00A9ADAD$_H$ EVRSDCOEFF2 - 00F91919$_H$ EVRSDCOEFF3 - 009C5A02$_H$ EVRSDCOEFF4 - 00006355$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 0000231C$_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-3R3N-H/D[1] OR • SLF7045T-3R3M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)
4	I_{DD} < 400 mA f_{DC} = 1.5 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - 0940051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49400002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 15240684$_H$ EVRSDCTRL3 - 00090A36$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00A9ADAD$_H$ EVRSDCOEFF2 - 00F91919$_H$ EVRSDCOEFF3 - 009C5A02$_H$ EVRSDCOEFF4 - 00006355$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 0000231C$_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-3R3N-H/D[1] OR • SLF7045T-3R3M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)

5	I_{DD} < 400 mA f_{DC} = 1 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - $0964051F_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49640003_H (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - $153806B8_H$ EVRSDCTRL3 - $00090A5A_H$ EVRSDCTRL4 - 00001001_H EVRSDCOEFF1 - $00CA8D8C_H$ EVRSDCOEFF2 - $00A97C7B_H$ EVRSDCOEFF3 - $009C5A02_H$ EVRSDCOEFF4 - 00006355_H EVRSDCOEFF5 - $001B1A02_H$ EVRSDCOEFF6 - $0000231C_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-4R7N-H/D OR • SLF7045T-4R7M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)
6	I_{DD} < 400 mA f_{DC} = 1 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - $0964051F_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49640003_H (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 15240684_H EVRSDCTRL3 - $00090A5A_H$ EVRSDCTRL4 - 00001001_H EVRSDCOEFF1 - $00CA8D8C_H$ EVRSDCOEFF2 - $00A97C7B_H$ EVRSDCOEFF3 - $009C5A02_H$ EVRSDCOEFF4 - 00006355_H EVRSDCOEFF5 - $001B1A02_H$ EVRSDCOEFF6 - $0000231C_H$	**Complementary MOSFET** • BSL215C (TSOP-6) **Inductor** • LTF3020T-4R7N-H/D OR • SLF7045T-4R7M2R1 **Output Capacitor** • 10uF • CGA6M3X7R1C106K (1210)[2] **Input Capacitor** • 6.8uF • CGA5L1X7R1C685K (1206)
7	I_{DD} < 1 A f_{DC} = 1.8 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - $0937051F_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49370002_H (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - $15B406C8_H$ EVRSDCTRL3 - $00090A30_H$ EVRSDCTRL4 - 00001001_H EVRSDCOEFF1 - $00997E7C_H$ EVRSDCOEFF2 - $00D9AEBC_H$ EVRSDCOEFF3 - $009B5A02_H$ EVRSDCOEFF4 - 00006255_H EVRSDCOEFF5 - $001B1A02_H$ EVRSDCOEFF6 - 00002324_H	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-3R3N2R5-H/D[1] OR • LTF4022T-3R3N-H/D OR • RLF7030T-3R3M4R1-T OR • SLF7045T-3R3M2R1 **Output Capacitor** • 22uF or 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)

8	I_{DD} < 1 A f_{DC} = 1.8 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - 0937051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49370002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 157406A8$_H$ EVRSDCTRL3 - 00090A30$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00997E7C$_H$ EVRSDCOEFF2 - 00D9AEBC$_H$ EVRSDCOEFF3 - 009B5A02$_H$ EVRSDCOEFF4 - 00006255$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 00002324$_H$	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-3R3N2R5-H/D[1] OR • LTF4022T-3R3N-H/D OR • RLF7030T-3R3M4R1-T OR • SLF7045T-3R3M2R1 **Output Capacitor** • 22uF or 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)
9	I_{DD} < 1 A f_{DC} = 1.5 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - 0940051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49400002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 15B406C8$_H$ EVRSDCTRL3 - 00090A36$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00B91918$_H$ EVRSDCOEFF2 - 00B81817$_H$ EVRSDCOEFF3 - 009B5A02$_H$ EVRSDCOEFF4 - 00006255$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 00002324$_H$	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-3R3N2R5-H/D[1] OR • LTF4022T-3R3N-H/D OR • RLF7030T-3R3M4R1-T OR • SLF7045T-3R3M2R1 **Output Capacitor** • 22uF OR • 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)

10	I_{DD} < 1 A f_{DC} = 1.5 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - 0940051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49400002$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 157406A8$_H$ EVRSDCTRL3 - 00090A36$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00B91918$_H$ EVRSDCOEFF2 - 00B81817$_H$ EVRSDCOEFF3 - 009B5A02$_H$ EVRSDCOEFF4 - 00006255$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 00002324$_H$	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-3R3N2R5-H/D[1] OR • LTF4022T-3R3N-H/D OR • RLF7030T-3R3M4R1-T OR • SLF7045T-3R3M2R1 **Output Capacitor** • 22uF OR • 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)
11	I_{DD} < 1 A f_{DC} = 1 MHz V_{EXT} < 5,5 V	EVRSDCTRL1 - 0964051F$_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49640003$_H$ (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - 15B406C8$_H$ EVRSDCTRL3 - 00090A5A$_H$ EVRSDCTRL4 - 00001001$_H$ EVRSDCOEFF1 - 00F91918$_H$ EVRSDCOEFF2 - 00F81817$_H$ EVRSDCOEFF3 - 009B5A02$_H$ EVRSDCOEFF4 - 00006255$_H$ EVRSDCOEFF5 - 001B1A02$_H$ EVRSDCOEFF6 - 00002324$_H$	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-4R7N2R0-H/D OR • LTF4022T-4R7N-H/D OR • RLF7030T-4R7M3R4-T OR • SLF7045T-4R7M2R1 **Output Capacitor** • 22Uf OR • 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)

12	I_{DD} < 1 A f_{DC} = 1 MHz V_{EXT} < 3.63 V	EVRSDCTRL1 - $0964051F_H$ (TC26xA ,TC27xB, TC29xA) EVRSDCTRL1 - 49640003_H (TC26xB, TC27xC, TC27xD, TC29xB) EVRSDCTRL2 - $157406A8_H$ EVRSDCTRL3 - $00090A5A_H$ EVRSDCTRL4 - 00001001_H EVRSDCOEFF1 - $00F91918_H$ EVRSDCOEFF2 - $00F81817_H$ EVRSDCOEFF3 - $009B5A02_H$ EVRSDCOEFF4 - 00006255_H EVRSDCOEFF5 - $001B1A02_H$ EVRSDCOEFF6 - 00002324_H	**Complementary MOSFET** • BSZ15DC02KD (S3O8) **Inductor** • LTF5022T-4R7N2R0-H/D OR • LTF4022T-4R7N-H/D OR • RLF7030T-4R7M3R4-T OR • SLF7045T-4R7M2R1 **Output Capacitor** • 22uF OR • 2 x 10uF • CGA6P1X7R1C226M (1210)[2] **Input Capacitor** • 10uF • CGA6M3X7R1C106K (1210)

Note: For TC29x to achieve 300 MHz performance, a higher nominal core voltage has to be supplied.

Table 7 Additional register updates for TC29x for 1.33V +- 7.5%

Set	Condition	Register values	Components
1	V_{DD} = 1.33V +- 7.5%	EVRTRIM.SDVOUTSEL – 79_H EVRRSTCON.RST13TRIM – $D0_H$ EVRUVMON.EVR13UVVAL – $D4_H$	-

5.1.1 EVR13 example layout

Here we show a sample layout for the design which use single supply mode with EVR13 in SMPS/DC-DC regulator mode. The component references are the same in the table with recommended component values for identification. In addition, EVR13 allows for the LDO mode with a minimal component set.

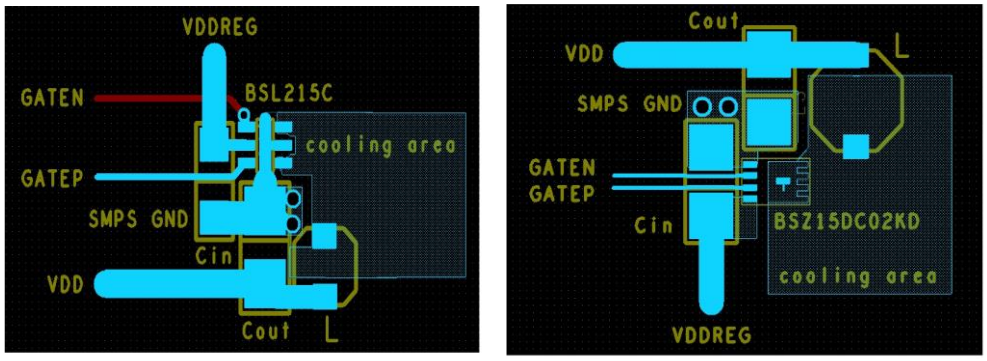


Figure 14 Layout schemes

5.2 Components for the EVR13 in LDO mode

A system integrator may decide to use EVR13 in LDO configuration if the power and thermal constraints of the applications allow this. No software based adjustment of register settings is required in the application.

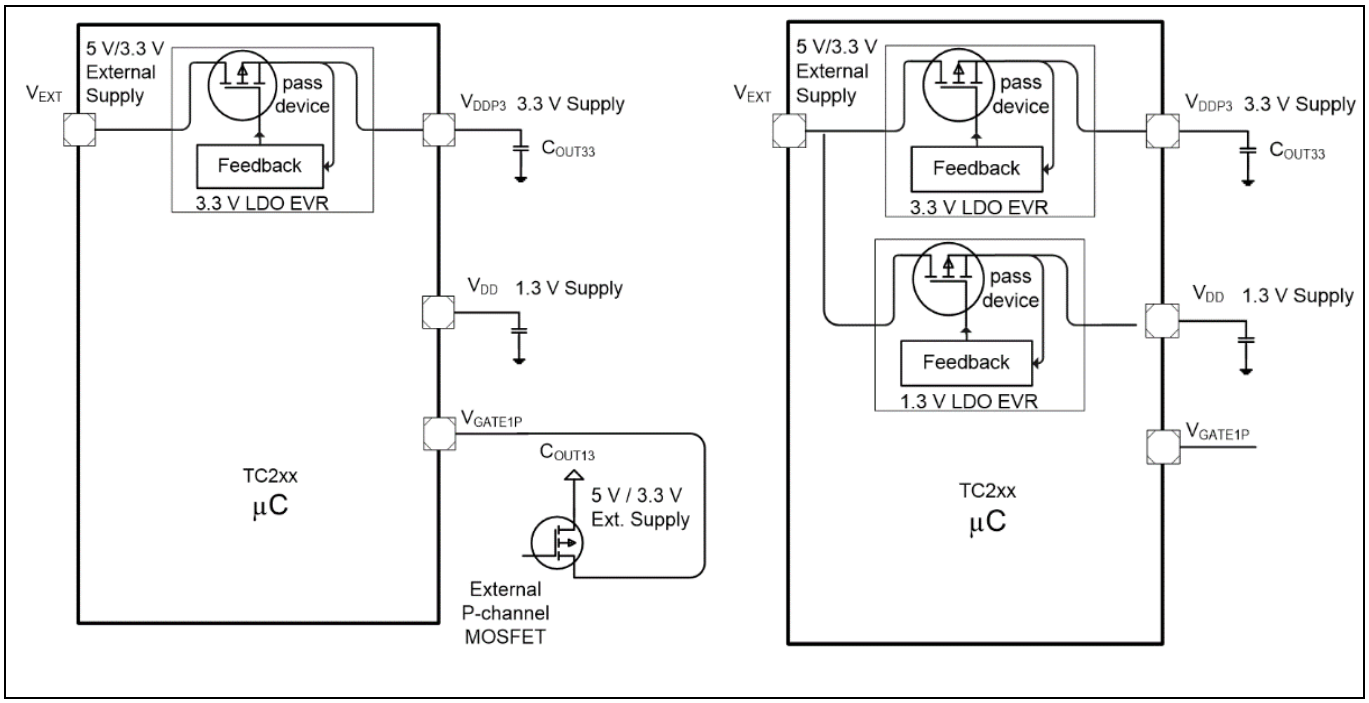


Figure 15 Basic schema of the EVR33 LDO and EVR13 in LDO mode with internal (right) and external (left) pass devices

Table 8 Components for the EVR13 on LDO mode

EVR13 LDO with an external P-Channel MOSFET as pass devices			
Set	**Core maximum load**	**Pass device**	**Buffer capacitor**
1.	I_{DD} < 300 mA	P-Channel MOSFET SPD04P10PL (TO-252) IPD50P04P4L (TO-252)	Output Capacitor10 uF CGA5L1X7R1C106K (1206)
EVRx3 LDO with internal pass devices			
2.	I_{DDX} < 100 mA	-	C3216X7R1C105K (1206)
3.	I_{DDX} < 200 mA	-	C3216X7R1C225K (1206)
4.	I_{DDX} < 300 mA	-	C3216X7R1C475K (1206)

5.3 Recommended settings for components and frequency for EVR13 in SMPS mode for TC23x

- Smaller devices of the TC2xx family (TC23x) provide the EVR13 SMPS regulator with switching capacitor configuration. This allows for a smaller component set. The maximum supported load current for supply dimensioning is:
  - 230mA IDD current / 10uF output capacitor (TC23x for example)
- Switching Frequency of the SMPS regulator:
  - 1 MHz
  - 1.85 MHz
- V_{EXT} Voltage supply range:
  - 3.0 V – 3.63 V range : Nominal 3.3V external single supply application.

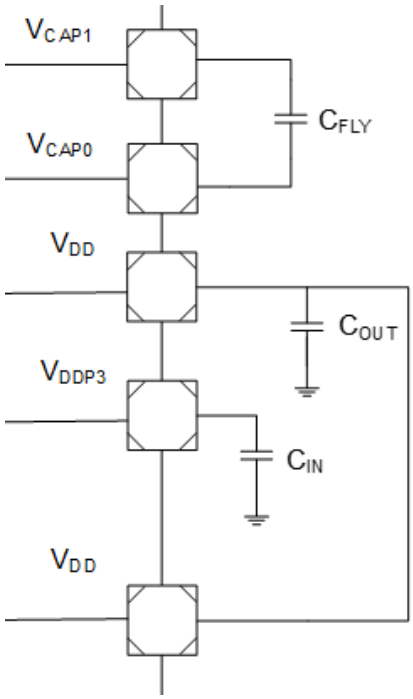


Figure 16 Basic schema EVR13 in SMPS mode in SCDCDC configuration

Attention: ***In the following table the capacitance sizes include a derating of up to 35% with respect to temperature process and aging, as documented in the corresponding datasheet. In case of higher temperature applications, a derating of 50% on the capacitor nominal sizes needs to be additionally considered, which would lead to higher nominal capacitance values.***

Table 9 Component choice, Load current, Frequency selection and Register settings

Case	Condition	Register values	Component options
1	I_{DD} < 230 mA f_{DC} = 1 MHz V_{ddp3} < 3,63 V	EVRSDCTRL1 - 0829 2901_H EVRSDCTRL2 - 1541 9100_H EVRSDCTRL3 - 3C49 0880_H EVRSDCOEFF2 - 0000 0507_H	**Output Capacitor (10 uF nominal value)** • CGA6M3X7R1C106K (12xx) • C3216X7R1C106 (1210) **Flying Capacitor (1 uF nominal value)** • CGA6P1X7R1C105K (12xx) • C2012X7R1E105 (0805) **Input Capacitor (4,7 uF nominal value)** • CGA6P1X7R1C475K (12xx) • C2012X7R1E475 (0805)
2	I_{DD} < 230 mA f_{DC} = 1.85 MHz V_{ddp3} < 3,63 V	EVRSDCTRL1 - 0812 1201_H EVRSDCTRL2 - 1541 9100_H EVRSDCTRL3 - 3C49 0880_H EVRSDCOEFF2 - 0000 0407_H	**Output Capacitor (10 uF nominal value)** • CGA6M3X7R1C106K (12xx) • C3216X7R1C106 (1210) **Flying Capacitor (1 uF nominal value)** • CGA6P1X7R1C105K (12xx) • C2012X7R1E105 (0805) **Input Capacitor (4,7 uF nominal value)** • CGA6P1X7R1C475K (12xx) • C2012X7R1E475 (0805)

6 Appendix

6.1 Example layouts for TC29x, TC27x and TC26x

The sample layout designs are based on the given stack-up and the following design rules:

- Trace = 130µm, Via-drill/-pad 0.3/0.6mm.
- 130µm clearance for signal-to-signal and signal-to-pad.
- Top/Bottom Cu Thickness 50µm.
- Inner layer Cu Thickness.

6.1.1 Example layout for BGA-516 package

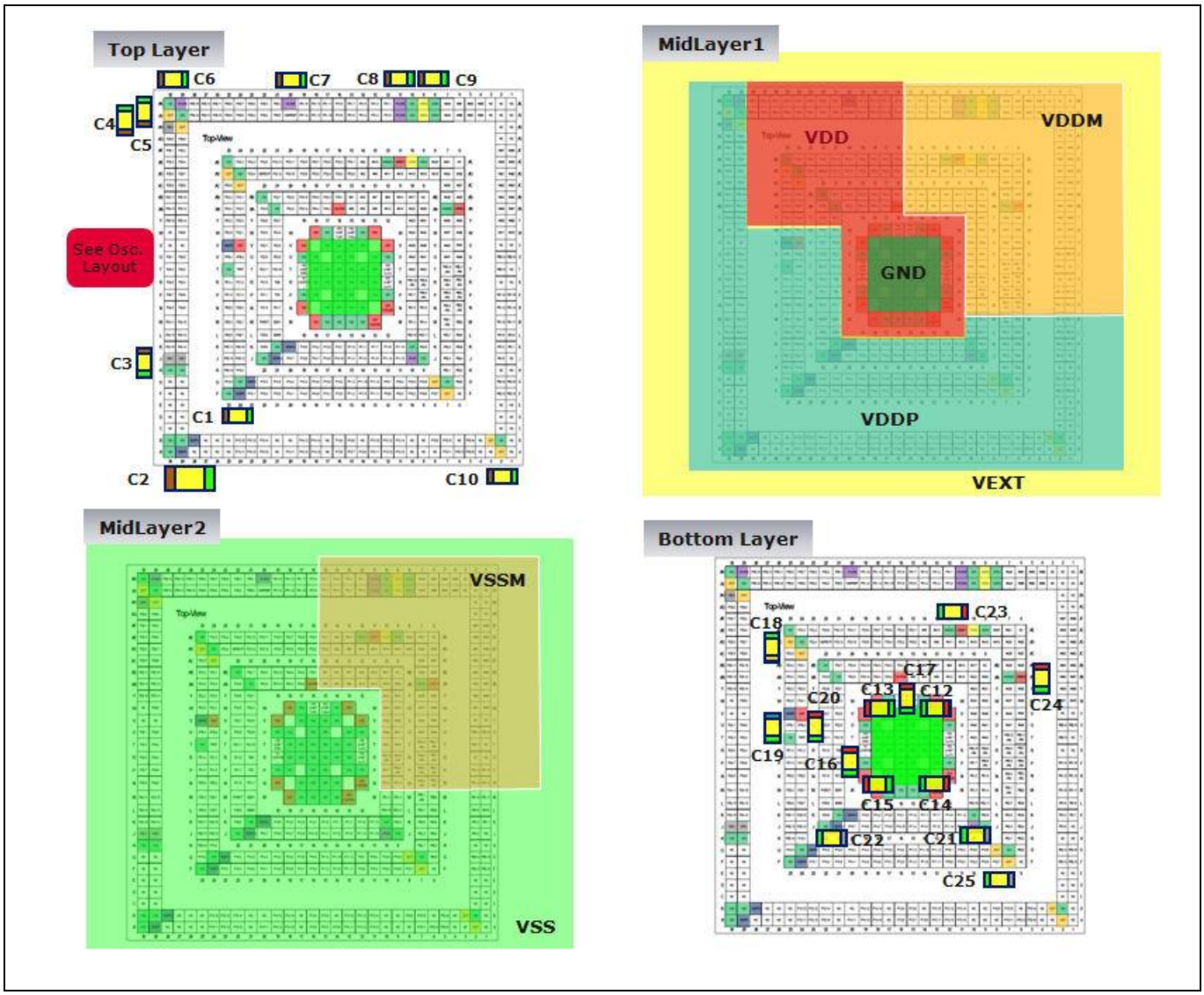


Figure 17 Example layout for BGA-516 package

Table 10 De-coupling capacitor list for BGA-516 for external supply mode

Capacitor	Value	Supply	BGA-516 pin
C12, C13, C15	3 x 100nF	V_{DD}	V19//W18, V12//W13, M18//N19
C14	1 x 100nF	V_{DD}/V_{DDSB} (PD/ED)	M13//N12
C6, C7, C8	3 x 100nF	V_{FLEXE}	AK29, AK20, AK11//AJ11
C21	1 x 100nF	V_{FLEX}	J10
C5, C18, C10, C25	4 x 100nF	V_{EXT}	AJ30//AH29, AD25//AC24, A2//B3, F7//G8
C4, C3	2 x 100nF	V_{EBU}	AH30, J30//J29
C22	1 x 100nF	V_{DDFL3}	J21//K20
C16	1 x 100nF	V_{DDPSB} (only for ED)	R19
C1	1 x 100nF	V_{DDP3}	F24//G23
C2	1 x 330nF-470nF in case of external supply or 1 x 1µF-2µF in case of internal LDO EVR supply	V_{DDP3}	A29//B28
C23	1 x 100nF	V_{AREF0} / V_{AGND0}	AE11
C24	1 x 100nF	V_{AREF2} / V_{AGND2}	AA6
C9	1 x 100nF	V_{DDM}	AK9//AJ9//AE10
C19	1 x 330nF	V_{DDP3}	V25
C20	1 x 330nF	V_{DD}	V24
C17	1 x 100nF	V_{EVRSB}	AA16

6.1.2 Example layout for BGA-416 package

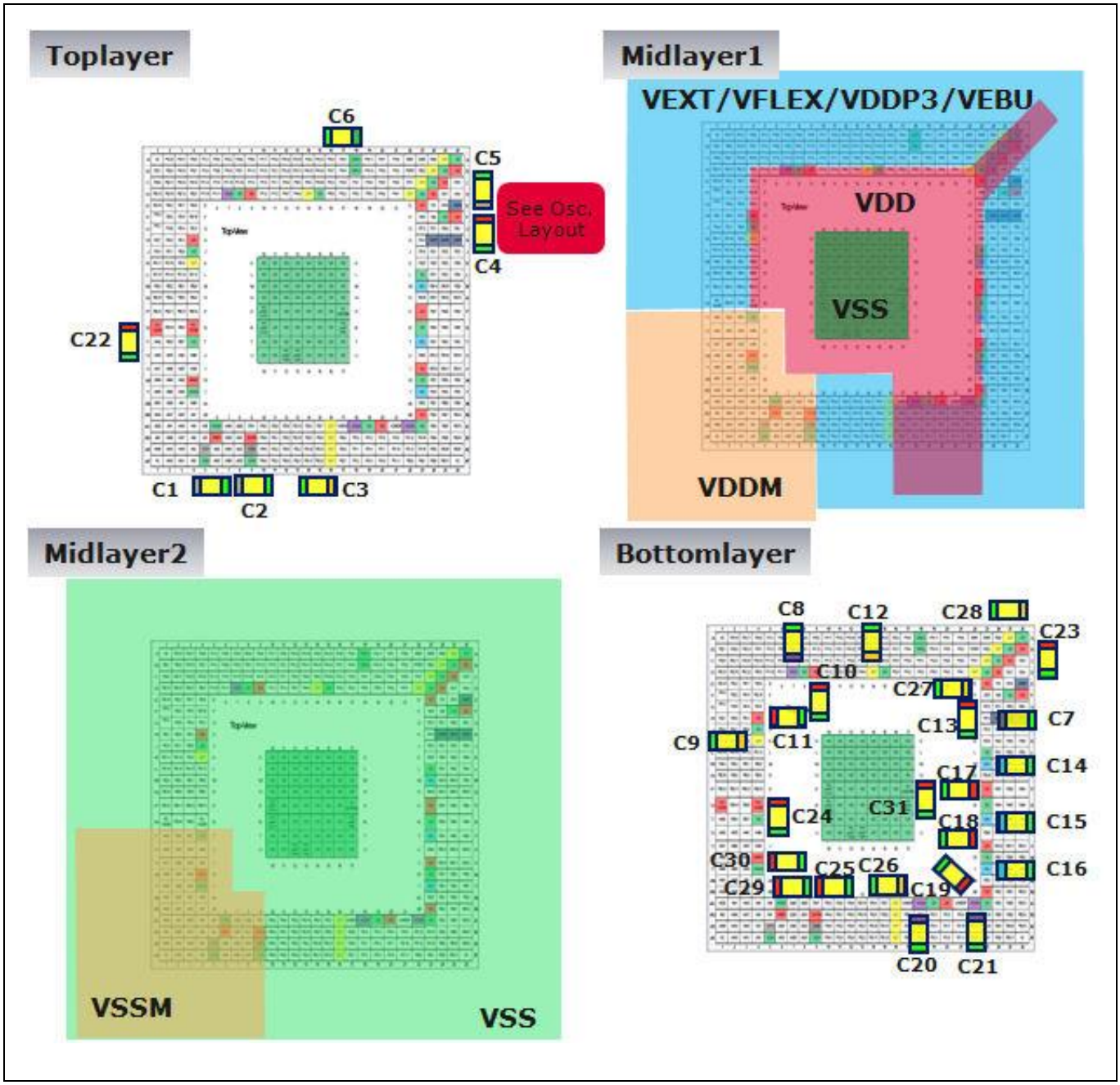


Figure 18 Example layout for BGA-416 package

Figure 19 De-coupling capacitor list for BGA-416 for external supply mode

Capacitor	Value	Supply	BGA-416 pin
C17, C18, C19, C13, C23, C10, C11	7 x 100nF	V_{DD}	P23, V23, AB23//AC20, E23//D24, C25//B26, D9, H4
C22, C24	2 x 100nF	V_{DDSTBY} (only for ED)	R1, R4
C9, C12, C3, C26, C27, C28	6 x 100nF	V_{EXT}	K4, D14, AC16//AD16, AE16//AF16, D22//C23, B24/A25
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply	V_{DDP3}	H24//H25//H26
C14, C15, C16	3 x 100nF	V_{EBU}	M23, T23, Y23
C20, C21	2 x 100nF	V_{FLEXE}	AC18, AC22
C8	1 x 100nF	V_{FLEX}	D7
C6	1 x 100nF	V_{DDFL3}	A18//B18
C5	1 x 330nF	V_{DDP3}	E26
C4	1 x 330nF	V_{DD}	F26
C1, C2	2 x 100nF	V_{DDM}	AE5, AE9
C25	1 x 100nF	$V_{DDEVRSB}$	AD9
C29	1 x 100nF	V_{AREF1}	AD6
C30	1 x 100nF	V_{AREF2}	W4
C31	1 x 100nF	V_{DDPSB}	P17

6.1.3 Example layout for LFBGA-292 package

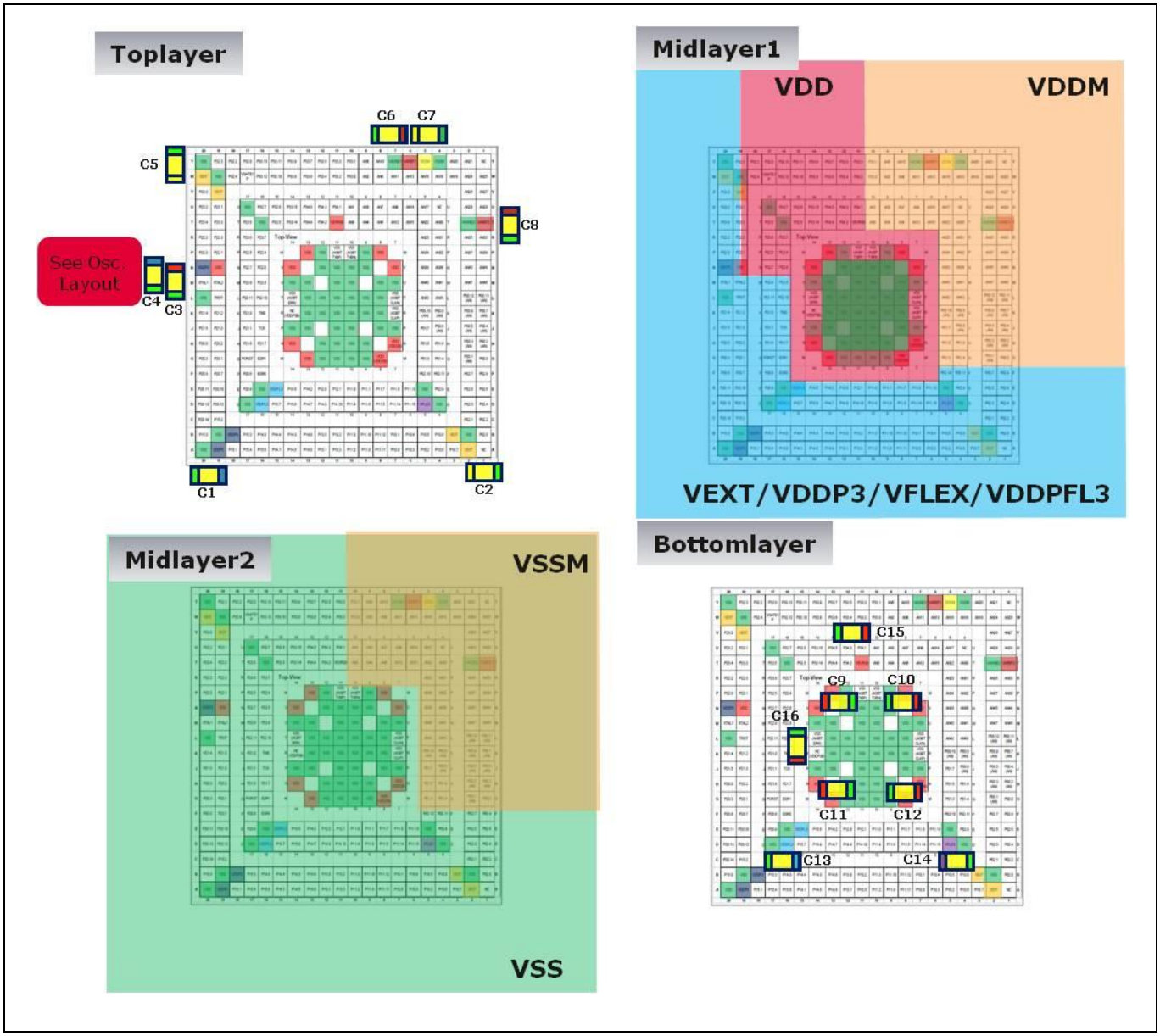


Figure 20 Example layout for LFBGA-292 package

Table 11 De-coupling capacitor list for LFBGA-292 package for external supply mode

Capacitor	Value	Supply	BGA-292 pin
C9, C10, C11	3 x 100nF	V_{DD}	P13//N14, P8//N7, H14//G13
C12	1 x 100nF	V_{DD}/V_{DDSTBY} (PD/ED)	H7//G8
C13	1 x 100nF	V_{DDFL3}	D16//E15
C14	1 x 100nF	V_{FLEX}	D5
C2, C5	2 x 100nF	V_{EXT}	A2//B3, V19//W20
C1	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply	V_{DDP3}	A19//B18
C3	1 x 330nF	V_{DD} (V_{DDOSC})	N19
C4	1 x 330nF	V_{DDP3} (V_{DDOSC3})	N20
C7	1 x 100nF	V_{DDM} / V_{SSM}	Y5
C6	1 x 100nF	V_{AREF1} / V_{AGND1}	Y6
C8	1 x 100nF	V_{AREF2} / V_{AGND2}	T1
C15	1 x 100nF	V_{EVRSB}	T11
C16	1 x 100nF	V_{DDPSB} (only for ED)	K14

6.1.4 Example layout for LQFP-176 package

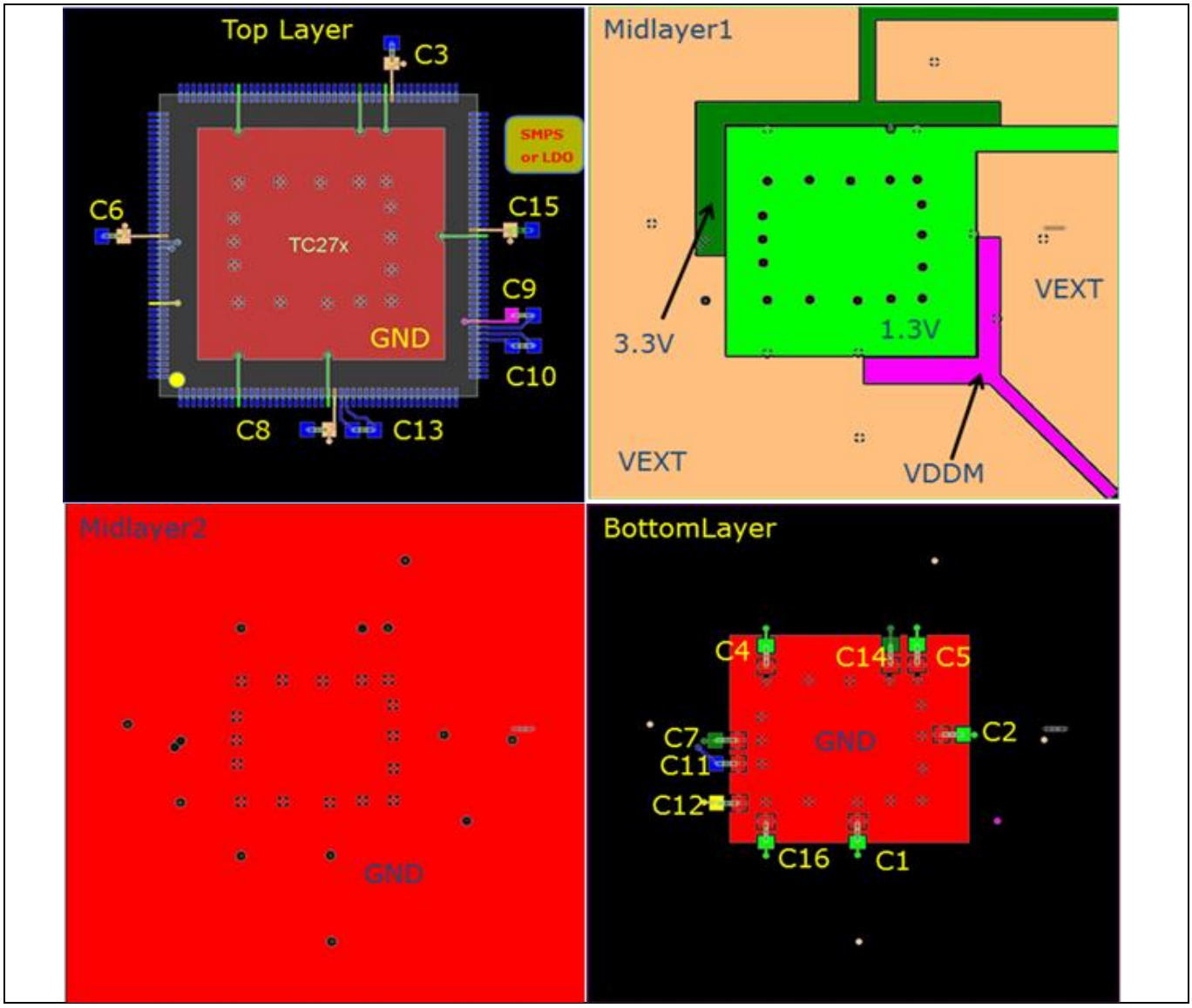


Figure 21 Example layout for LQFP-176 package

Table 12 De-coupling capacitor list for LQFP-176 package for external supply mode

Capacitor	Value	Supply	LQFP-176 pin
C1, C2, C4, C5	4 x 100nF	V_{DD}	24, 68, 123, 100
C3, C6, C8, C15	4 x 100nF	V_{EXT}	25, 69, 99, 153
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply configuration	V_{DDP3}	154
C14	1 x 330nF	V_{DDOSC3}	104
C11	1 x 100nF	V_{DDFL3}	155
C16	1 x 100nF	V_{DDSTBY}	10
C9	1 x 100nF	V_{DDM} / V_{SSM}	54 / 53
C10	1 x 100nF	V_{AREF1} / V_{AGND1}	52 / 51
C13	1 x 100nF	V_{AREF2} / V_{AGND2}	26 / 27
C12	1 x 100nF	V_{FLEX}	164

6.1.5 Example layout for LQFP-144 package

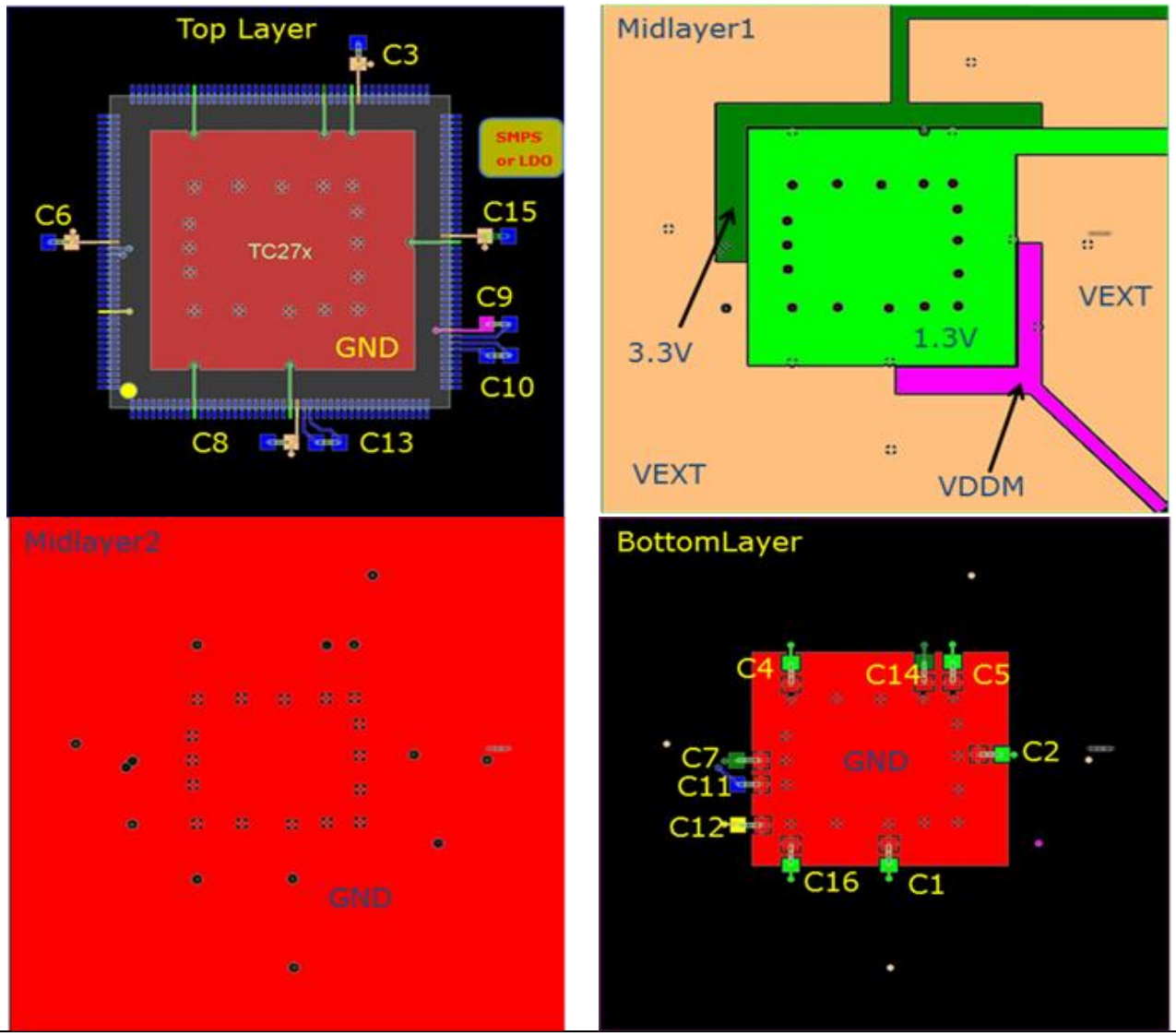


Figure 22 Example layout for LQFP-144 package

Table 13 De-coupling capacitor list for LQFP-144 for external supply mode

Capacitor	Value	Supply	LQFP-144 pin
C1,C2,C4,C5	4 x 100nF	V_{DD}	22, 58, 99, 79
C3,C6,C8,C15	4 x 100nF	V_{EXT}	23, 59, 78, 125
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply configuration	V_{DDP3}	126
C14	1 x 330nF	V_{DDOSC3}	83
C11	1 x 100nF	V_{DDFL3}	127
C16	1 x 100nF	V_{DDSTBY}	10
C9	1 x 100nF	V_{DDM} / V_{SSM}	44 / 43
C10	1 x 100nF	V_{AREF1} / V_{AGND1}	42 / 41
C13	1 x 100nF	V_{AREF2} / V_{AGND2}	24 / 25
C12	1 x 100nF	V_{FLEX}	136

6.2 Example layouts for TC23x, TC22x, TC21x

These microcontroller options have the following supply domains:

- VDD=1.3V for Core
- VDDP3=3.3V for I/O Pad
- VDDM=3.3V or 5V for ADC

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

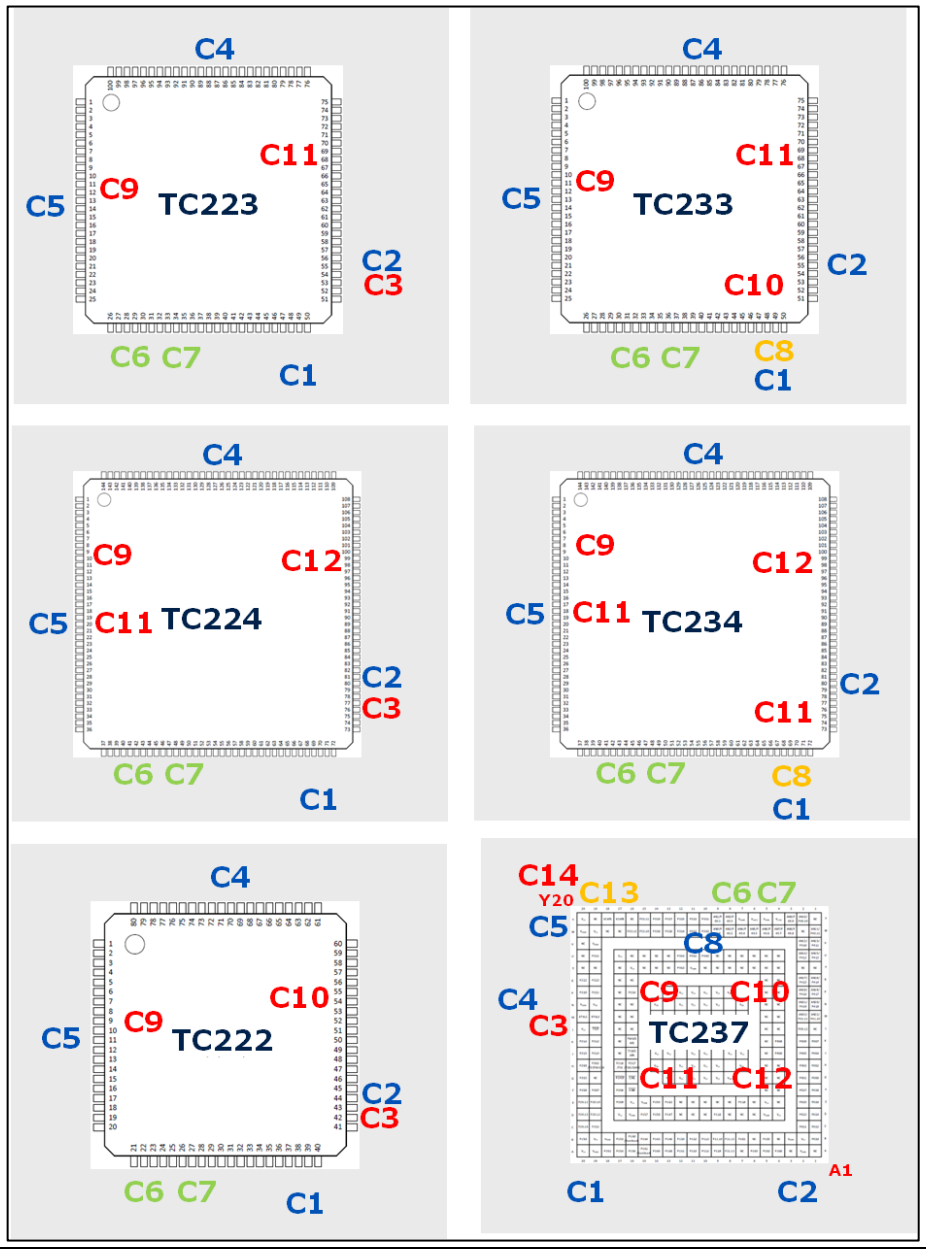


Figure 23 De-coupling capacitor placement overview according to the layout examples for TC22x and TC23x in figures 9 -12 (C8 / C13: Flying capacitor for SMPS mode)

6.2.1 Example layout for LFBGA-292 package

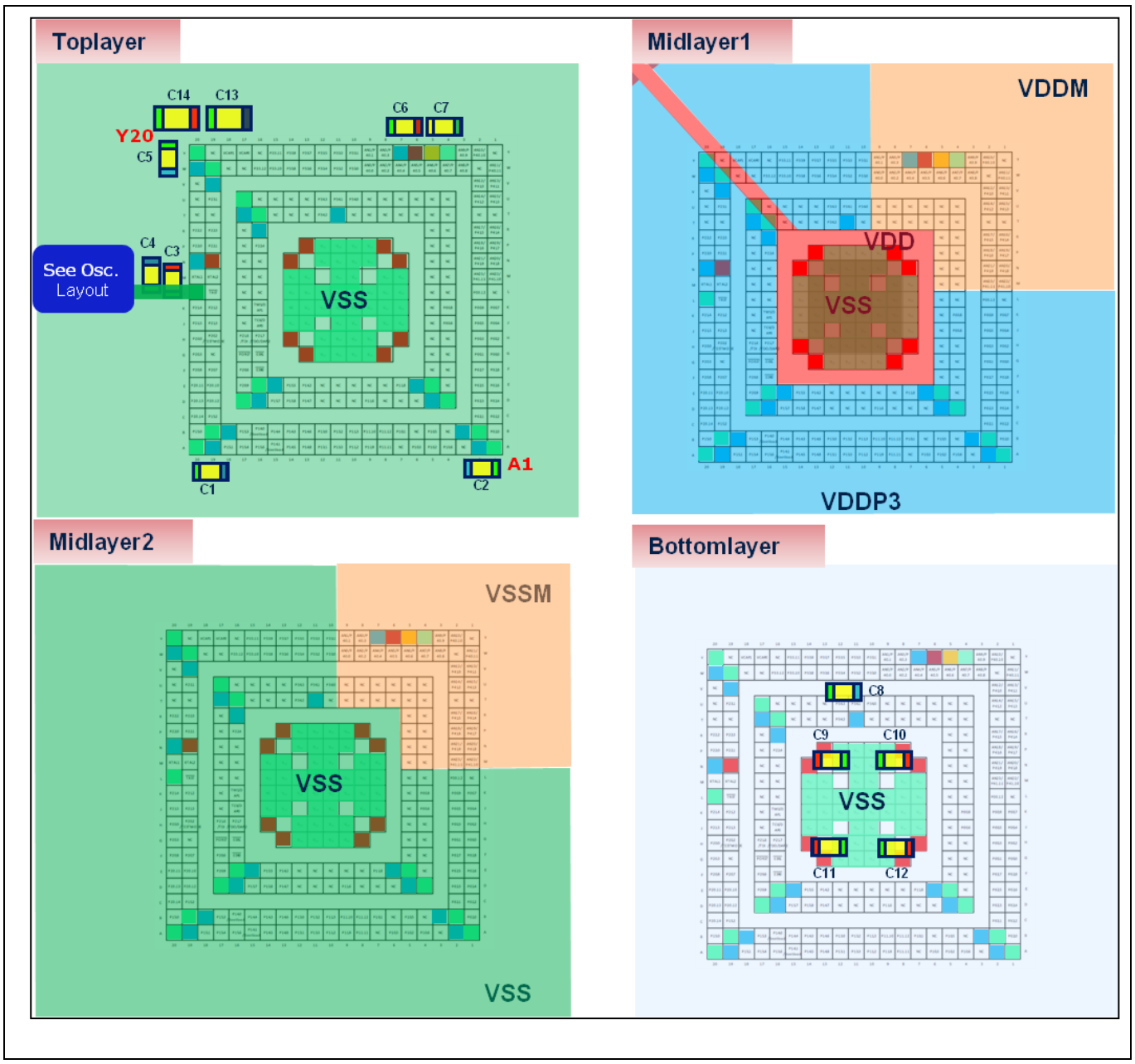


Figure 24 LFBGA-292 package

Table 14 De-coupling capacitor list for LFBGA-292 package

Capacitor	Value	Supply	LFBGA-292 pin
C3, C9, C10, C11, C12	5 x 100nF	V_{DD}	N19//L20, N14+P13//M13+N12, N7+P8//M8+N9, G8+H7//J8+H9, G13+H14//H12+J14
C14	1 x 2.2uF for LDO mode 1 x 10uF for SMPS mode	V_{DD}	VDD Plane
C4	1 x 330nF	V_{DDP3}	N20//L20
C1	1 x 100nF	V_{DDP3}	A19//A20, B18//B19, D16//D17, E15//E16
C2	1 x 100nF	V_{DDP3}	A2//B2, B3//B2, D5//D4
C5	1 x 100nF for external supply mode 1 x 4.7uF for SMPS mode	V_{DDP3}	W20// Y20, V19//W19
C8	1 x 100nF	V_{DDP3}	T11//P11
C7	1 x 100nF	V_{DDM} / V_{SSM}	Y5//Y4
C6	1 x 100nF	V_{AREF} / V_{AGND}	Y6//Y7
C13	1 x 1uF only for SMPS mode	V_{CAP0} /V_{CAP1}	Y17//Y18

6.2.2 Example layout for TQFP-144 package

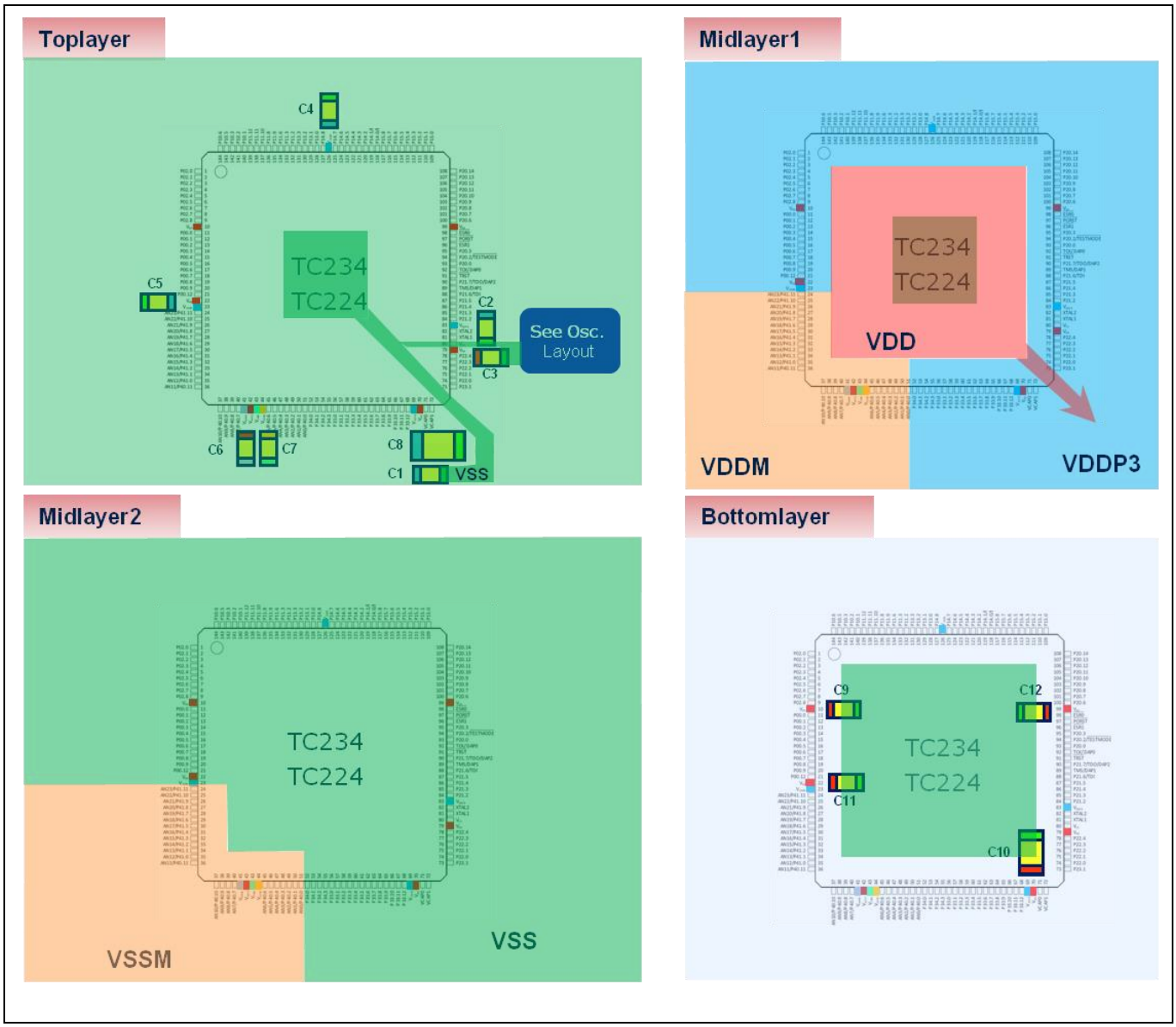


Figure 25 TQFP-144 package

Table 15 De-coupling capacitor list for TQFP-144 package

Capacitor	Value	Supply	TQFP-144 pin
C12, C9, C11	3 x 100nF	V_{DD}	99, 10 (VDDSB for ADAS device), 22
C3	1 x 2.2µF for TC224 with LDO mode 1 x 100nF for all other cases	V_{DD}	79
C10	1 x 100nF for TC234 for external supply mode 1 x 2.2uF for TC234 for LDO mode 1 x 10uF for TC234 for SMPS mode	V_{DD}	70
C2	1 x 330nF	V_{DDP3}	83
C1	1 x 4.7uF for TC234 in SMPS mode 1 x 100nF for all other cases	V_{DDP3}	69
C4, C5	2 x 100nF	V_{DDP3}	126, 23
C8	1 x 1uF for TC234 in SMPS mode No cap required for all other cases	V_{CAP0}-V_{CAP1}	71//72
C6	1 x 100nF	V_{AREF}//V_{AGND}	41//42
C7	1 x 100nF	V_{DDM} //V_{SSM}	44//43

6.2.3 Example layout for TQFP-100 package

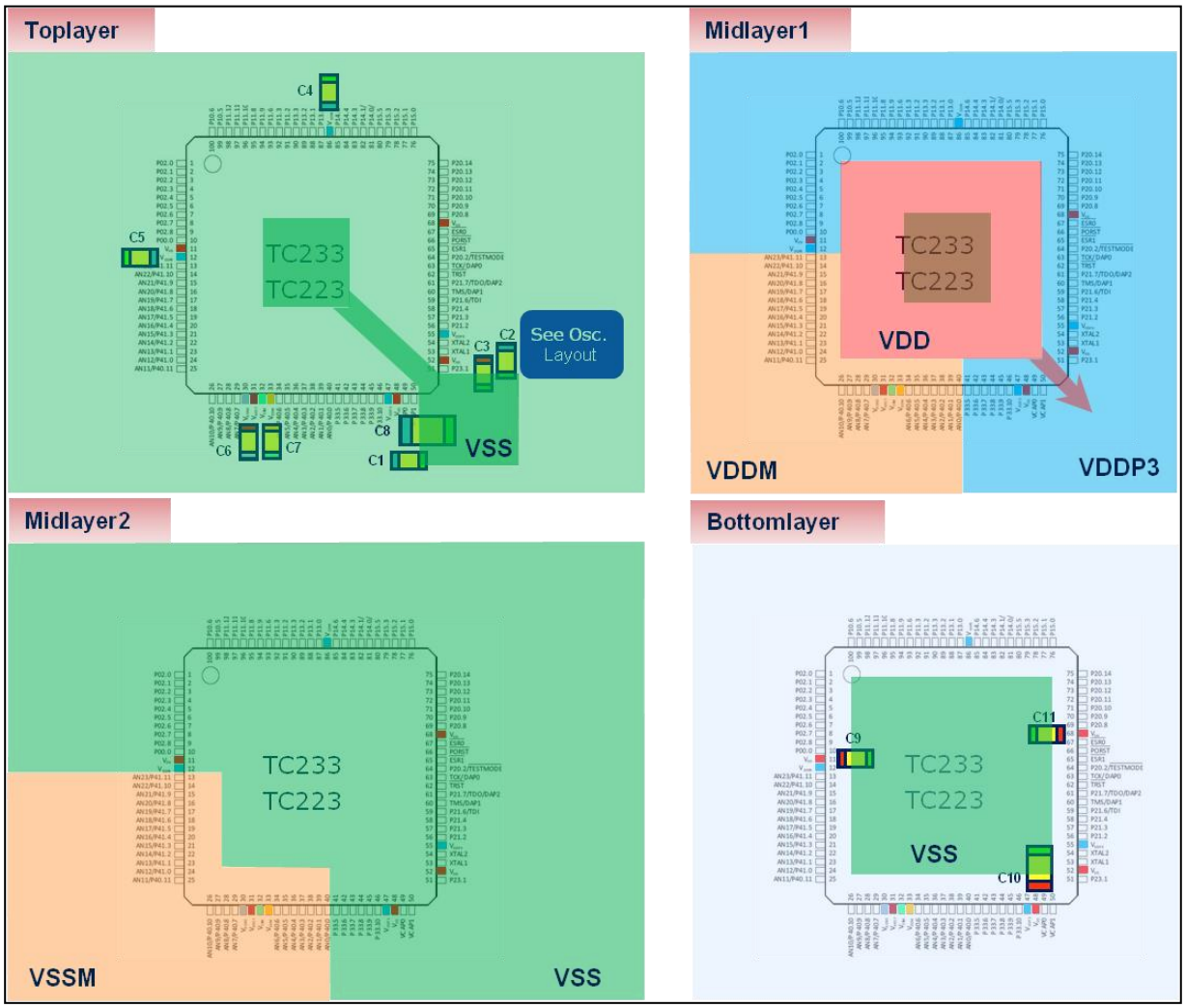


Figure 26 TQFP-100 package

Table 16 De-coupling capacitor list for TQFP-100 package

Capacitor	Value	Supply	TQFP-100 pin
C9, C11	2 x 100nF	V_{DD}	11, 68
C3	1 x 100nF for TC223 in external supply mode 1 x 2.2uF for TC223 in LDO mode	V_{DD}	52
C10	1 x 100nF for TC233 in external supply mode 1 x 2.2uF for TC233 in LDO mode 1 x 10uF for TC233 in SMPS mode	V_{DD}	48
C2	1 x 330nF	V_{DDP3}	55
C4, C5	2 x 100nF	V_{DDP3}	86, 12
C1	1 x 100nF for external supply mode 1 x 4.7uF for SMPS mode	V_{DDP3}	47
C6	1 x 100nF	V_{AREF}//V_{AGND}	31//30
C7	1 x 100nF	V_{DDM}//V_{SSM}	33//32
C8	1 x 1uF only for TC233 in SMPS mode	V_{CAP0}-V_{CAP1}	49, 50

6.2.4 Example layout for TQFP-80 package

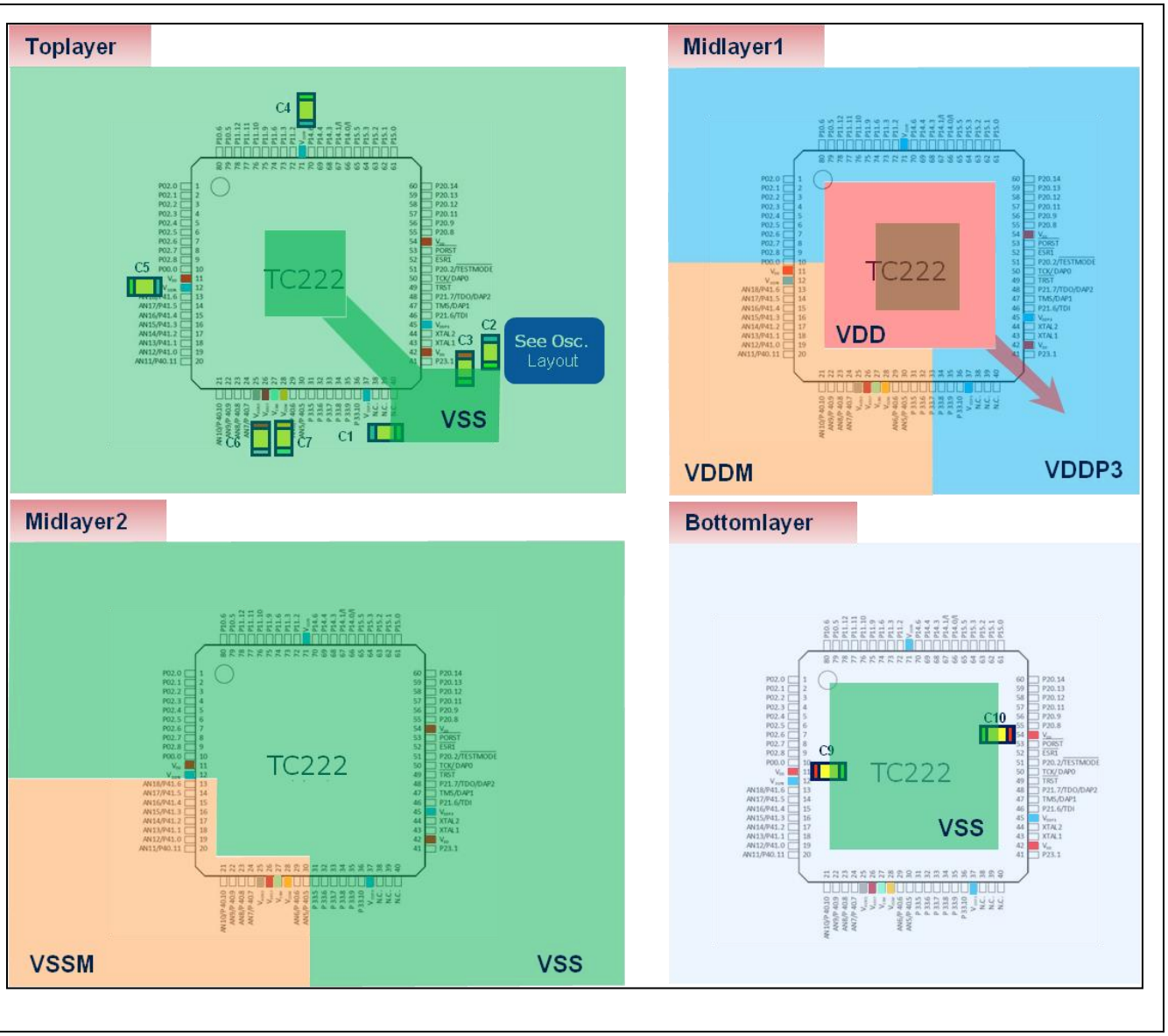


Figure 27 TQFP-80 package

Table 17 De-coupling capacitor list for TQFP-80 package

Capacitor	Value	Supply	TQFP-80 pin
C9, C10	2 x 100nF	V_{DD}	54, 11
C3	1x 100nF for external supply mode 1x 2.2uF for LDO mode	V_{DD}	42
C4, C5	2 x 100nF	V_{DDP3}	71, 12
C1	1 x 100nF	V_{DDP3}	37
C2	1 x 330nF	V_{DDP3}	45
C6	1 x 100nF	V_{AREF}//V_{AGND}	26//25
C7	1 x 100nF	V_{DDM}//V_{SSM}	28//27

Acronyms and abbreviations

Table 18

Term	Definition
ADC	Analog-to-Digital Converter
AGBT	Aurora Gigabit Trace (Interface)
BGA	Ball Grid Array (Package)
DAP	Debug Access Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EME	Electro Magnetic Emission
EMI	Electro Magnetic Interference
ESR	External Service Request (pin ESRx)
EVR	Embedded Voltage Regulator
GPIO	General Purpose Input Output
HSCT	High Speed Communication Tunnel (module)
HSSI	High Speed Serial Interface (Link)
LDO	Low Drop Out (Voltage regulator)
LVDS	Low Voltage Differenetial Interface
MSC	Micro Second Channel
OCDS	On-chip Debug Support
PCB	Printed Circuit Board
PLL	Phased Locked Loop
PWM	Pulse Width Modulation
QFP	Quad Flat Package
QSPI	Queued Synchronous Peripheral Interface
RAM	Random Access Memory
SMPS	Switched Mode Power Supply (Voltage regulator)

Revision history

Document version	Date of release	Description of changes
V1.0	2016-03	First release

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Edition 2016-03

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

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Document reference
AP32469

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