Synchronous buck converter with XMC™ Digital Power Explorer Kit

XMC1300, XMC4200

About this document

Scope and purpose
This application note provides information on how a synchronous buck converter can be implemented with either the XMC4000 or XMC1000 devices. The XMC™ Digital Power Explorer Kit is used as an example to illustrate the implementation of the buck converter in both voltage mode control and peak current mode control.

Applicable products
XMC1000 and/or XMC4000 microcontroller family
XMC™ Digital Power Explorer Kit

References
Infineon: DAVE™ - http://www.infineon.com/DAVE
Infineon: XMC™ family - http://www.infineon.com/XMC
Introduction to digital power conversion application guide - http://www.infineon.com/xmc_dp_exp
The example codes supplied can be downloaded from - http://www.infineon.com/xmc_dp_exp

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1 Overview

A buck converter (Figure 1) is a DC-DC converter topology that is only able to generate a lower output voltage (V_{OUT}) than the input voltage (V_{IN}). Accordingly, the buck converter is also called “step-down” converter. The DC-DC conversion is *non-isolating*, meaning that there is a common ground between input and output.

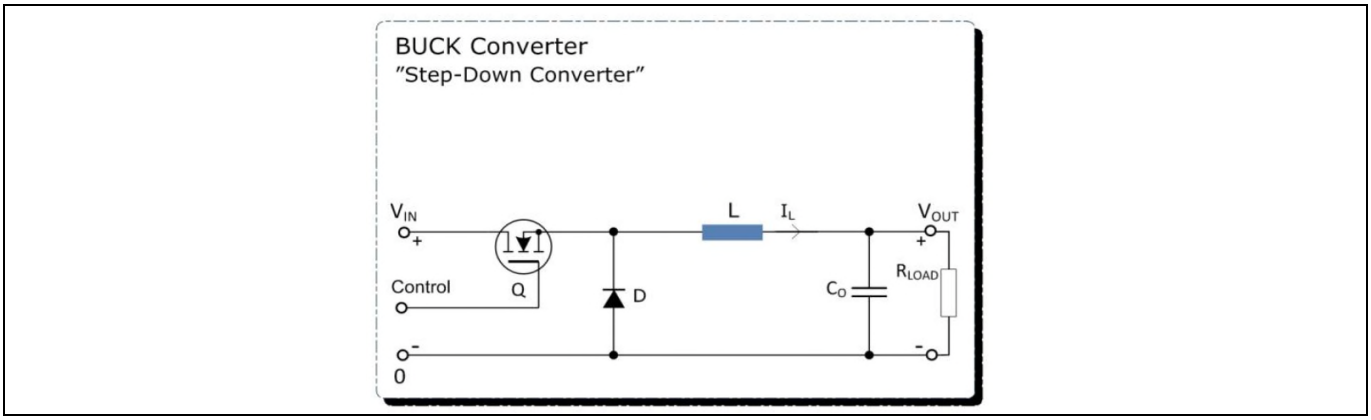

Figure 1 Buck converter

Several improvements of this topology are already widely used. When load current increases, power losses through the diode (V_F*I_D) increase. If better efficiency values are required, the rectifying diode (D) may be replaced by an active switch with a lower voltage drop (resulting in a synchronous buck converter topology). With such a solution the rectification will be synchronously controlled by a signal that is complementary to the control signal (PWM). See Figure 2.

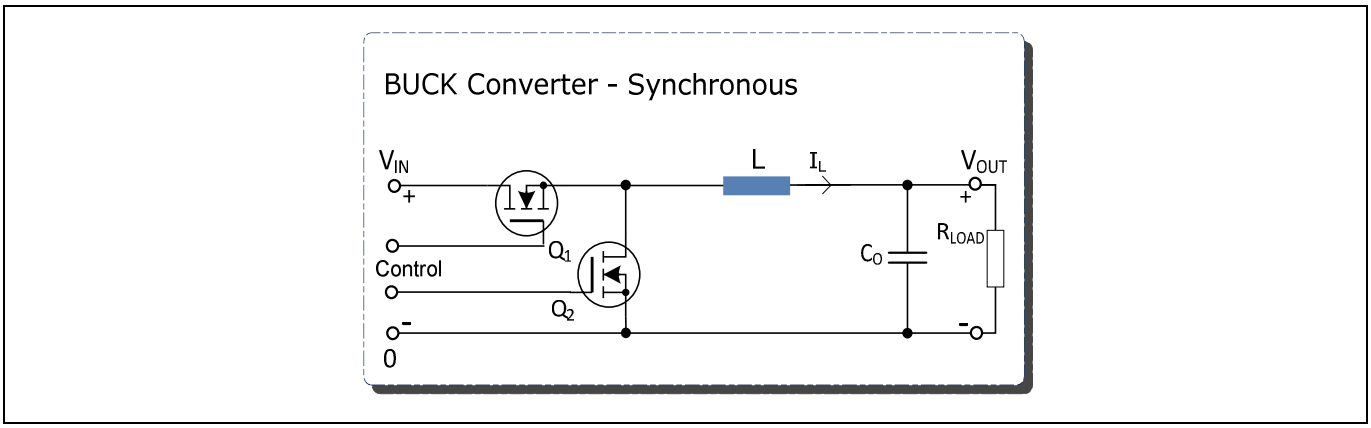

Figure 2 Synchronous buck converter

Synchronous buck converters have received a lot of attention in low voltage DC-DC converter applications because they can offer high efficiency, provide more precise output voltage and also meet the requirement for small size solutions. Additionally, buck converters are easier to control than other DC-DC topologies and the technology is generally well understood.

Typical applications for synchronous buck converters include server and telecomm power supplies, lighting applications, battery chargers, etc.

This document looks at how and where a synchronous buck converter should be implemented - with either the XMC4000 or XMC1000. The XMC™ Digital Power Explorer Kit is used as a hardware reference for the explanation of examples.

1.1 Types of modulation in a buck converter

In Figure 3, a typical system control diagram for a switch-mode power supply can be seen. The modulator generates the pulses needed to maintain the steady state duty-cycle-to-output-voltage transfer function of the sense-modulate-drive control loop. There is also an output filter, typically comprising an inductor, capacitor(s), a compensator and a voltage reference to regulate the output voltage.

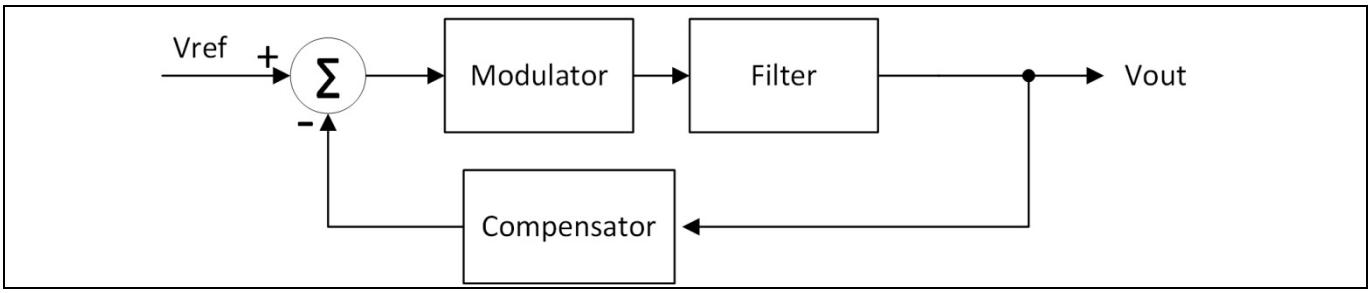

Figure 3 System control diagram

The output of the modulator is a rectangle wave. This rectangle is averaged by the output filter and applied to the load as a DC voltage. The DC voltage is therefore the average of the rectangular pulse waveform

$$V_{out} = \frac{1}{T}\int_0^{t_{on}} V_{in}dt = \frac{V_{in} * t_{on}}{t_{on} + t_{off}}$$

$$V_{out} = V_{in} * D$$

where T is the period, V_{out} is the output voltage, V_{in} is the input voltage, t_{on} is the ON time, t_{off} the OFF time and D is the duty cycle of the PWM ($1 - \frac{t_{off}}{T}$).

Each modulation mode meets different required properties and alters the frequency response of the converter transfer function.

The basic modulation modes (below) can be used in combination to improve performance:

- Voltage control (VC): The feedback function of the voltage control loop modulates the duty cycle of the PWM, so that the target output voltage is maintained.
- Average current control (ACC): The average current of the inductor modulates the duty cycle of the PWM to maintain the output voltage.
- Peak current control (PCC): The steady state duty-cycle-to-output transfer function in peak current control is maintained by two essential control loops - one inherent loop, reacting to limit current detections and one coherent loop that reflects output vs reference deviations, adjusting the limit current.
- Resonant constant ON time with zero crossing detection (ZCD): This technique utilizes a resonant tank circuit to force the current through the semiconductor switch to oscillate, whereby the semiconductor switch turns off at zero current level, drastically reducing switching stresses and losses.

This document will not consider modulation by average current control (ACC) or resonant constant ON time.

1.2 Voltage versus current mode control in a buck converter

Voltage mode control implies that the actual output voltage error ($V_{measured}$-V_{target}) controls the voltage applied across the inductor. See Figure 4

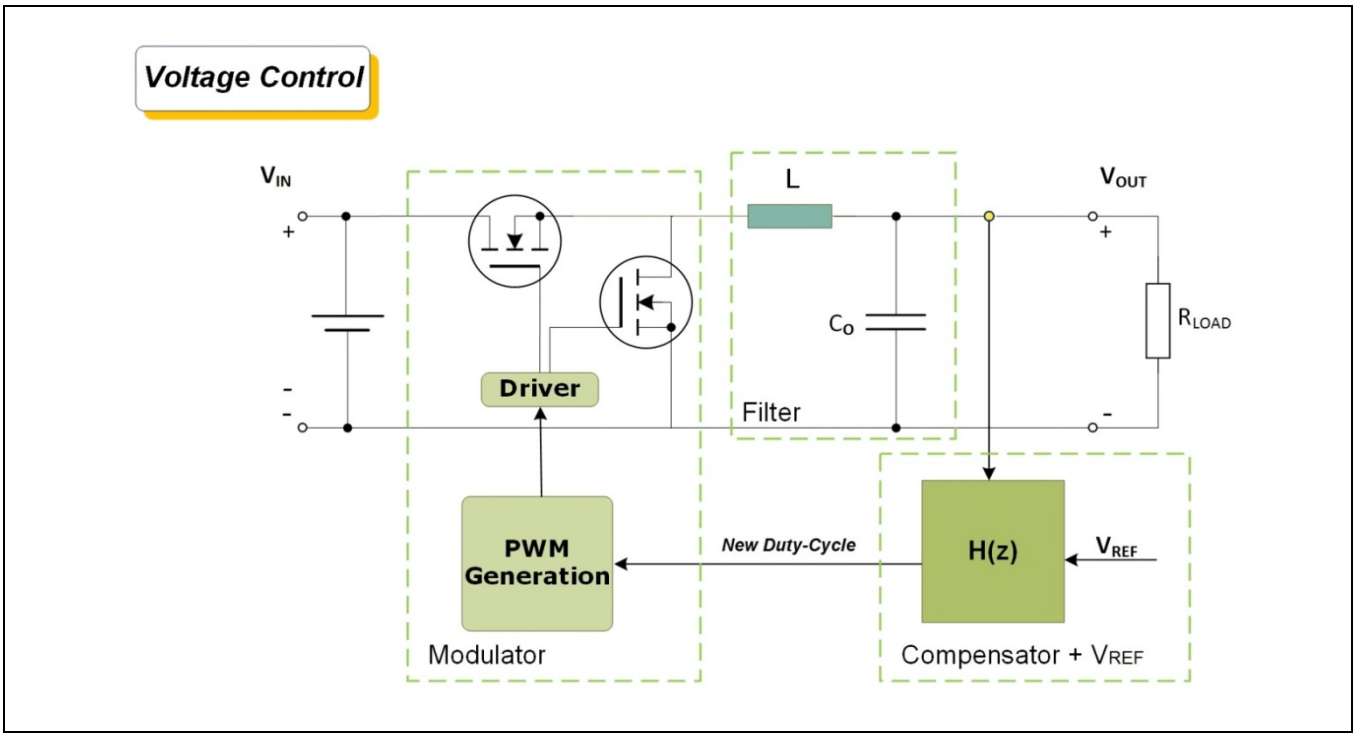

Figure 4 Synchronous buck converter with voltage control mode

Current mode control implies that the actual output voltage error ($V_{measured}$-V_{target}) controls the peak current through the inductor.

The current mode control features a dual loop control circuit—an outer loop (VCM) and an inner loop (current loop within a voltage loop). See Figure 5.

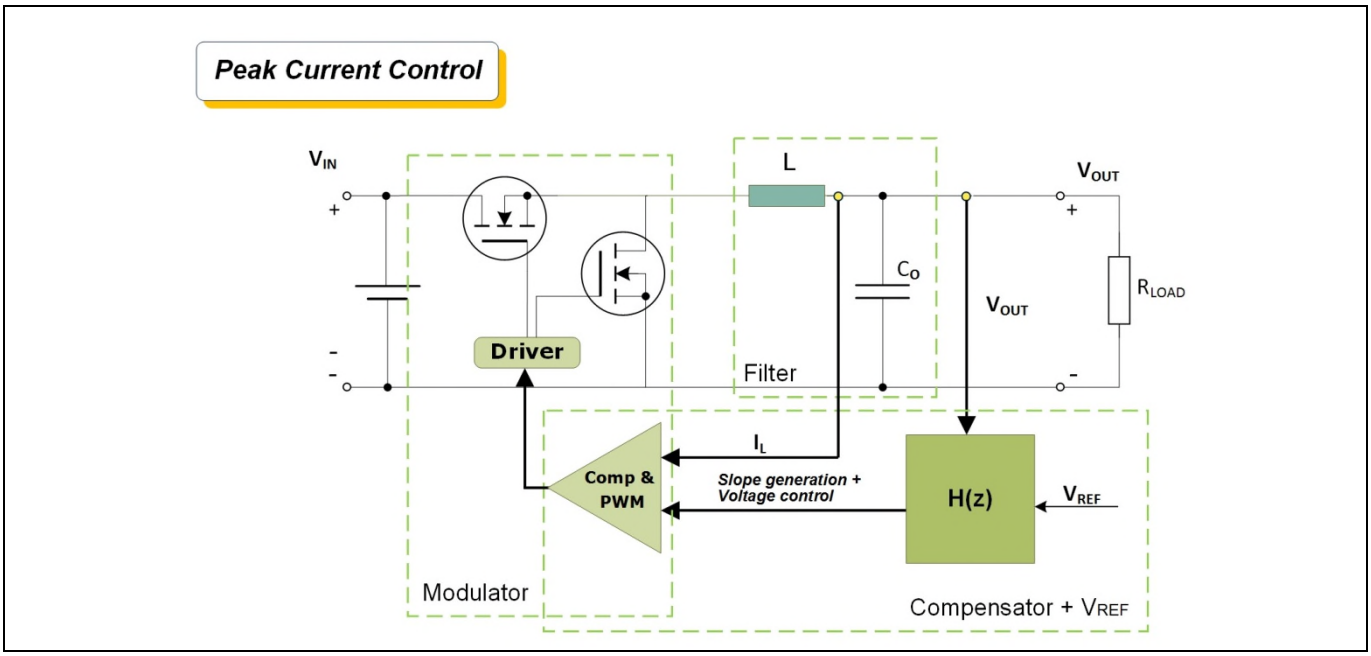

Figure 5 Synchronous buck converter with peak current control mode

Table 1 compares the advantages and drawbacks of each mode.

Table 1 Comparison of PCC and VCM

	Peak current control mode	Voltage control mode
Noise sensitivity	High noise sensitivity	Low noise sensitivity
Cost	Higher cost	Lower cost
Resolution	Resolution limited by the comparator reference resolution	Resolution limited by PWM timer clock
Easiness of feedback design	Control stabilization issues at duty cycles > 50%: Requires slope compensation to reject sub-harmonic oscillations	Easy feedback design
Response to condition changes	Responds immediately to input voltage changes. Cannot handle very wide input voltage variations	Relatively slow response to input/output condition changes
Current limiting	Inherent cycle by cycle current limiting	Requires additional current protection (comparator)

2 XMC™ key features

XMC™ family microcontrollers have embedded peripherals that bring significant benefits to the required functions of a digitally controlled buck converter.

XMC4x devices:

- ARM® Cortex™-M4F with DSP instructions
- Extended temperature range, up to 125 °C
- Up to 2 MB embedded flash with 22 ns access time and error correction unit

XMC1x devices:

- ARM® Cortex™-M0
- Control peripherals such as PWM timers run at speeds up to 96 MHz
- The MATH co-processor boosts standard Cortex™-M0 computing performance accelerating divisions and trigonometric operations such as SIN and COS[1]

The peripherals used for a buck converter are:

- CCU8 – PWM generation [2]
- HRPWM – high resolution PWM generation (XMC4400, XMC4200, XMC4100) [3]
- VADC – sensing of input and output voltages [4]
- CSG – comparator and slope generator for peak current detection (XMC4400, XMC4200, XMC4100) [3]
- ACMP – analog comparator for peak current detection (XMC1300, XMC1200) [5]

[1] Math Coprocesor(MATH) Application Note, http://www.infineon.com/xmc
[2] CCU8 training material, http://www.infineon.com/xmc
[3] HRPWM training material, http://www.infineon.com/xmc
[4] Versatile Analog to Digital Converter (VADC) Application Note, http://www.infineon.com/xmc
[5] ACMP training material, http://www.infineon.com/xmc

2.1 CCU8-PWM generation

The CCU8 is a multi-purpose timer unit for signal monitoring/conditioning and pulse width modulation (PWM) signal generation. It is designed with repetitive structures with multiple timer slices that have the same base functionality. The internal modularity of the CCU8 translates into a software friendly system for fast code development and portability between applications. Each CCU8x has four 16-bit timer slices CC8y (y=3-0), which can be concatenated up to 64-bit.

Each slice has:

- 1 timer
- 4 capture registers
- 1 period register
- 2 compare registers

XMC™ key features

The numerous key features for a flexible PWM generation scheme make it the perfect peripheral for PWM generation in switch-mode power supplies. Key features include:

- Each timer slice of the CCU8 can operate in center aligned or edge aligned mode
- Additional operation modes such as single shot, counting or dithering modes are also available
- Complementary PWM signal generation with dead time
- HW asymmetric PWM generation for multichannel/multi-phase pattern generation with parallel updates
- Additional externally controllable functions give an additional degree of PWM manipulation (e.g. timer gate, timer load, timer clear, etc.)
- HW TRAP generation
- Both the period and compare registers have shadow registers
- Each slice can work independently and in different modes, and still be synchronized to other CCU8 slices. See Chapter 2.1.1

As a result of these features the CCU8 timer slices are used to drive the synchronous buck converters. See Figure 6 for examples of CCU8 usage.

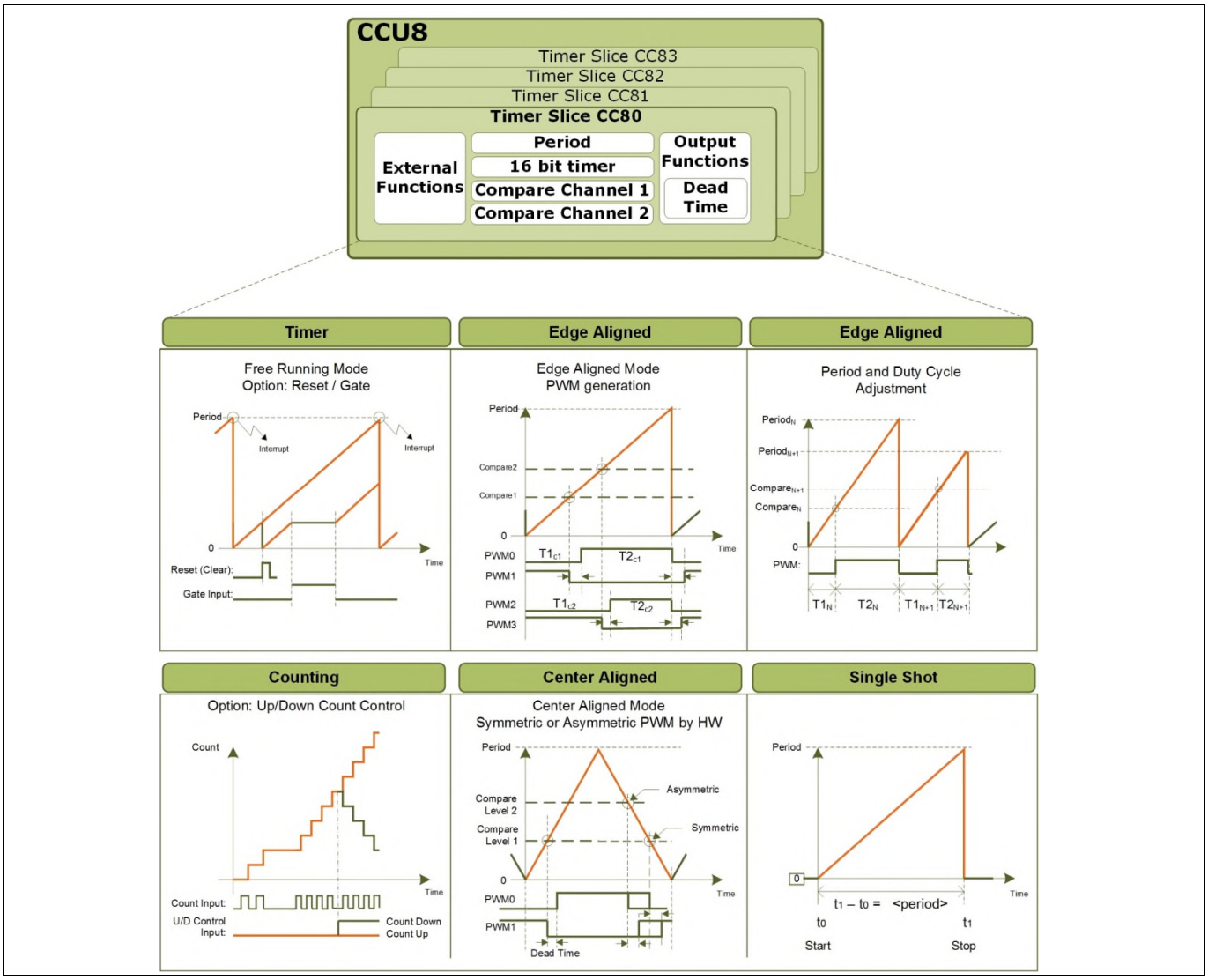

Figure 6 CCU8 flexible PWM generation scheme

2.1.1 Single channel PWM with complementary outputs for synchronous buck

A single compare channel of CC8y timer slice is used to output a complementary PWM signal pair in edge-aligned mode. Dead time is inserted on the rise time. See Figure 7

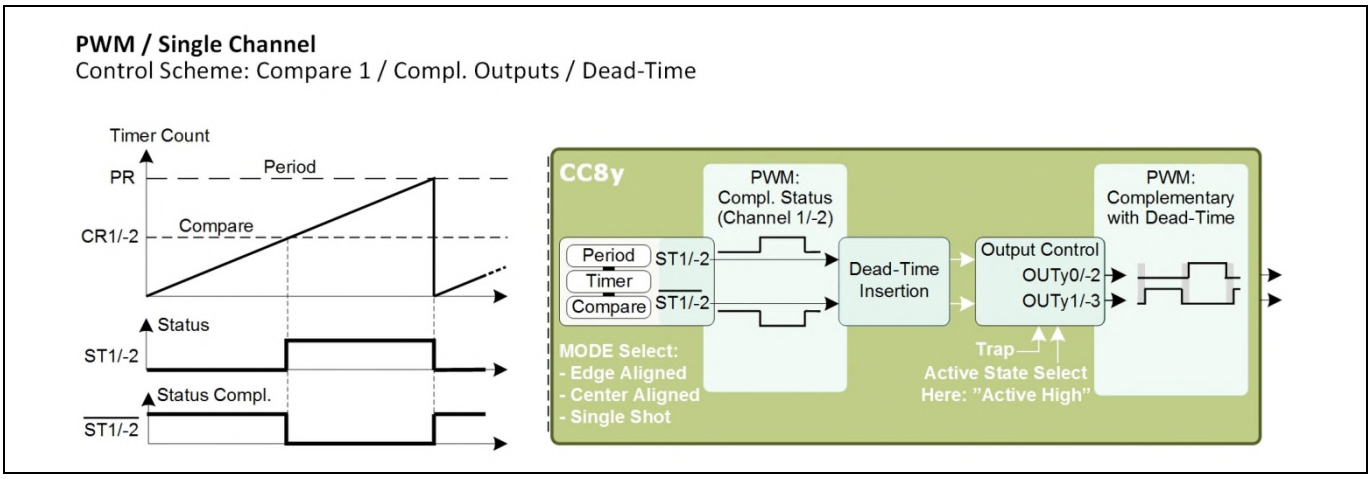

Figure 7 PWM single channel with complementary outputs

2.1.2 High resolution PWM generation

The high resolution PWM generator (150 ps) is an essential module for cutting edge / optimized switch-mode power supply applications development.

The XMC44xx/42xx/41xx devices offer high resolution channel (HRC) generation. The high resolution PWM is used together with CC8 slices.

The enhanced PWM resolution is achieved by insertion that shortens or lengthens the original pulse width of the CCU8 slice output pulse, in steps of 150 ps. It can offer a resolution of 10-bits up to 6 MHz PWM. The dynamic dead time insertion feature is available in the HRPWM path.

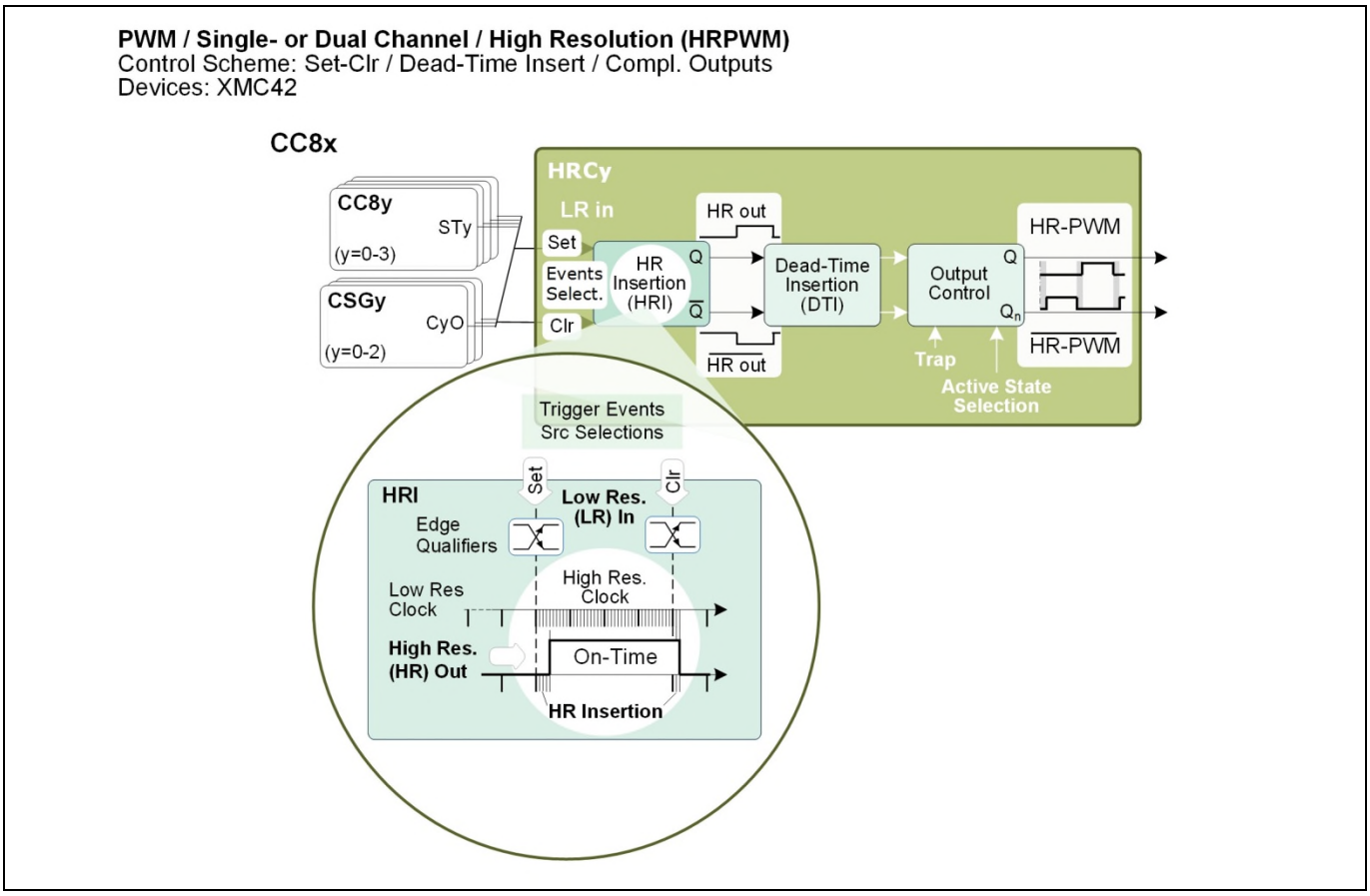

Figure 8 High resolution channel

2.2 Voltage and current sensing - VADC

Input voltage, output voltage and inductor current and all required signals to control a buck converter can be monitored via versatile analog-to-digital converter (VADC) channels in the XMC™ device.

The functionalities of VADC that are useful for digital power control include:

- Automatic scheduling of complex conversion sequences with priority for time-critical conversions
- Synchronous sampling of several analog signals.
- Independent result registers, selectable for 8/10/12 bits, with 16 steps FIFO
- Sampling rates up to 2 MHz (up to 1 MHz for XMC1000 family)
- FIR / IIR filter with selectable coefficients plus accumulation

The VADC module is intelligently connected to other peripherals, such as PWM generation modules, in the MCU. This provides an accurate sampling point for real time applications where the conversion of the analog signals have to be performed in a deterministic way.

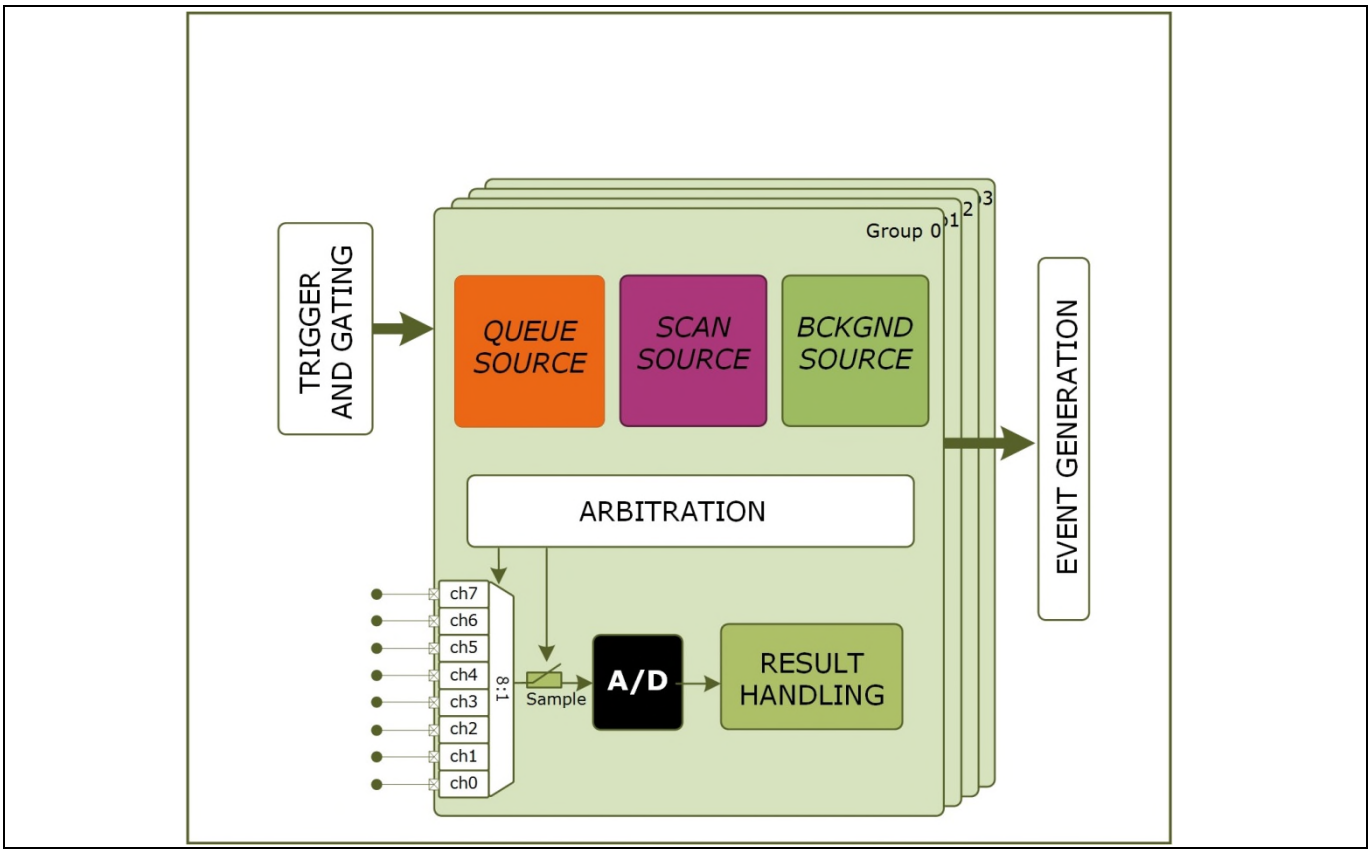

Figure 9 VADC scheme

2.3 Comparator and slope generator (CSG) - XMC4200 MCU

With three high speed comparators and a hardware slope, it is possible to address several power conversion topologies with reduced SW interaction. The comparator and slope generator (CSG) consists of essential factors for several control techniques as shown in Figure 10

- Analog high speed comparator ~20 nsec that can be used to monitor:
  - coil current for current protection or PCC
  - voltage outputs for protection
- Slope generator with high speed DAC (~30 Msample/sec) that can be used to:
  - provide a reference control for the comparator
  - insert a decrementing or incrementing ramp to the comparator for PCC
- Filtering and blanking capabilities to avoid current commutation spikes passing the comparator

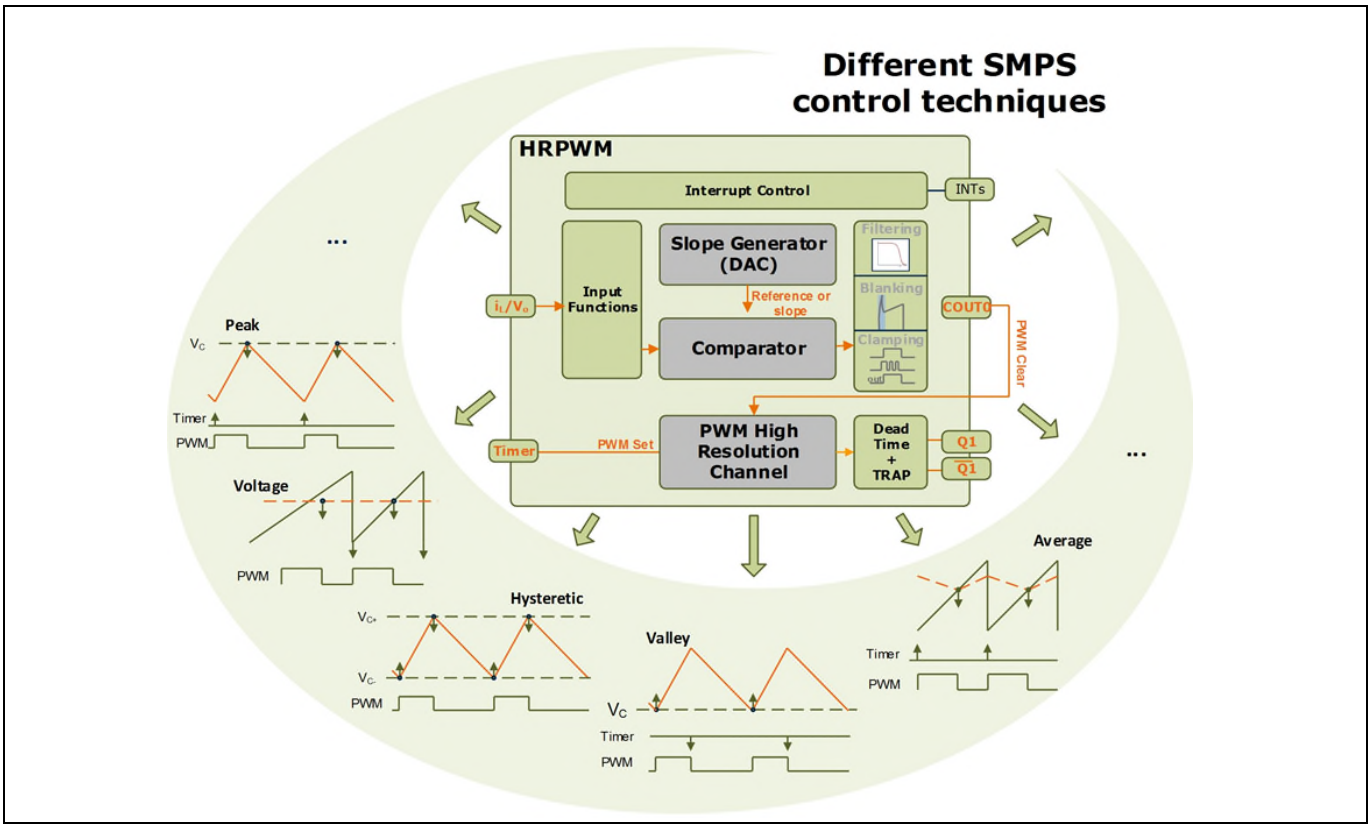

Figure 10 Using the CSG together with the HRC for implementing different SMPS control techniques

2.4 Analog comparator (ACMP) – XMC1300 MCU

The XMC1300 MCU has three analog comparators as well as low input offset voltage (3 mV) and a short propagation delay (25 nsec). These make it ideal for power conversion applications that require real-time and precise signal level comparisons (i. e. for protections or PCC)

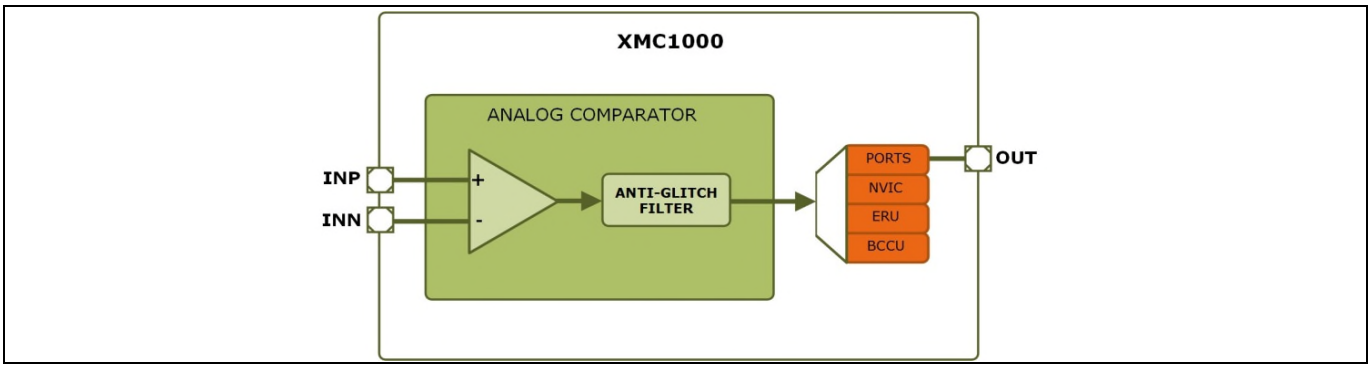

Figure 11 Analog comparator in XMC1000 family

2.5 Event request unit (ERU)

The ERU module can be used to expand the P-to-P connections of the device: ports-to-peripherals, peripherals-to-peripherals and ports-to-ports. It also offers configurable logic that allows the generation of triggers, pattern detection and real-time signal monitoring.

The ERU module is used to expand the peripheral to peripheral connections in the MCU device. For example, in the XMC1300 peak current control project, the hardware connection of the ACMP output to the CCU8 input event is done via the ERU swithcing off the PWM when the comparator trips.

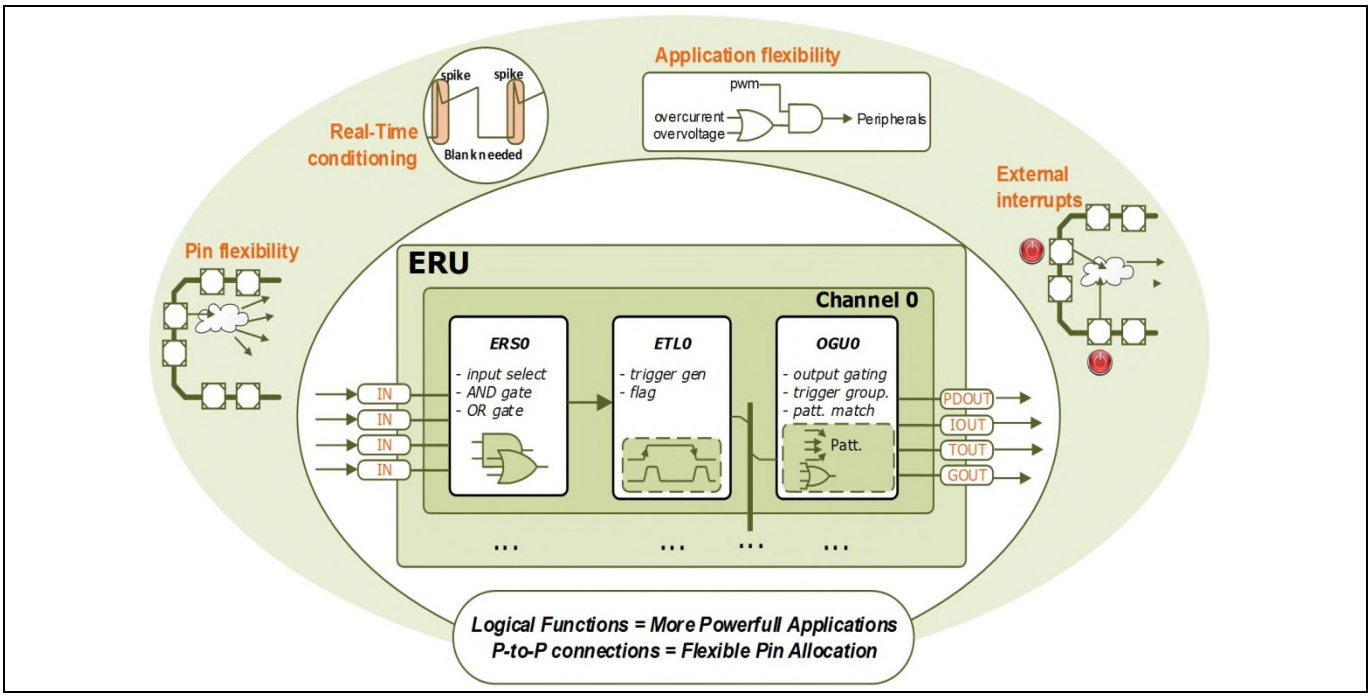

Figure 12 XMC™ peripherals interconnections through ERU

3 XMC™ Digital Power Explorer Kit

The XMC™ Digital Power Explorer Kit is an evaluation kit that demonstrates the wide capabilities of the XMC™ devices. The kit comprises a power board with a synchronous buck converter and 2 different control cards that can be connected to the power board:

- XMC4200 Digital Power Control Card with HRPWM peripheral and ARM® Cortex™-M4F core for high end applications
- XMC1300 Digital Power Control Card with Analog Comparators peripherals and ARM® Cortex™-M0 core for a cost optimized solution

Voltage control mode and current control modes (peak current control with slope compensation) are supported. This allows the user to experiment on both families with a wide variety of control schemes.

The high resolution channels and the comparator slope generation unit in the XMC4200 device extend the capabilities of the associated CCU with features tailored for power conversion.

With the XMC1300 device, lean and cost-saving solutions can be realized with the in-built fast analog comparators (ACMP).

More details on the implementation of the digital buck converter in voltage mode control and peak current mode control can be found in chapters 4 and 5, as well as on the kit web page (http://www.infineon.com/xmc_dp_exp). The software projects are developed in the Infineon DAVE™ development platform, which can be downloaded from the Infineon website.

3.1 Specification

The XMC™ Digital Power Explorer buck converter is targeted for low voltage and the specification is shown in Table 2. The schematic view of the buck converter stage is shown in Figure 3. The target output voltage is 3.3 V although any voltages from 0 V to V_{in} are theoretically possible depending on the driving of the MOSFETs duty cycle. The inductor value ensures continuous conduction mode (CCM) operation of the buck converter so long as any of the load switches (SW2, SW3) are in the “ON” position. In other words, DCM operation occurs only when the SW1 load switch is activated (assuming 200 kHz switching frequency). Nevertheless, the current remains continuous so long as the buck is used in synchronous mode (meaning the low side is active).

Table 2 XMC™ Digital Power Explorer Kit specification

Specification	Value
Input voltage	12 V_{DC}
Output	3.3 V_{DC} (depending on SW)
Maximum output current	2 A
On board load values	3.9 Ω (SW3, SW2)→45% load 22 Ω (SW1)→ 10% load
Main inductor	22 uH
Output capacitor	200 uF || 200 uF→ 400 uF
Gate driver high and low side	IRS2011SPBF (International Rectifier)
Dual MOSFET (high and low side)	BSC0924NDI (Infineon Technologies)

3.2 System block diagram

This chapter gives a brief description of the features and hardware of the XMC™ Digital Power Explorer Kit. The kit consists of:

- XMC™ Digital Power Explorer Board
- XMC4200 Digital Power Control Card
- XMC1300 Digital Power Control Card

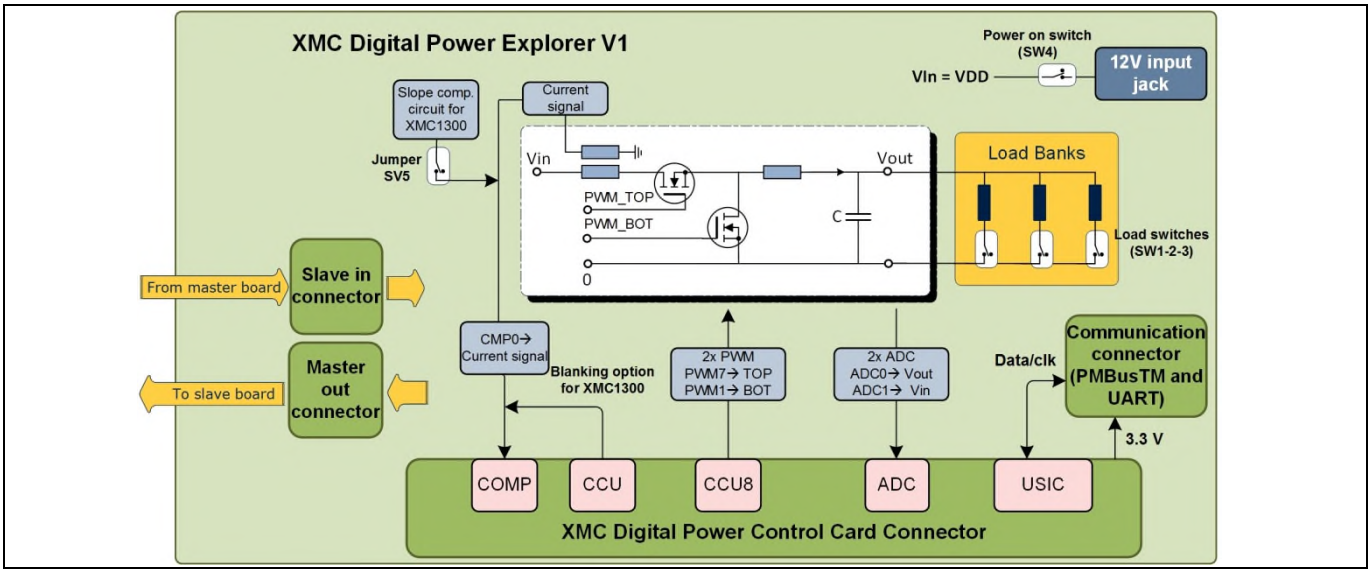

Figure 13 XMC™ Digital Power Explorer Kit system overview

3.2.1 XMC™ Digital Power Explorer Board

Features of the XMC™ Digital Power Explorer Board include:

- Synchronous buck converter
- On-board switches for step load testing
- Connection for PMBus communication
- Network analyzer ready for stability analysis
- Option to connect a second buck for interleaving control (two buck converters, one XMC™)

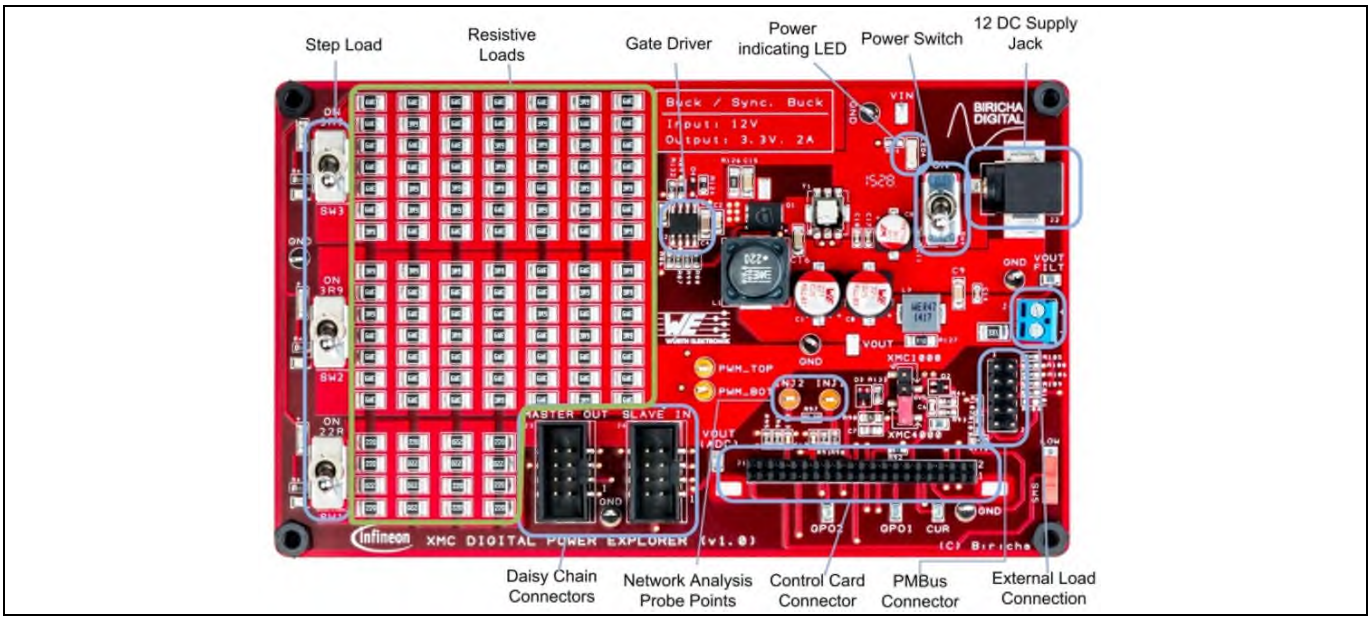

Figure 14 XMC™ Digital Power Explorer Board

3.2.2 XMC4200 Digital Power Control Card

Features of the XMC4200 Digital Power Control Card include:

- XMC4200 (with ARM®Cortex™-M4 based) microcontroller, LQFP64
- Connection to buck board (applicable to other boards) via card edge header
- J-Link debugger and UART virtual COM port, with micro USB connector
- Support 8 PWM pins, 8 ADC pins, 3 CSG pins, selectable via signal conditioning circuit

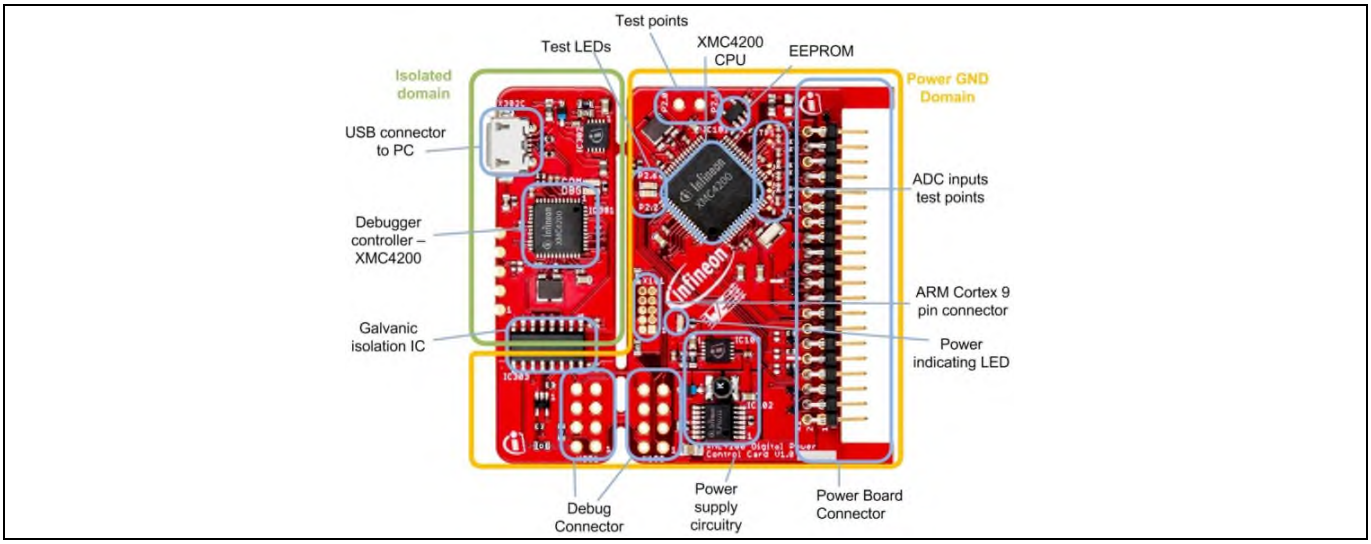

Figure 15 XMC4200 Digital Power Control Card

3.2.3 XMC1300 Digital Power Control Card

Features of the XMC1300 Digital Power Control Card include:

- XMC1302 (with ARM®Cortex™-M0 based) microcontroller, TSSOP38
- Connection to buck board (applicable to other boards) via card edge header
- J-Link Debugger and UART virtual COM port, with micro USB connector
- Support 8 PWM pins, 8 ADC pins, 3 ACMP pins, selectable via signal conditioning circuit

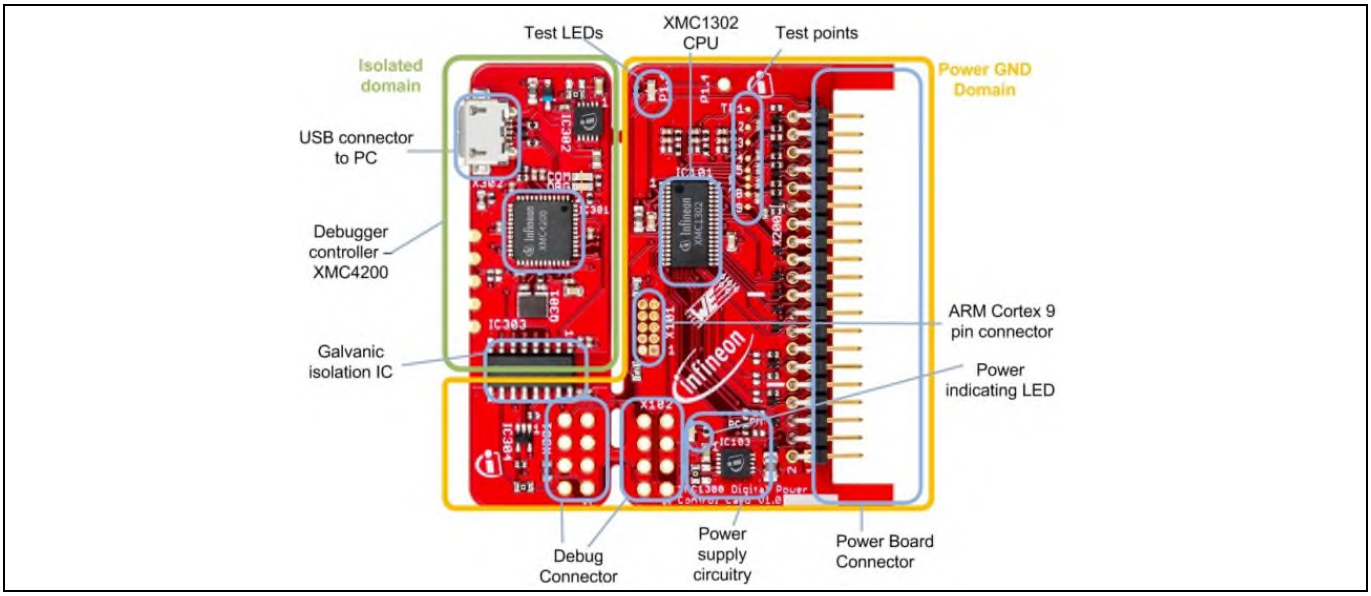

Figure 16 XMC1300 Digital Power Control Card

4 Buck converter voltage control mode (VCM) with XMC™

The steady-state function of a buck converter voltage control is based on $V_{OUT} = D * V_{IN}$. The feedback function of the voltage control loop modulates the duty-cycle (D), so that the output voltage (V_{OUT}) is maintained.

One of the most prominent features of the XMC™ family of devices is the comprehensive interconnectivity matrix within the on-chip peripherals. The VADC and CCU8 modules are highly interconnected and the conversion can be run completely in the background. The start of the conversion is triggered when compare match 2 in CCU8 slice occurs. Once the conversion result is available, an interrupt service request is activated and the voltage control function is executed in software (error cancelation and H(z)-3P3Z). This function updates the CC8y slice compare register. A safe update with no glitches of the PWM occurs due to the shadow transfer mechanism and the duty-cycle of the PWM signal will be updated in the next cycle.

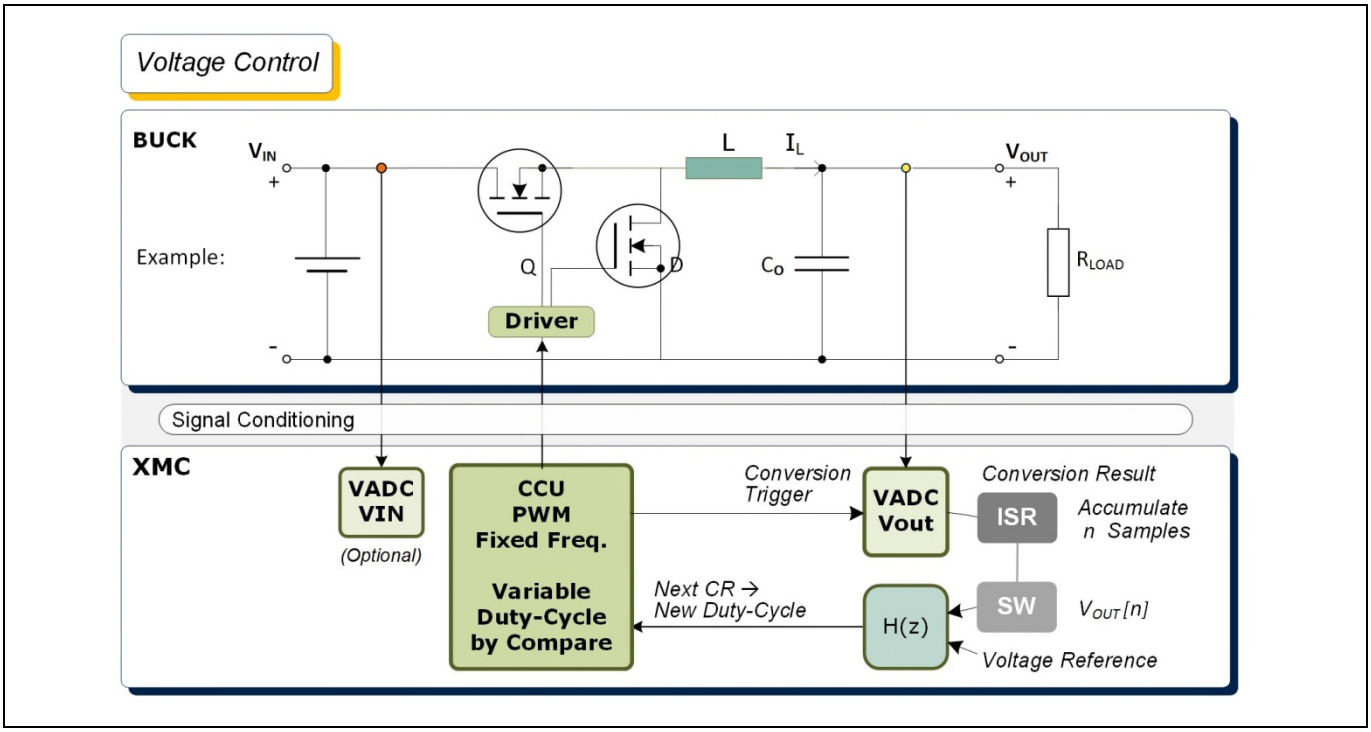

Figure 17 Voltage mode control with XMC™

Timing scheme

The sampling and control loop executes when the PWM switches. In voltage control mode the sensing of inductor current is not required. The waveform of the inductor current is shown in Figure 18.

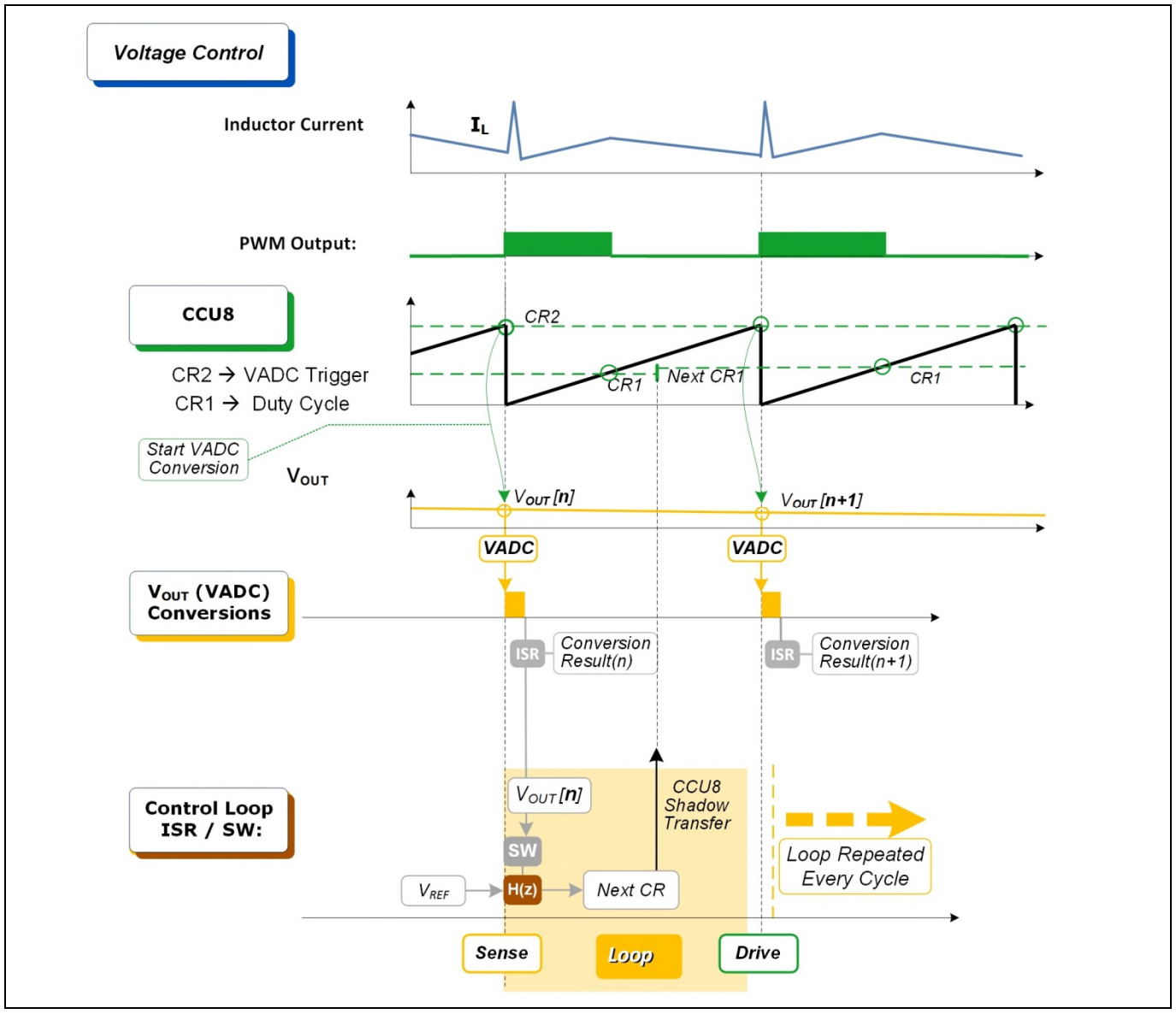

Figure 18 Voltage mode control with XMC™, generic timing diagram

4.1 Compensator design (3P3Z)

The objective of the compensator in the system is to add the necessary mechanism for helping the system output to track a desired reference even in the presence of noise, modeling error or disturbances. A type-3 (3 poles, 3 zeros) filter is one of the most suitable feedback controllers for voltage-controlled buck converters. The poles and zeros of the compensation networks should be placed according to the analysis of the control-to-output transfer function. See Figure 19 and Chapters 4.2.1 and 4.3.1.

Type 3 filters have 3 poles and 2 zeros implementing the following transfer function (H(s)):

$$H_c(s) = \frac{\omega_{p0}}{s} \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right)\left(\frac{s}{\omega_{p3}} + 1\right)}$$

For converting the poles and zeros into the digital domain, the continuous time (s-domain) needs to be converted to the discrete z-domain by using:

$$s = \left(\frac{2}{T}\right)\frac{z-1}{z+1}$$

Having:

$$H_c(z) = \frac{B_3Z^{-3} + B_2Z^{-2} + B_1Z^{-1} + B_0}{-A_3Z^{-3} - A_2Z^{-2} - A_1Z^{-1} + 1}$$

Which, in a linear difference equation:

y[n] = b0x[n] + b1x[n-1] + b2x[n-2] + b3x[n-3] + a1y[n-1] + a2y[n-2] + a3y[n-3]

Where x[n] = reference – feedback

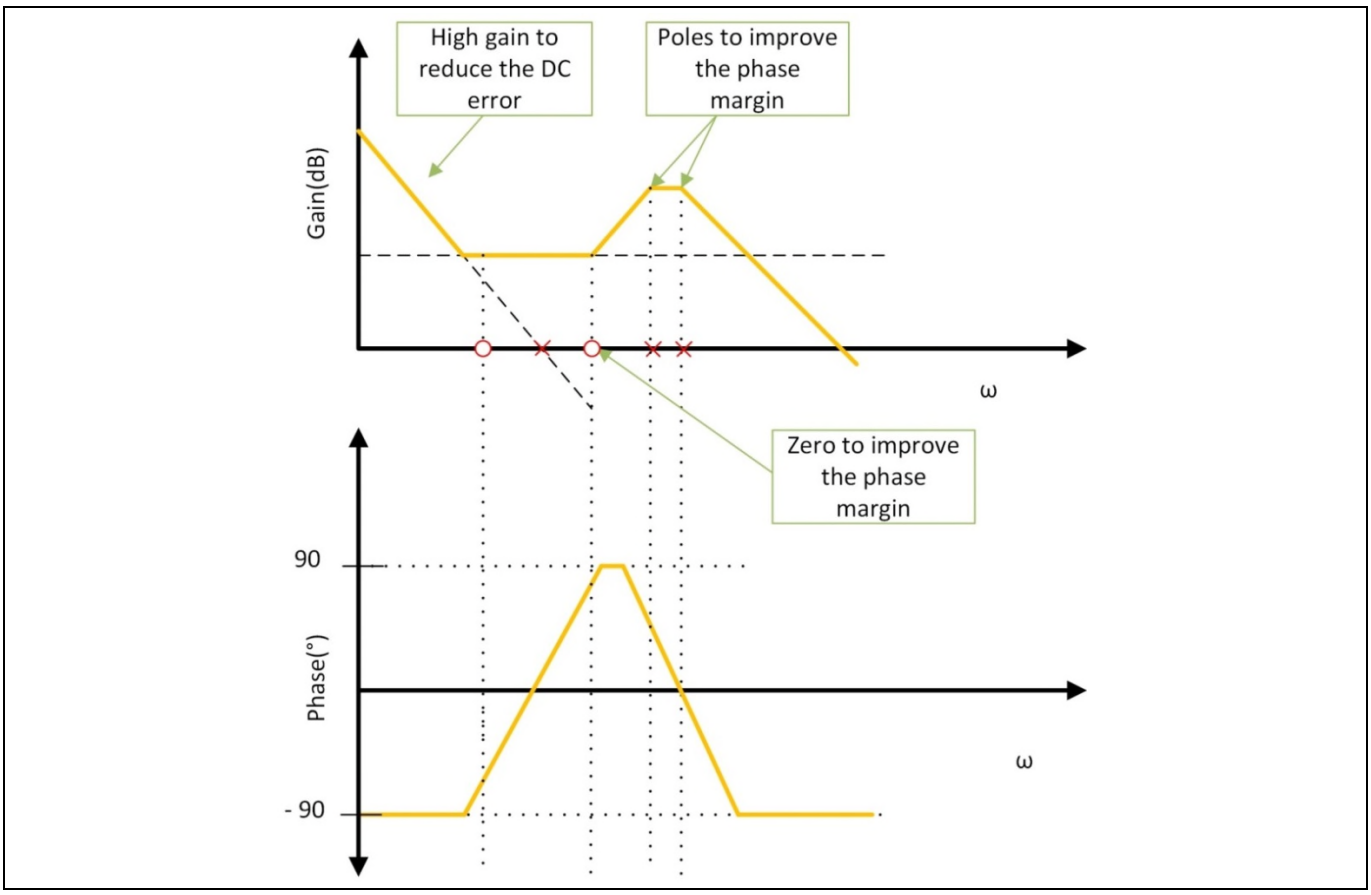

Figure 19 Designing a type 3 compensator (Bode plot).

4.2 XMC4200 VCM implementation example

The boards used are the XMC4200 Digital Power Control Card and XMC™ Digital Power Explorer Board. The voltage control loop is implemented by a classic 3 poles, 3 zeros filter using floating-point values. The filter coefficients are provided and have been selected to have the following controller characteristics:

- Switching freq = 200 kHz
- Crossover freq = 10 kHz
- Phase margin = 50 degrees
- PWM master clock = 80 MHz * 256 (8 bits for HRPWM)
- PWM resolution = 150 ps
- ADC resolution = 12 bits

VADC conversion is continuously triggered by the compare match 2 of CCU8 (set by default to the maximum = period value, although the user can change it to experiment).

Once the output voltage has being measured by the VADC, an interrupt is generated. Inside the ISR, the 3 poles, 3 zeros controller is applied and the value for the duty cycle is updated.

4.2.1 Control specification

The control mode and coefficients selection for the controller have been defined with the help of the WDS tool from Biricha Digital™. The WDS tool allows the user to easily specify the different characteristics of the power system (topology, controller type, control mode, switching frequency, phase margin, crossover frequency, semiconductors…) in order to define the related coefficients and theoretical frequency response. The coefficients can be copied to a DAVE™ project directly from the Infineon tab of WDS tool.

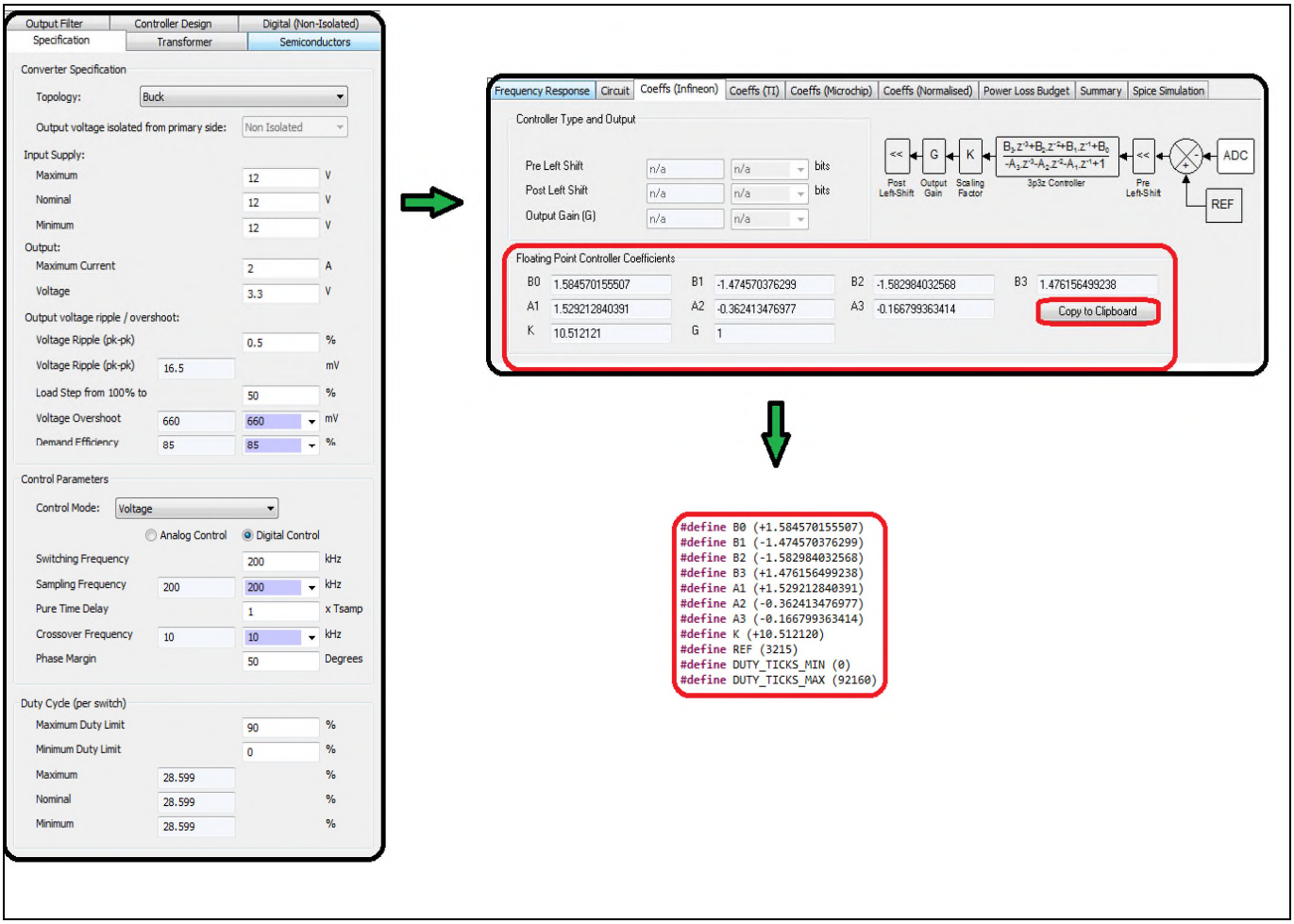

Figure 20 WDS specification and raw floating point coefficients.

4.2.2 Software overview

The software project is developed in the DAVE™ development platform. One instance of each of these DAVE™ (Version 4) APPs has been used to ease the peripheral configuration:

- HRPWM (High resolution PWM, generates the ADC trigger through the CCU8 peripheral and the HRPWM)
- ADC_MEASUREMENT_ADV (output voltage measurement)
- INTERRUPT (NVIC configuration)

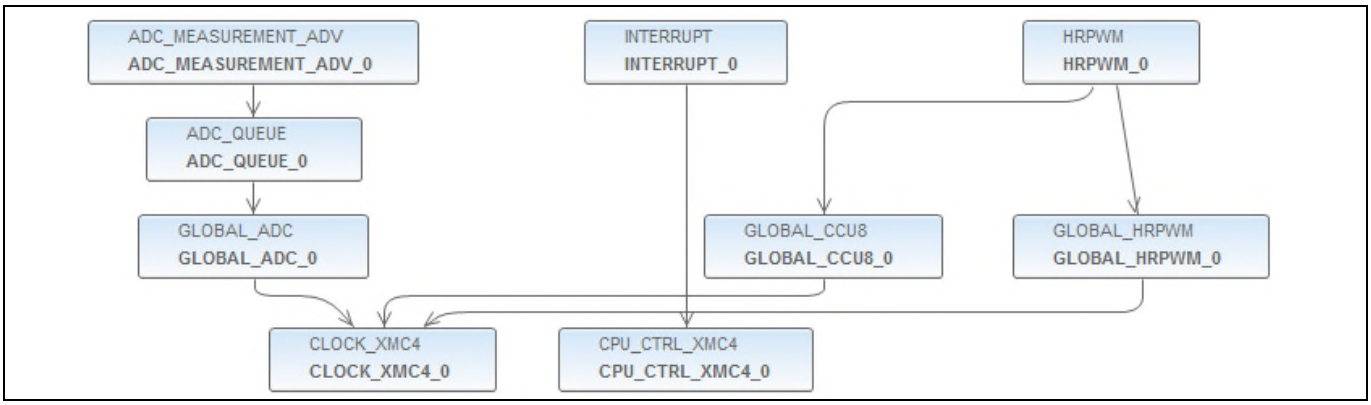

Figure 21 APPs used in the project

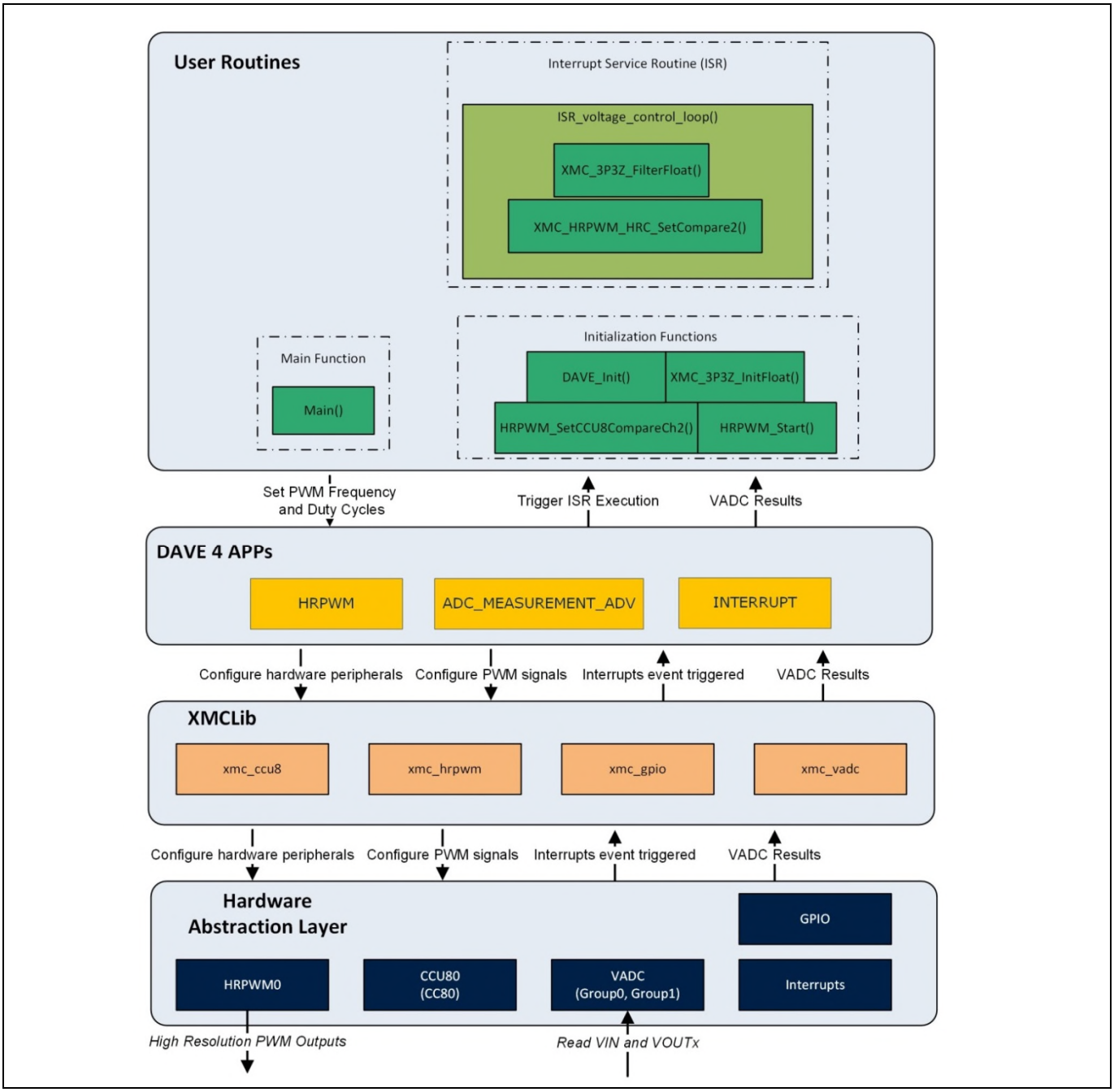

Figure 22 Software overview

4.2.3 3P3Z filter implementation

The voltage control loop is implemented by a classic 3 poles 3 zeros filter using floating point values.

```
__STATIC_INLINE void XMC_3P3Z_FilterFloat(XMC_3P3Z_DATA_FLOAT_t* ptr )
{
  float acc;

  /* Filter calculations */
  acc = ptr->m_B3*ptr->m_E[2]; ptr->m_E[2] = ptr->m_E[1];
  acc += ptr->m_B2*ptr->m_E[1]; ptr->m_E[1] = ptr->m_E[0];
  acc += ptr->m_B1*ptr->m_E[0]; ptr->m_E[0] = (float)(ptr->m_Ref-((uint16_t)*ptr->m_pFeedBack));
  acc += ptr->m_B0*ptr->m_E[0];

  acc += ptr->m_A3*ptr->m_U[2]; ptr->m_U[2] = ptr->m_U[1];
  acc += ptr->m_A2*ptr->m_U[1]; ptr->m_U[1] = ptr->m_U[0];
  acc += ptr->m_A1*ptr->m_U[0];

  /* Max/Min truncation */
  acc = MIN( acc , ptr->m_Max );
  acc = MAX( acc , -ptr->m_Max );
  ptr->m_U[0] = acc;
  if ( acc < ptr->m_Min) acc = ptr->m_Min;

  /*Filter Output*/
  ptr->m_Out = (uint32_t)acc;
}
```

4.2.4 Interrupt service routine implementation

The ISR_voltage_control_loop () routine is used to apply the filter to the ADC measured value, and update the CCU8 and HRPWM compare values.

A 3 pole, 3 zero controller is then run and the output is available in CtrlFloat.m_Out as a 24 bit integer, where the 16 MSB (b23 to b8) are entered into the CCU8 compare value and the 8 LSB (b7 to b0) are intended for the high resolution part. As a result, the output of the filter has to be shifted by 8 to obtain the low resolution part and mask the bottom 8 bits to obtain the high resolution part.
But, since the high resolution is actually 100% = 82, to scale this value the following equation should be used:

$\frac{(m_{Out}\&0xFF)*82}{256}$ (should be divided by 255 but dividing by 256 is faster).

```
void ISR_voltage_control_loop()
{
  /* Applying the filter to the ADC measured value */
  XMC_3P3Z_FilterFloat(&ctrlFloat);

  /* Updating the compare value 1 of the CCU8 with the Low resolution part of the filter output */
  HRPWM_0.ccu8_slice_ptr->CR1S = ctrlFloat.m_Out>>8;

  /* Updating the compare value 2 of the High Resolution Channel with the high resolution part of the
filter output */
  XMC_HRPWM_HRC_SetCompare2(HRPWM_0.hrc_slice_ptr, ((ctrlFloat.m_Out & 0xFF)*(HRPWM_0.hr_cr_max))/256);

  /* Enabling shadow transfer */
  HRPWM_0.ccu8_module_ptr->GCSS |= HRPWM_0.shadow_txfr_msk;
}
```

Execution timing of the interrupt service routine and filter

Table 3 shows the experimental results for execution time of the ISR_voltage_control_loop () where the voltage control loop is executed.

Compiler: ARM-GCC
Optimization level: -O3

Table 3 Execution timing with compiler optimization set to the highest level

Functions	Timing
ISR_voltage_control_loop ()	90 cpu cycles(12.125 us)
3P3Z filter function	50 cpu cycles(625 ns)

4.2.5 Bode plot

Stability of the buck voltage mode control is checked using an OMICRON Bode 100 device. The measured phase margin is about 51 degrees and the gain margin is 8 dB. The results are compared with the theoretical results obtained from the specification. In the example shown in the figure, the specification was created on the WDS tool from Biricha Digital™.

For the setup of the Bode 100 network analyzer, please refer to the OMICRON Bode 100 user manual [6] and the XMC™ Digital Power Explorer user manual [7].

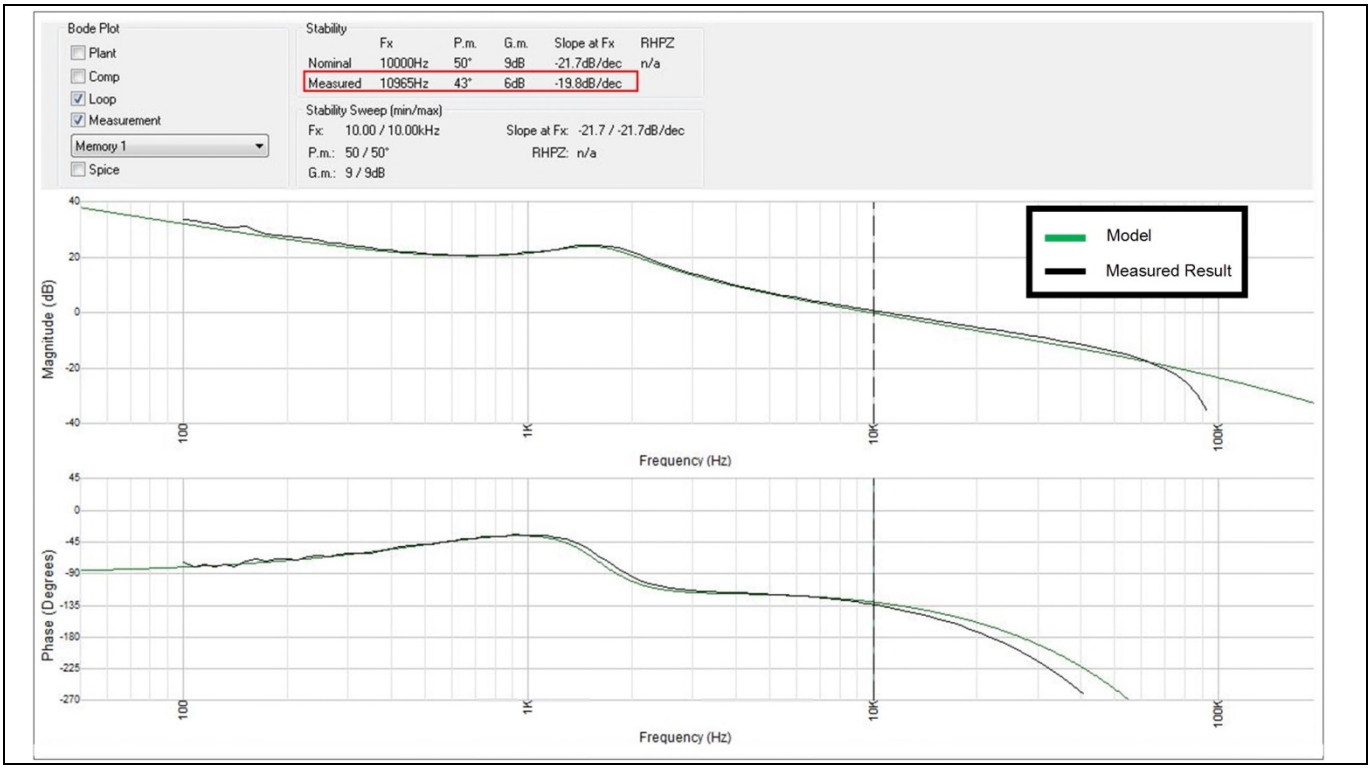

Figure 23 XMC4200 buck voltage mode control Bode plot

[6] OMiCRON Bode 100 User Manual, http://www.omicron-lab.com
[7] XMC Digital Power Explorer User Manual, http://www.infineon.com/xmc_dp_exp

4.2.6 HRPWM versus CCU8 PWM

As stated in chapter 2.1.2, the enhanced PWM resolution is achieved by an insertion that shortens or lengthens the original pulse width of the CCU8 slice output pulse, in steps of 150 psec. By increasing the PWM resolution, the dynamic behavior and control stability of the system is improved considerably. In the Figure 24, the V_{out} ripple and PWM stepping is compared when using HRPWM and only CCU8 PWM.

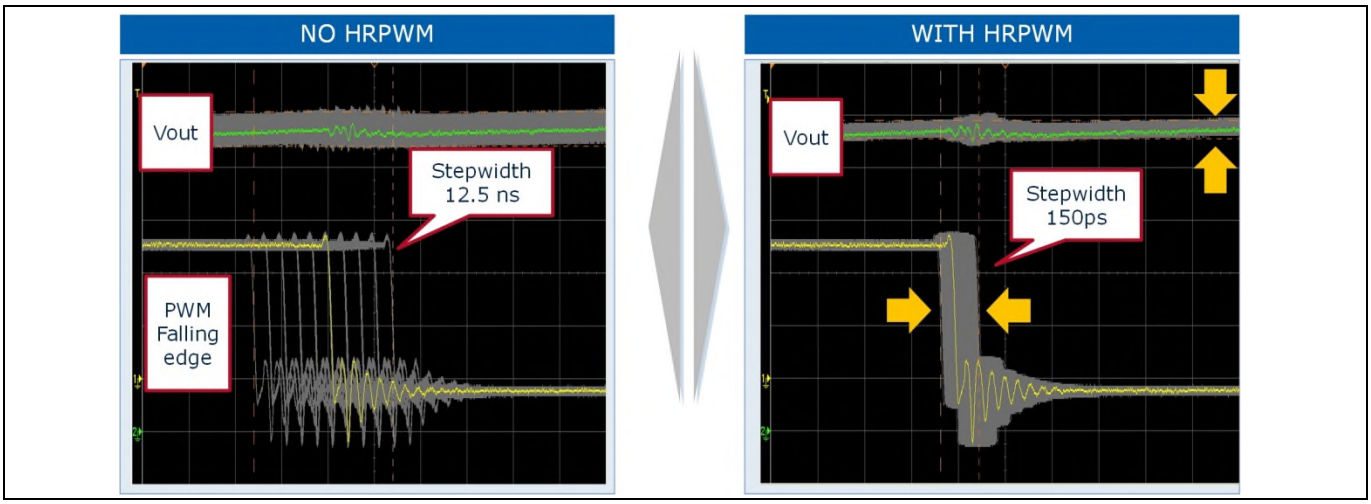

Figure 24 HRPMW vs CCU8 PWM

4.3 XMC1300 VCM implementation example

The boards used are the XMC1300 Digital Power Control Card and XMC™ Digital Power Explorer Board. The output of the buck is driven by the CCU8 PWM signals. The switching frequency is set to 100 kHz.

The controller used is a 3-poles, 3-zeros digital filter. The voltage control loop is executed every cycle of the PWM generation.

The filter coefficients are provided and have been selected to have the following controller characteristics:

- Switching freq = 100 kHz
- Crossover freq = 5 kHz
- Phase margin = 50 degrees
- PWM master clock = 64 MHz
- PWM resolution = 15.625 ns
- ADC resolution = 12 bits

4.3.1 Control specification

The control mode and coefficient selection for the controller have been defined by using the WDS tool from Biricha Digital™. The WDS tool allows the user to easily specify the different characteristics of the power system (topology, controller type, control mode, switching frequency, phase margin, crossover frequency, semiconductors…) in order to obtain the related coefficients and theoretical frequency response. The coefficients can be copied to a DAVE™ project directly from the Infineon tab of the WDS tool.

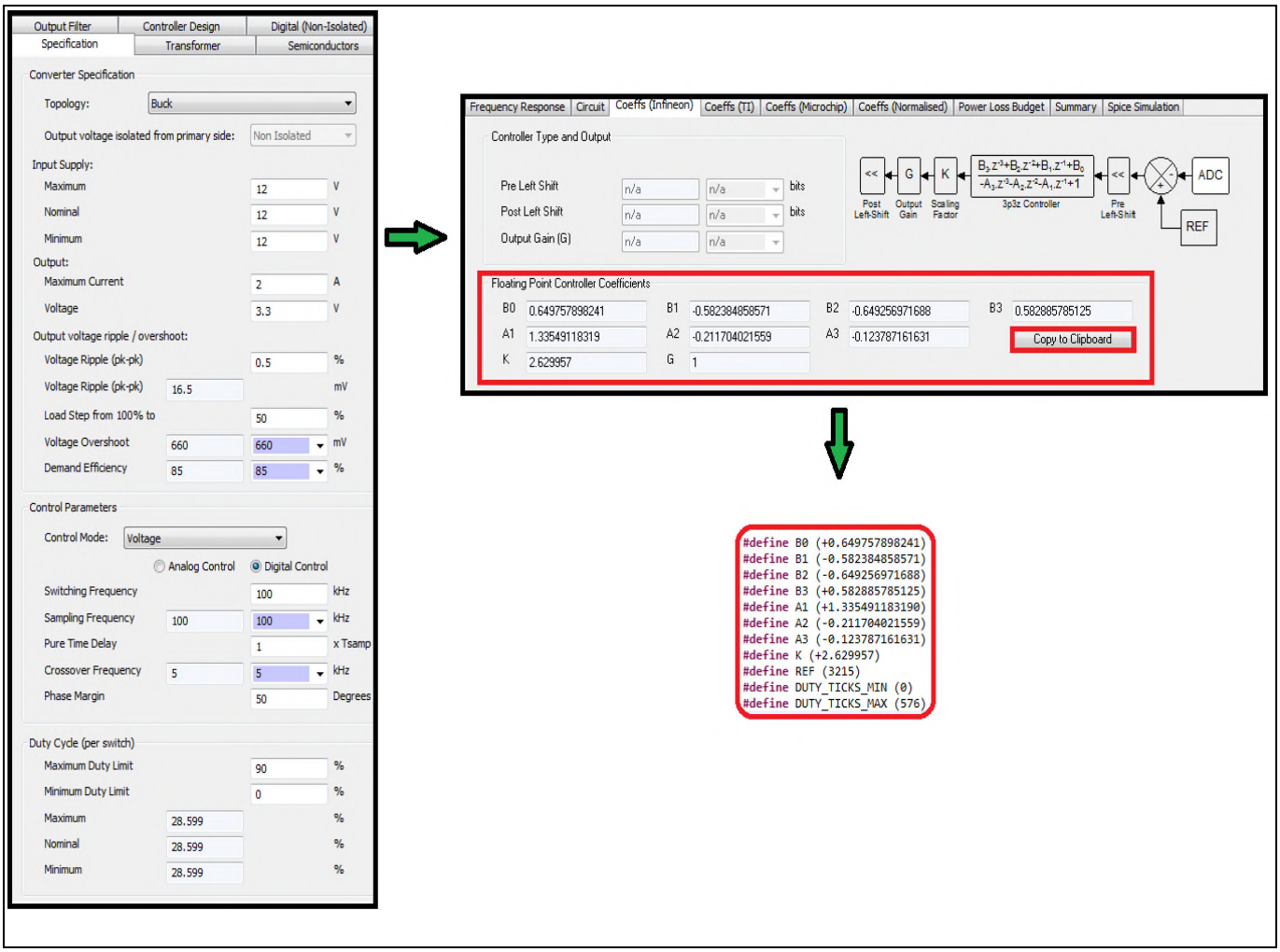

Figure 25 WDS specification and raw floating point coefficients

4.3.2 Software overview

The software project is developed in the DAVE™ development platform. One instance of each of these DAVE™ (Version 4) APPs has been used to ease the peripheral configuration:

- PWM_CCU8 (generates PWM, generates the ADC trigger through the CCU8 peripheral)
- ADC_MEASUREMENT_ADV (output voltage measurement)
- INTERRUPT (NVIC configuration)

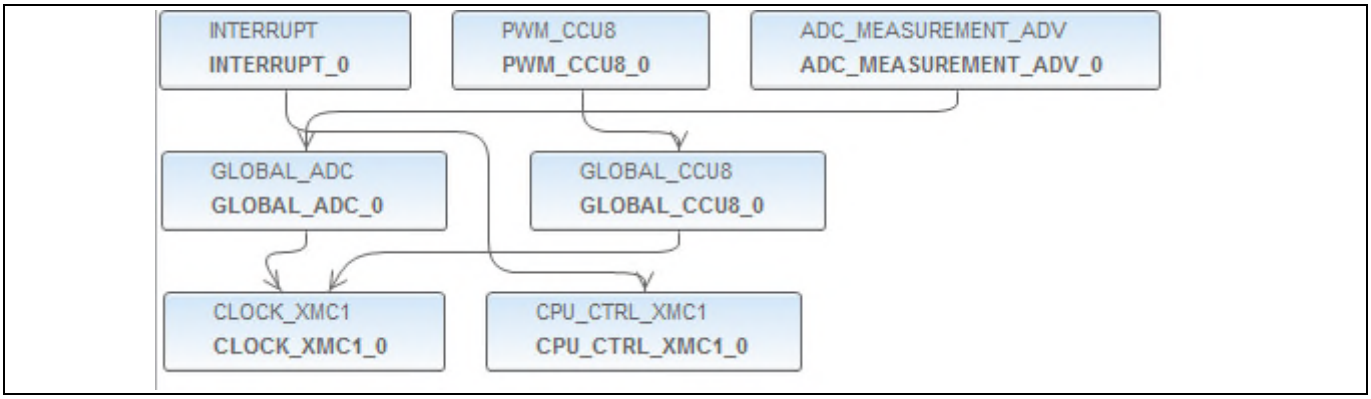

Figure 26 APPs used in the project

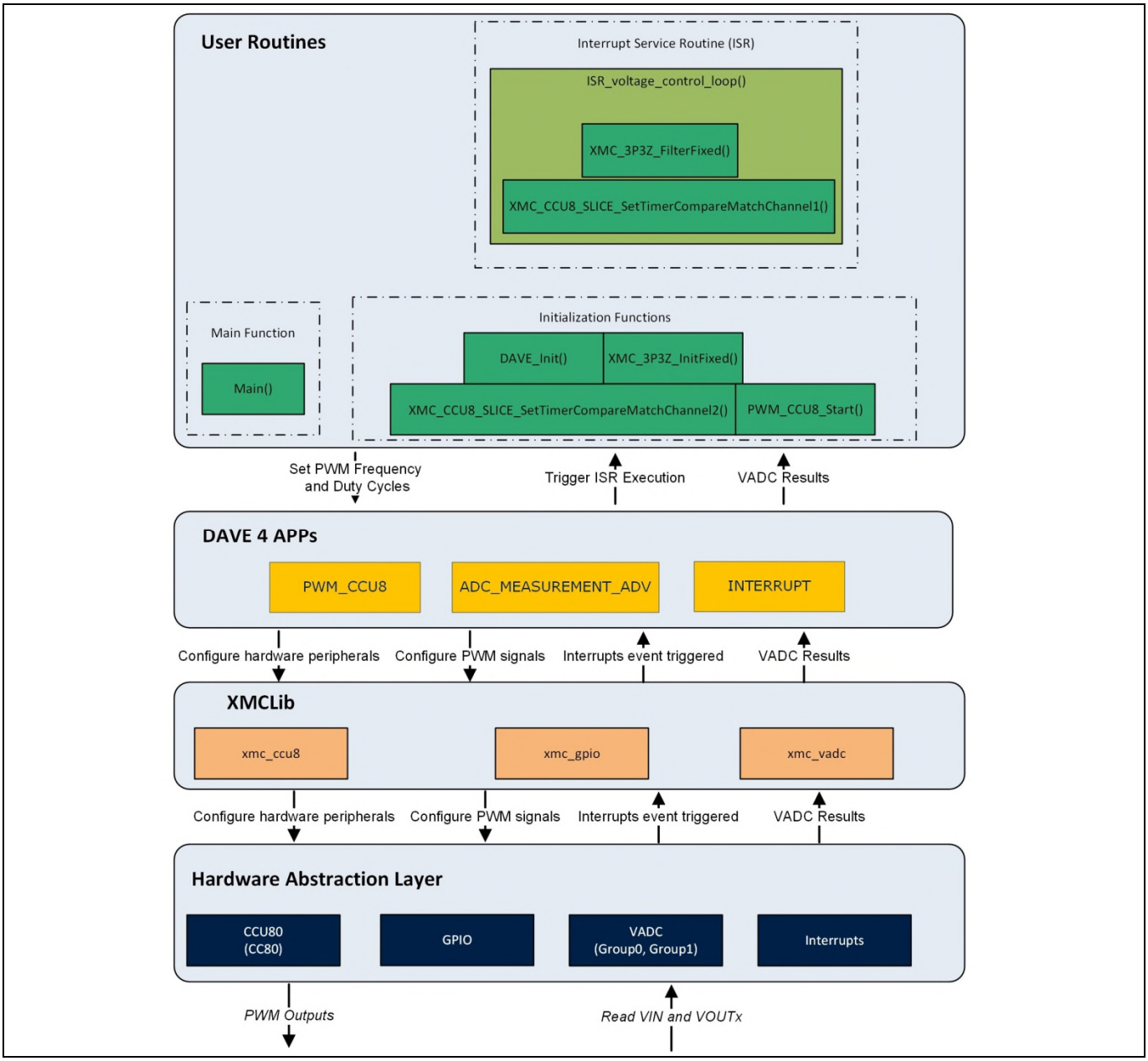

Figure 27 Software overview

4.3.3 3-Pole, 3-Zero filter implementation

The voltage control loop is implemented by a classic 3 poles, 3 zeros filter using fixed points. The fixed point value type for each coefficient is chosen to avoid an overflow. This allows to the filter to ignore any value overflow thus increasing CPU performance.

The formats chosen for the coefficients are:

- **A**: iq-1.19
- **B**: iq1.14
- **U**: iq8.8

```
__STATIC_INLINE void XMC_3P3Z_FilterFixed( XMC_3P3Z_DATA_FIXED_t* ptr )
{
    int32_t acc;
```

```
    // acc (iq9.22) = An (iq-1.19) * Un (iq(8.8)
    acc  = ptr->m_A[3]*ptr->m_U[2]; ptr->m_U[2] = ptr->m_U[1];
    acc += ptr->m_A[2]*ptr->m_U[1]; ptr->m_U[1] = ptr->m_U[0];
    acc += ptr->m_A[1]*ptr->m_U[0];
    acc = acc >> ptr->m_AShift;  //iq is now iq9.19

    // acc (iq12.19) = Bn (iq1.14) * En (iq(12.0)
    acc += ptr->m_B[3]*ptr->m_E[2]; ptr->m_E[2] = ptr->m_E[1];
    acc += ptr->m_B[2]*ptr->m_E[1]; ptr->m_E[1] = ptr->m_E[0];
    acc += ptr->m_B[1]*ptr->m_E[0]; ptr->m_E[0] = ptr->m_Ref-((uint16_t)*ptr->m_pFeedBack);
    acc += ptr->m_B[0]*ptr->m_E[0];

    //our number is now a iq12.19, but we need to store U as a iq8.8
    acc = acc >> ptr->m_BShift; //now it's a iq12.8

    acc = MIN( acc , ptr->m_KpwmMax );
    acc = MAX( acc , ptr->m_KpwmMaxNeg ); //now it's a iq8.8
    ptr->m_U[0] = acc;

    acc = acc >> ptr->m_OShift; //now it's a iq8.0
    if ( acc < ptr->m_KpwmMin) acc = ptr->m_KpwmMin;
    ptr->m_pOut = acc;

}
```

4.3.4 Interrupt service routine implementation

The ISR_voltage_control_loop () routine's function is to apply the filter to the ADC measured value, and update the CCU8 compare value. The voltage controller is a floating point 3 poles, 3 zeros filter.

```
void ISR_voltage_control_loop()
{
  /* Applying the filter to the ADC measured value */
  XMC_3P3Z_FilterFixed(&ctrlFixed);

  /* Updating the compare value 1 of the CCU8 */
  PWM_CCU8_0.ccu8_slice_ptr->CR1S = ctrlFixed.m_pOut;

  /* Enabling shadow transfer */
  PWM_CCU8_0.ccu8_module_ptr->GCSS= 0x1;
}
```

Execution timing of the interrupt service routine and filter

Table 4 shows the experimental results for execution time of the ISR_voltage_control_loop () where the voltage control loop is executed.

Compiler: ARM-GCC

Optimization level: -O3

Table 4 Execution timing with compiler optimization set to the highest level

Functions	Timing
ISR_voltage_control_loop ()	144 cpu cycles (4.5 us)
3P3Z filter function	113 cpu cycles (3.531 us)

4.3.5 Bode plot

Stability of the buck voltage mode control is checked by using an OMICRON Bode 100. The measured phase margin is approximately 58 degrees and the gain margin is 9 dB. The results are compared with the theoretical results obtained from the specification. In the example in Figure 28, the specification was created on the WDS tool from Biricha Digital™. For the setup of the Bode 100 network analyzer, please refer to the OMICRON Bode 100 user manual [8] and the XMC™ Digital Power Explorer user manual [9].

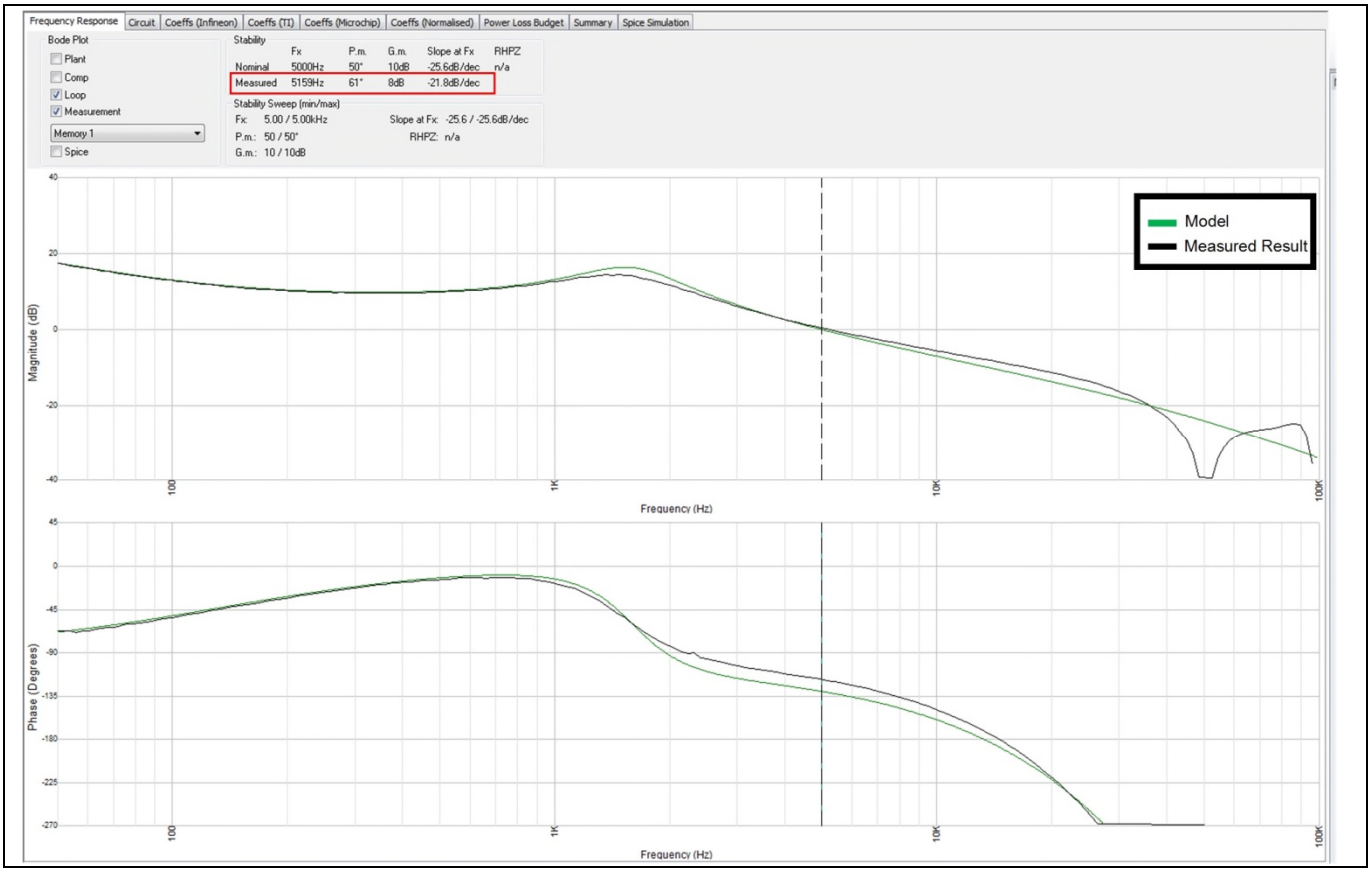

Figure 28 XMC1300 buck voltage mode control Bode plot

[8] OMiCRON Bode 100 User Manual, http://www.omicron-lab.com
[9] XMC Digital Power Explorer User Manual, http://www.infineon.com/xmc_dp_exp

5 Buck converter peak current control (PCC) with XMC™

During peak current control, the steady state transfer function is maintained by two essential control loops:

- A fast inherent loop that reacts to limit current detection on a cycle-by-cycle basis
- A slow coherent loop that reflects the output versus reference deviation and adjusts the limit current

The cycle-by-cycle current loop provides a good response for fast load transients. However, this becomes unstable with a duty cycle of more than 50%. To avoid this, slope compensation is added to maintain an average current waveform and avoid the instability. The XMC™ device contains the necessary peripherals to accomplish this mode with the minimum CPU or external hardware requirements.

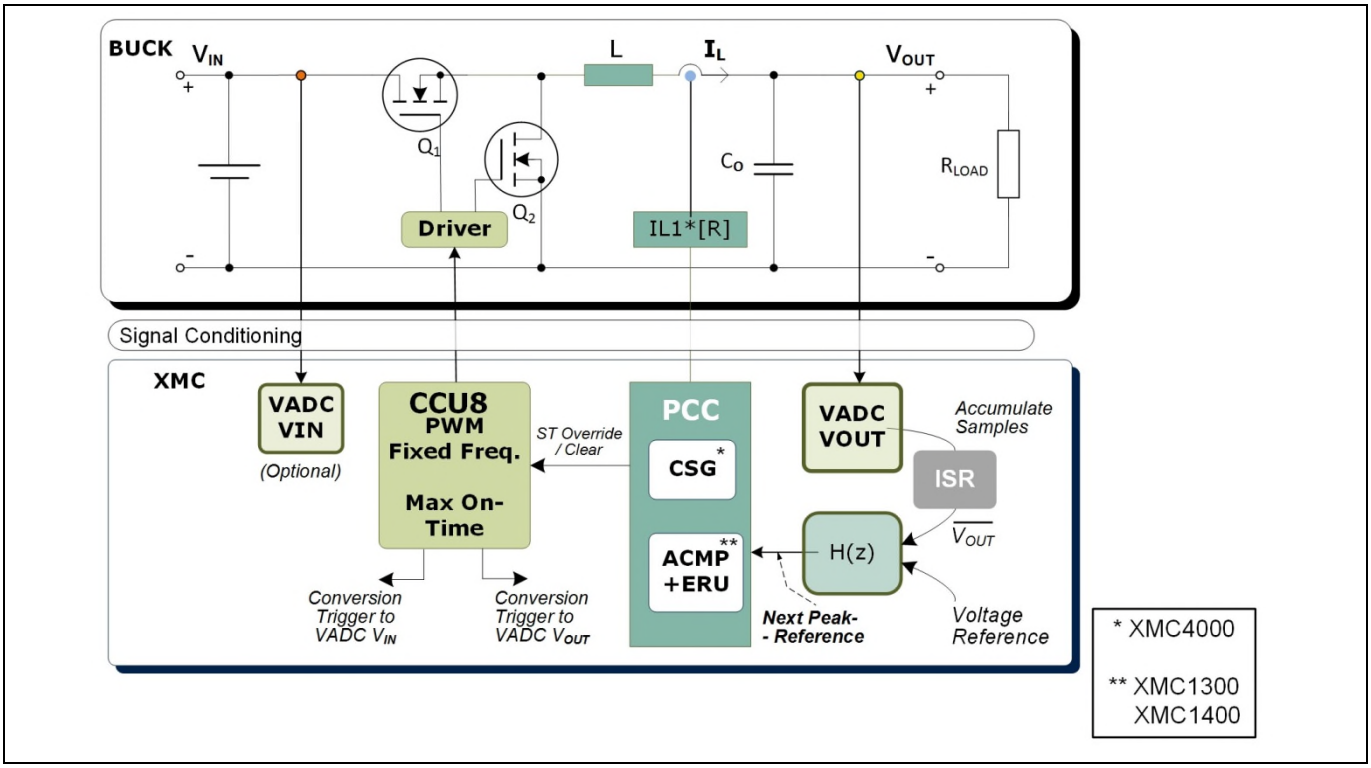

Figure 29 Peak current control maximum on-time, fixed frequency

Timing scheme

During the on-time of the PWM, the inductor current rises. Once this current reaches the peak current reference level, the PWM on-time period is terminated by a set. The output voltage is sampled periodically. Any difference to the reference voltage is compensated for and supplied as the peak current reference.

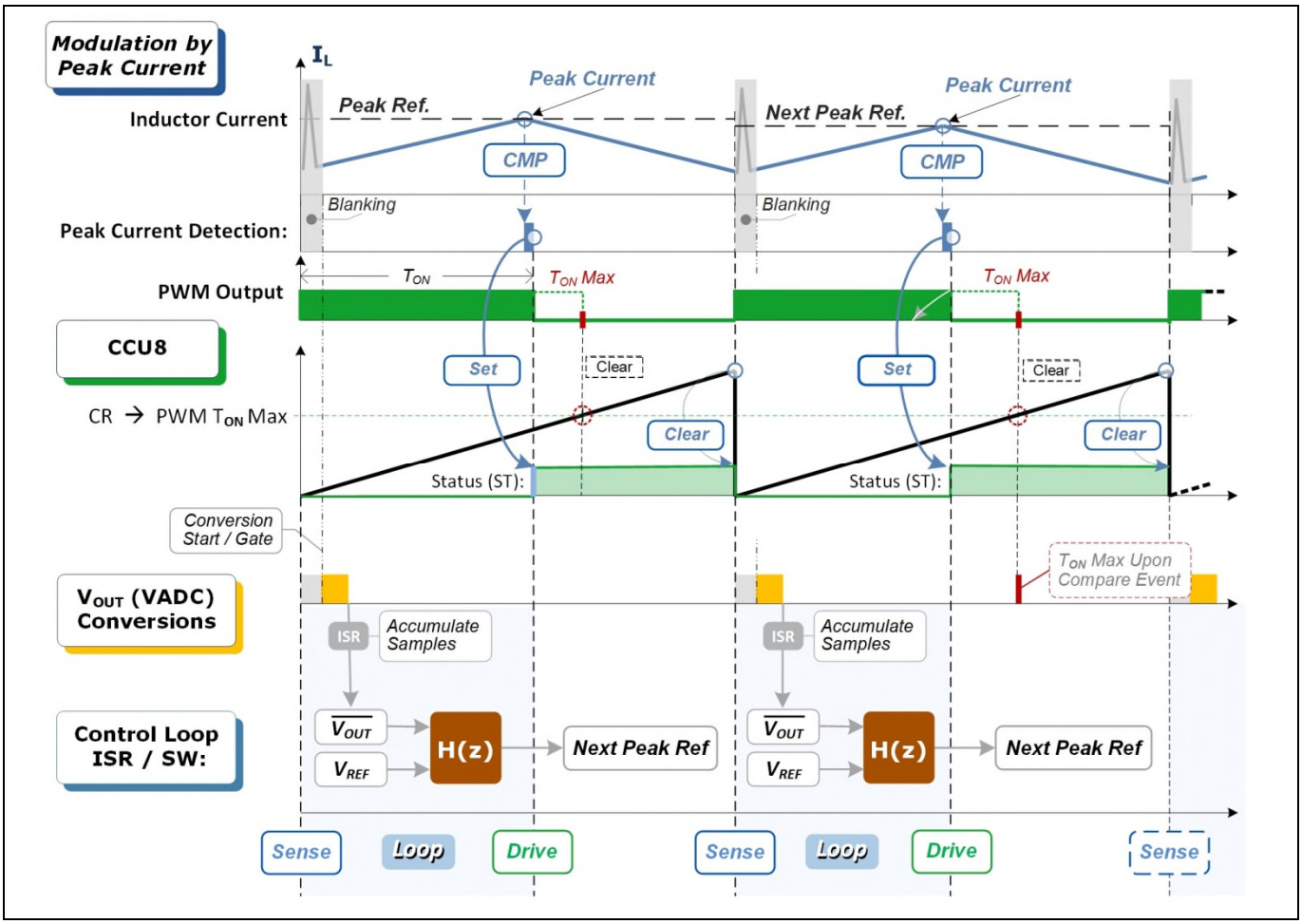

Figure 30 Peak current control timing scheme

5.1 Compensator design (2P2Z)

The objective of the compensator in the system is to add the required mechanism for helping the system output to track a desired reference input - even in the presence of noise, modeling error or disturbances. A Type-2 (2 poles, 2 zeros) filter is one of the most common types of feedback controllers used in peak current controlled buck converters. The poles and zeros of the compensation networks should be placed according to the analysis of the control-to-output transfer function. See Figure 31 and Chapters 5.2.1 and 5.3.1

Type 2 filters have 2 poles and 1 zero implementing the following transfer function (H(s)):

$$H_c(s) = \frac{\omega_{p0}}{s} \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right)}$$

For converting the poles and zeros into the digital domain, the continuous time (s-domain) needs to be converted to the discrete z-domain by using:

$$s = \left(\frac{2}{T}\right) \frac{z-1}{z+1}$$

Having:

$$H_c(z) = \frac{B_2 Z^{-2} + B_1 Z^{-1} + B_0}{-A_2 Z^{-2} - A_1 Z^{-1} + 1}$$

Which, in a linear difference equation:

$$y[n] = b0x[n] + b1x[n-1] + b2x[n-2] + a1y[n-1] + a2y[n-2]$$

Where x[n] = reference – feedback

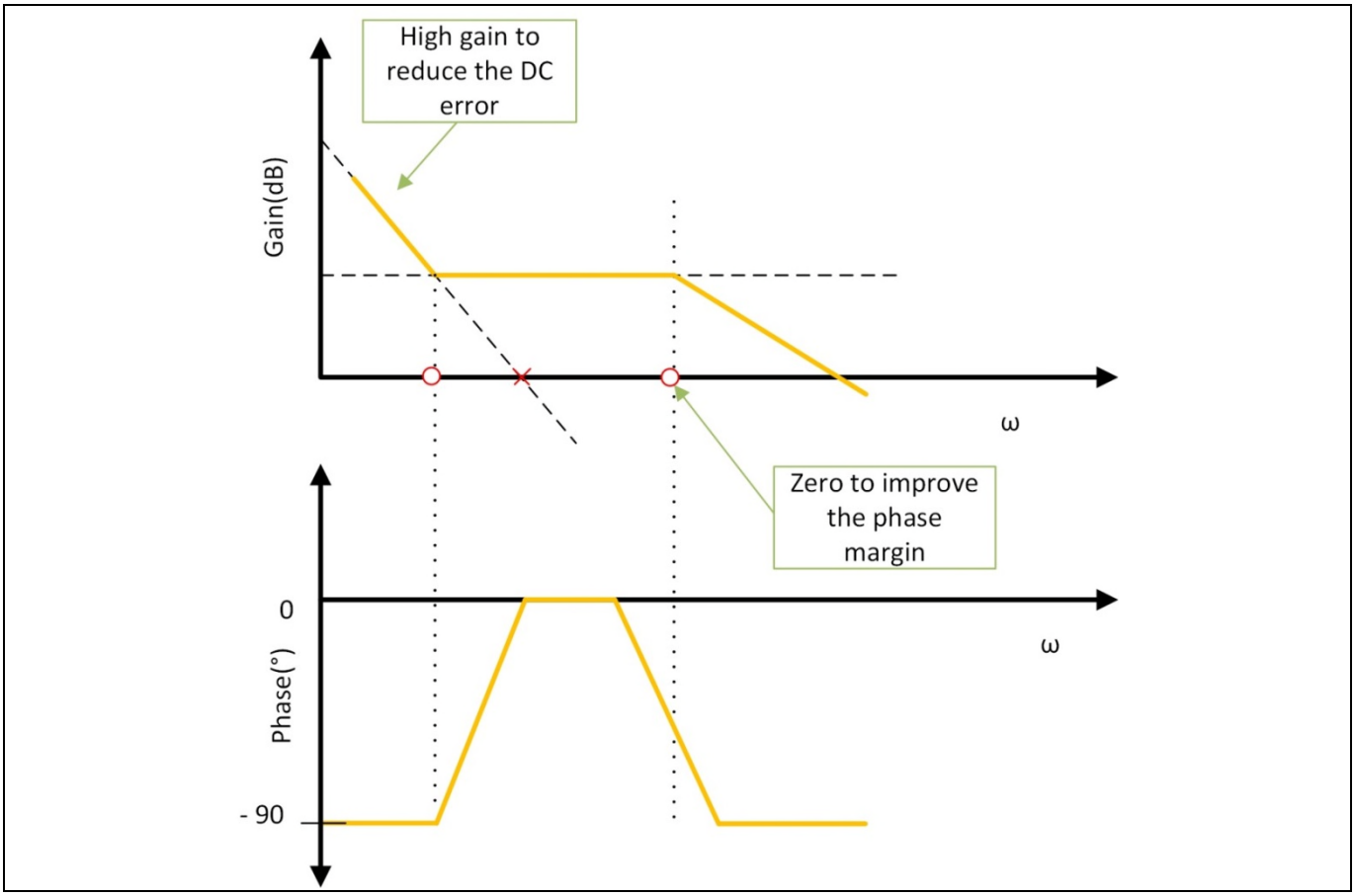

Figure 31 Designing type 2 compensator (Bode plot)

5.2 XMC4200 PCC implementation example

Using XMC4200 devices, with integrated comparator, slope generator, and blanking functionality, the fast peak current control loop can be realized cost effectively.

- Bill of material (BOM) cost is reduced with integrated comparator and slope generator.
- No DMA / data transfer is required for slope generation unlike a typical system. This means that the MCU resources can be used for critical tasks instead of performing data transfer.

The filter coefficients provided have been selected to have the following controller characteristics:

- Switching freq = 200 kHz
- Crossover freq = 10 kHz
- Phase margin = 50 degrees
- PWM master clock = 80 MHz
- ADC resolution = 12 bits

The hardware boards used are the XMC4200 Digital Power Control Card and the XMC™ Digital Power Explorer Board. The voltage loop controller used is a 2 poles, 2 zeros filter. The control loop is executed every cycle of the PWM generation.

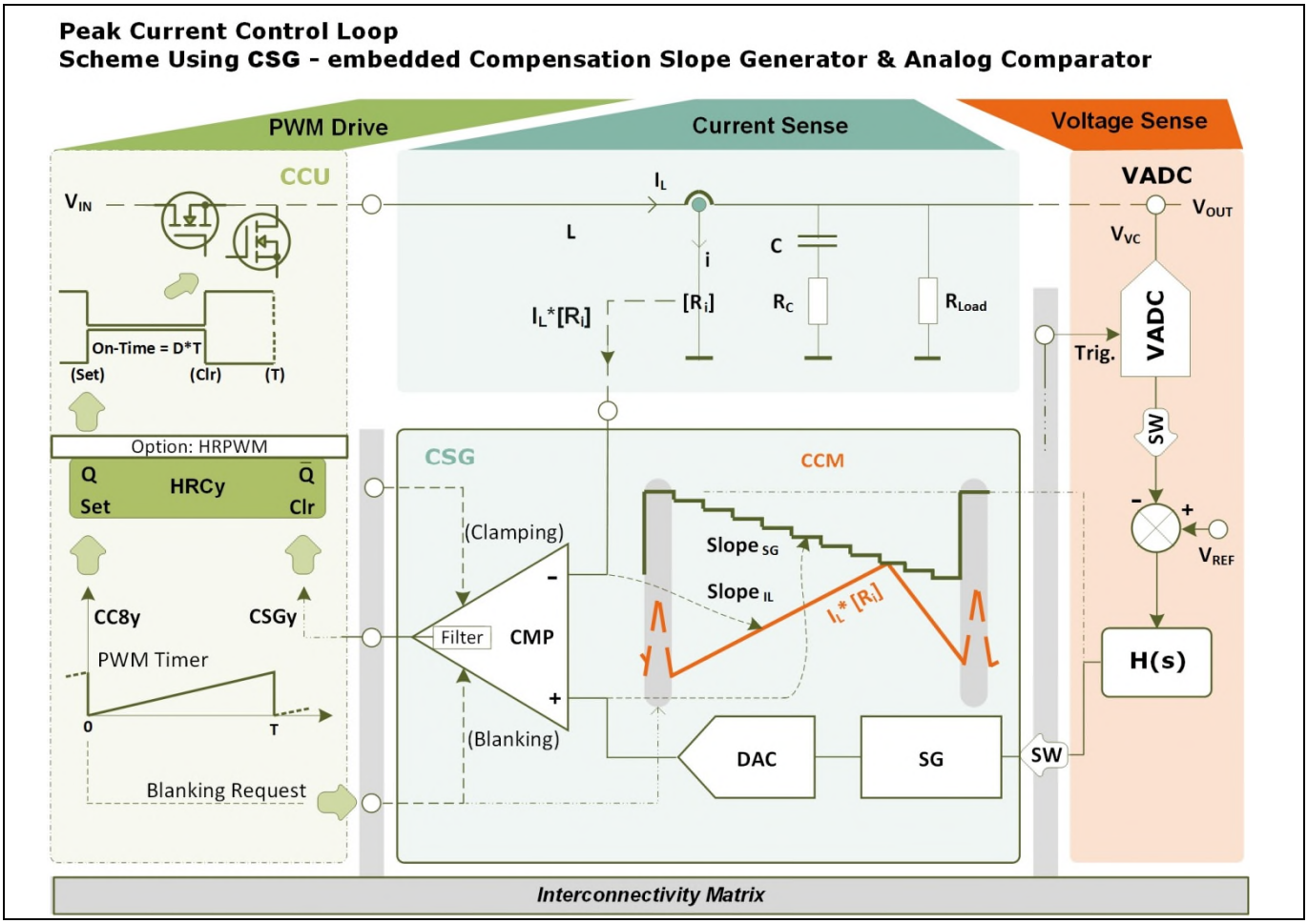

Figure 32 Peak current control with CSG

5.2.1 Control specification

The control mode and coefficient selection for the controller have been defined using the WDS tool from Biricha Digital™. The WDS tool allows the user to easily specify the different characteristics of the power system (topology, controller type, control mode, switching frequency, phase margin, crossover frequency, semiconductors…) in order to obtain the related coefficients and theoretical frequency response. The coefficients can be copied to a DAVE™ project directly from the Infineon tab of WDS tool.

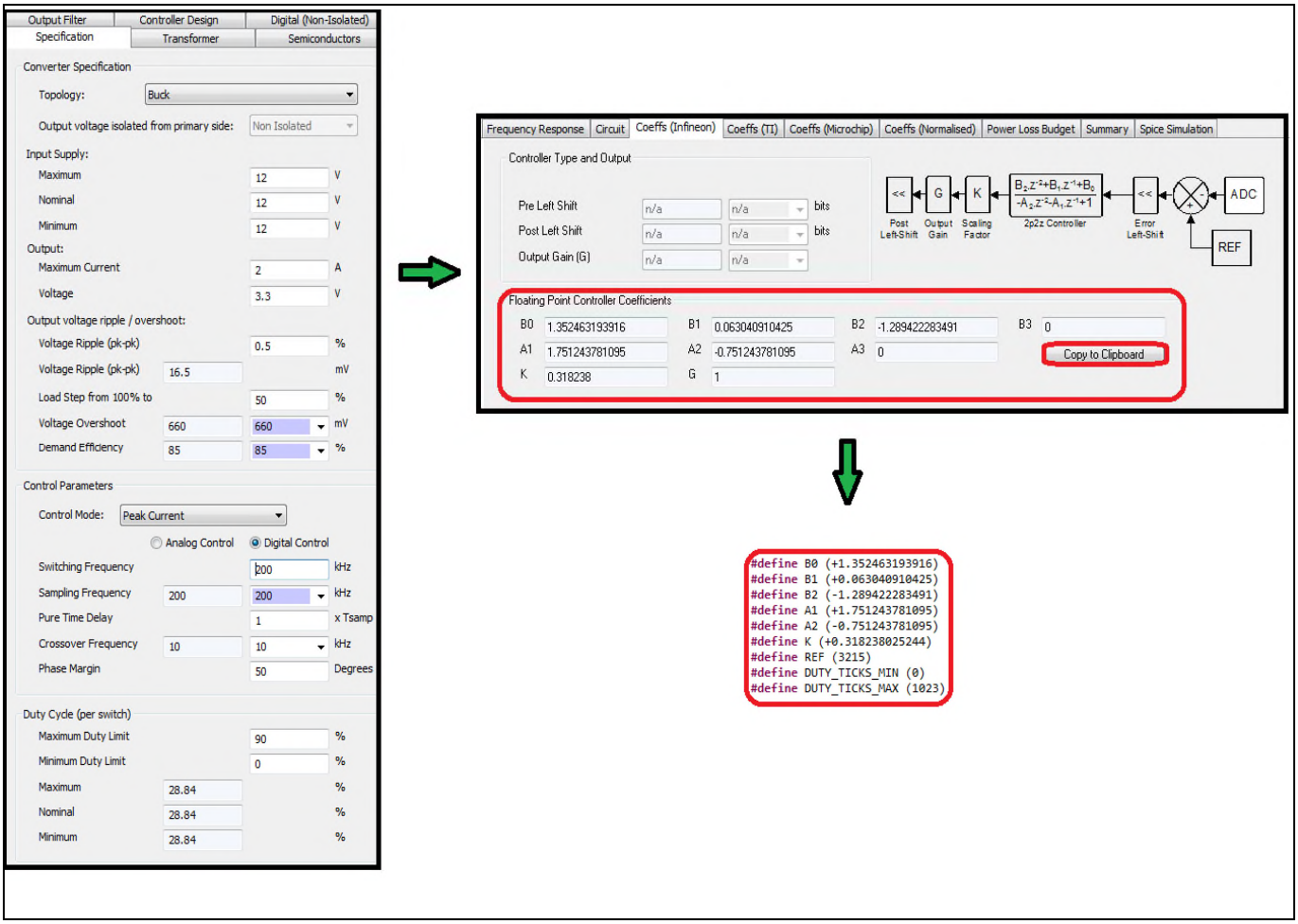

Figure 33 WDS specification and raw floating point coefficients

5.2.2 Software overview

Similar to the XMC4200 voltage control project, the project is developed in the DAVE™ development platform. One instance of each of these DAVE™ (Version 4) APPs have been used to ease the peripheral configuration:

- HRPWM (High resolution PWM, generates the ADC trigger through the CCU8 peripheral and the HRPWM)
- ADC_MEASUREMENT_ADV (output voltage measurement)
- COMP_SLOPE_GEN (comparator and slope generator)
- INTERRUPT (NVIC configuration)

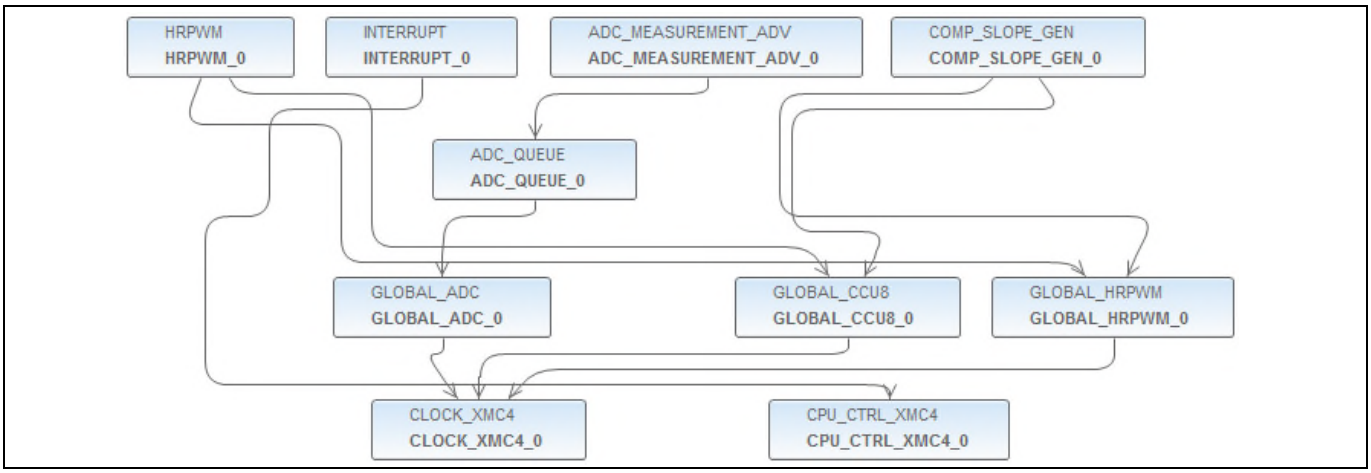

Figure 34 APPs used in the project

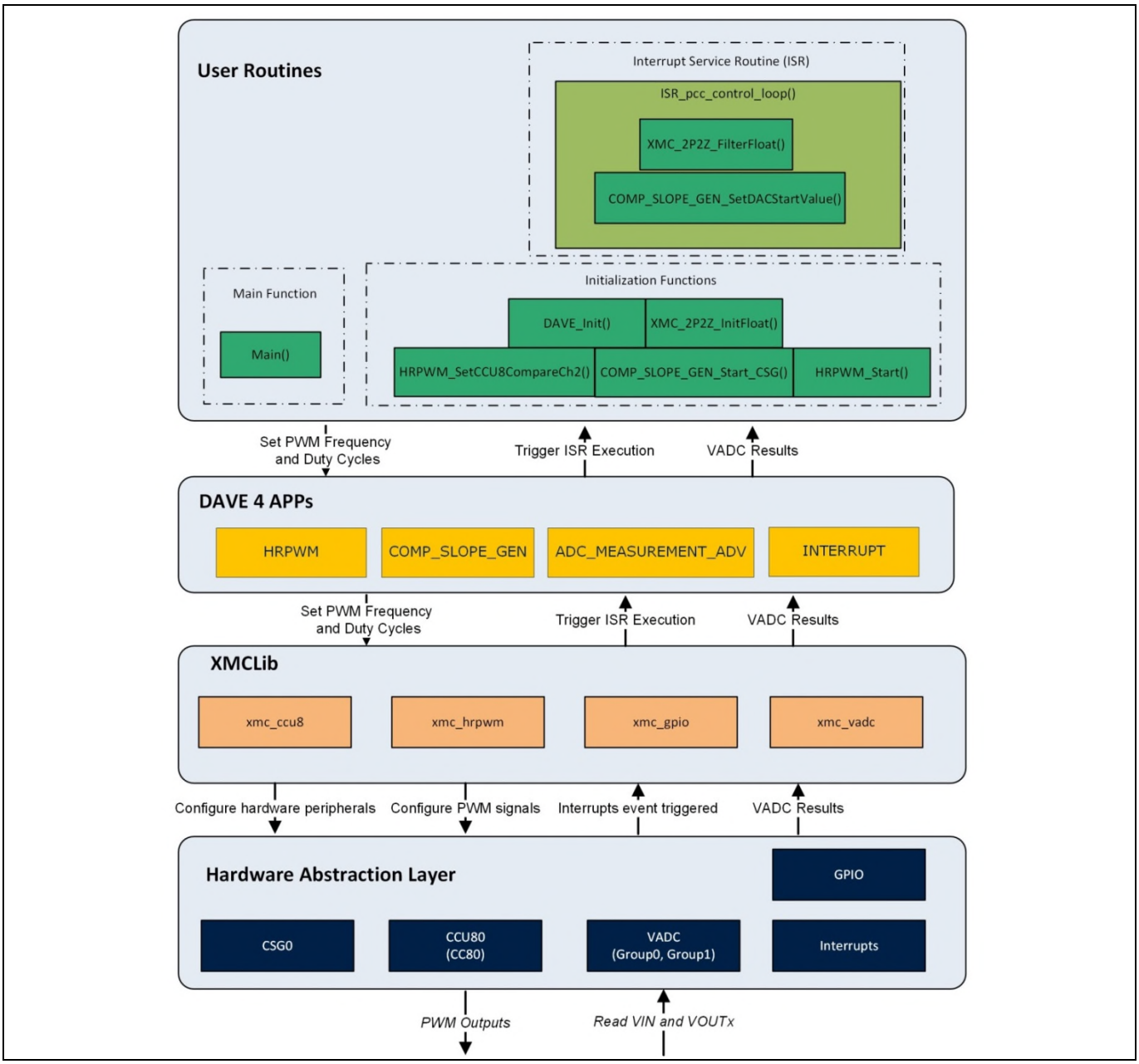

Figure 35 Software overview

5.2.3 2P2Z filter implementation

The voltage control loop is implemented by a classic 2 poles, 2 zeros filter using floating point values.

```
__STATIC_INLINE void XMC_2P2Z_FilterFloat(XMC_2P2Z_DATA_FLOAT_t* ptr )
{
  float acc;

  /* Filter calculations */
  acc = ptr->m_B2*ptr->m_E[1]; ptr->m_E[1] = ptr->m_E[0];
  acc += ptr->m_B1*ptr->m_E[0]; ptr->m_E[0] = (float)(ptr->m_Ref-((uint16_t)*ptr->m_pFeedBack));
  acc += ptr->m_B0*ptr->m_E[0];

  acc += ptr->m_A2*ptr->m_U[1]; ptr->m_U[1] = ptr->m_U[0];
  acc += ptr->m_A1*ptr->m_U[0];

  /* Max/Min truncation */
  acc = MIN( acc , ptr->m_Max );
  acc = MAX( acc , ptr->m_NegMax );
  ptr->m_U[0] = acc;
  if ( acc < ptr->m_Min) acc = ptr->m_Min;

  /*Filter Output*/
  ptr->m_Out = (uint32_t)acc;
}
```

5.2.4 Interrupt service routine implementation

The ISR_pcc_control_loop () routine is used to apply the filter to the ADC measured value, and update the DAC start value for the slope compensation generation.

```
void ISR_pcc_control_loop()
{

 /* Applying the filter to the ADC measured value */
  XMC_2P2Z_FilterFloat(&ctrlFloat);

 /* Set new DAC start value- ramp is automatically generated */
  COMP_SLOPE_GEN_SetDACStartValue(&COMP_SLOPE_GEN_0,ctrlFloat.m_Out);

}
```

Execution timing of the interrupt service routine and filter

Table 5 shows the experimental results of execution time for the ISR_pcc_control_loop () where the voltage control loop is executed.

Compiler: ARM-GCC

Optimization level: -O3

Table 5 Execution timing with compiler optimization set to the highest level

Functions	Timing
ISR_pcc_control_loop ()	75 cpu cycles (937 ns)
2P2Z filter function	41 cpu cycles(512.5 ns)

5.2.5 Bode plot

Stability of the buck peak current control is checked using the OMICRON Bode 100. Measured phase margin is approximately 56 degrees and the gain margin is 7 dB. The results are compared with the theoretical results obtained from the specification. In the example in Figure 36, the specification was created on WDS tool from Biricha Digital™.

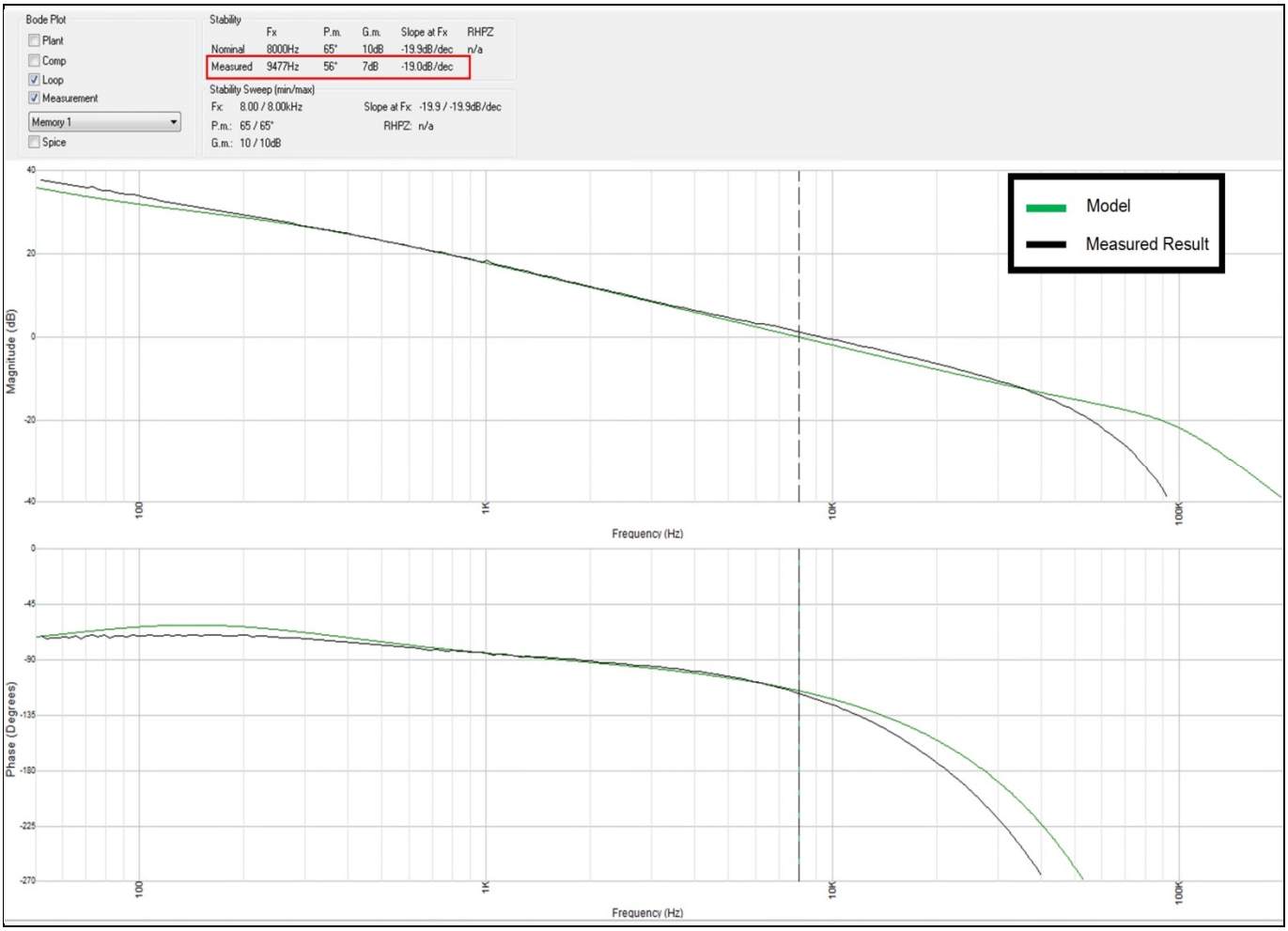

Figure 36 XMC4200 buck peak current control Bode plot

5.3 XMC1300 PCC implementation example

For mid to low end solutions, peak current control modulation can be implemented with the XMC1300 device. It has internal ACMP which, together with the external slope compensator, means that peak current detection can be realized. The external slope generation, blanking control and reference for ACMP is performed interactively with the CCU4 slices.

Boards used for this project are the XMC1300 Digital Power Control Card and XMC™ Digital Power Explorer Board.

The buck is driven by the PWM signals using CCU8. The switching frequency is set to 100 kHz.

The controller used is a type 2 filter. In this example the jumper needs to be in the XMC1000 position to enable the slope compensation circuitry - see Figure 38.

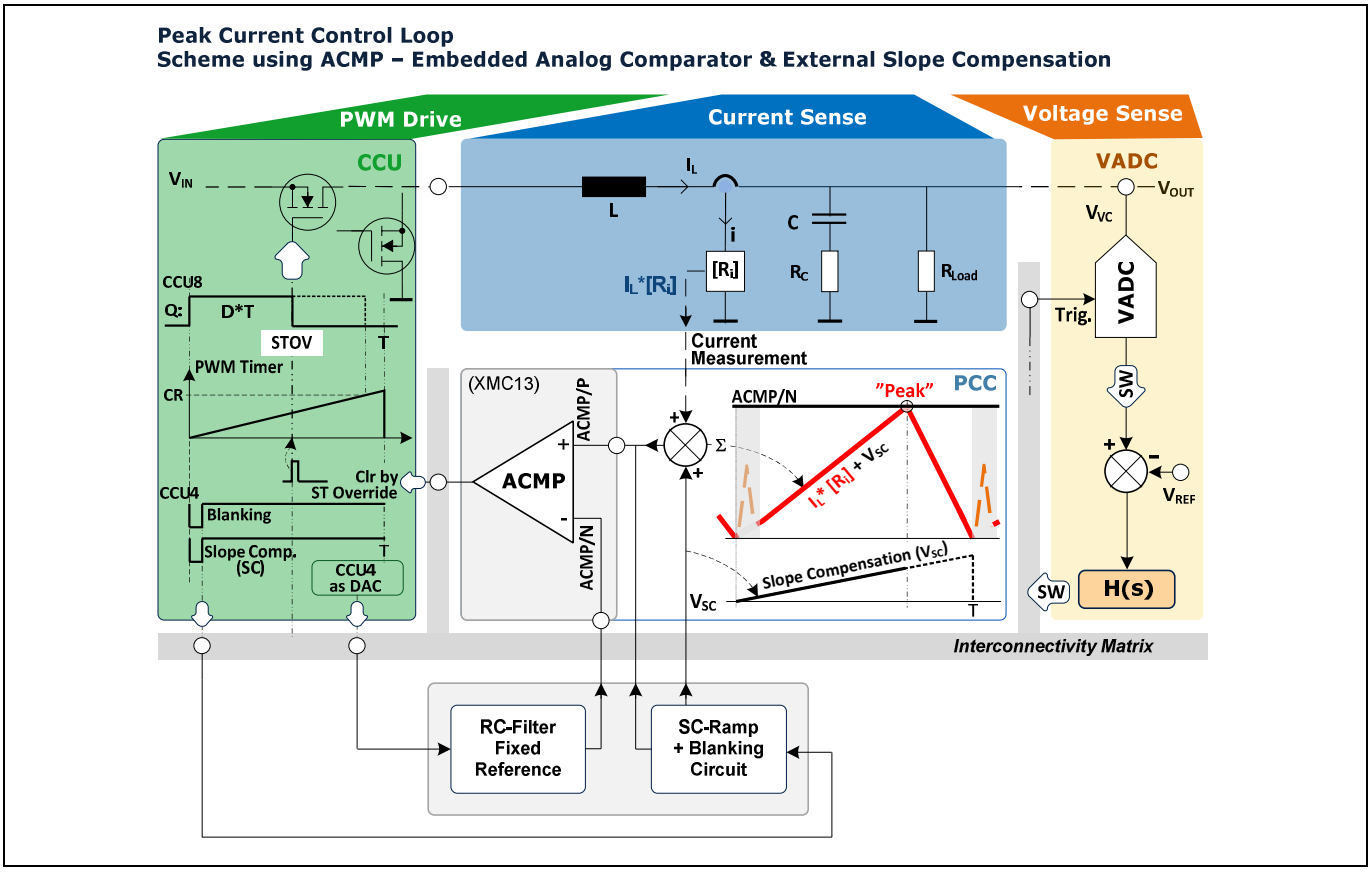

Figure 37 Peak current control with ACMP

Slope generation can be performed by adding a ramp (V_{SC}) to the inductor current measurement signal (I_L *R_i). By using a simple RC and diode network together with the CCU8 PWM output, external linear control of a slope compensation voltage ramp is accomplished, please refer to Figure 38.

When the PWM signal is high, the capacitor voltage (V_{SC}) is ramped up. The ramp voltage is added to the ACMP input (BUCK0_ISENSE) and so invokes slope compensation. A CCU4 timer is used to generate the blanking signal (BUCK0_PWM_BLANKING). This timer works synchronously with the CCU8 timer and rejects switching noise by forcing the analog comparator (ACMP) input to ground.

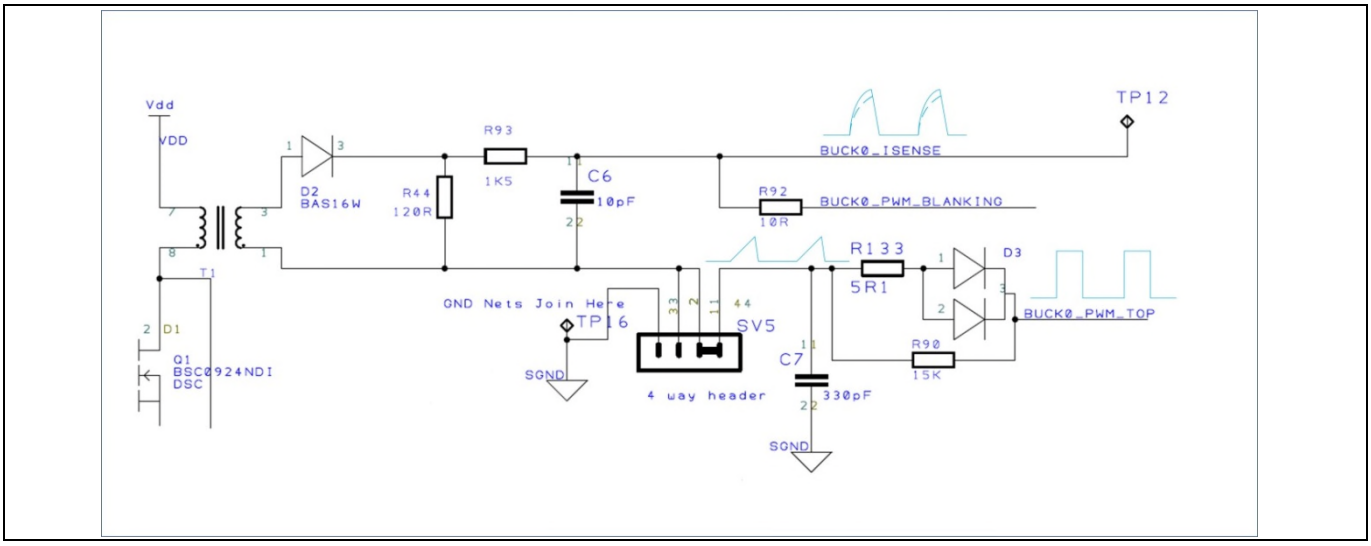

Figure 38 ACMP peak current control – slope compensation circuitry

Figure 39 Current sense waveforms with / without external slope compensation

The provided RC filter components can be replaced by the user in order to achieve the desired results. The values for R and C need to be chosen by reaching a compromise between desired bandwidth and permitted ripple of the output voltage signal.

5.3.1 Control specification

The control mode and coefficient selection for the controller have been defined by using the WDS tool from Biricha Digital™. The WDS tool allows the user to easily specify the different characteristics of the power system

(topology, controller type, control mode, switching frequency, phase margin, crossover frequency, semiconductors…) in order to obtain the related coefficients and theoretical frequency response. The coefficients can be copied to a DAVE™ project directly from the Infineon tab of WDS tool.

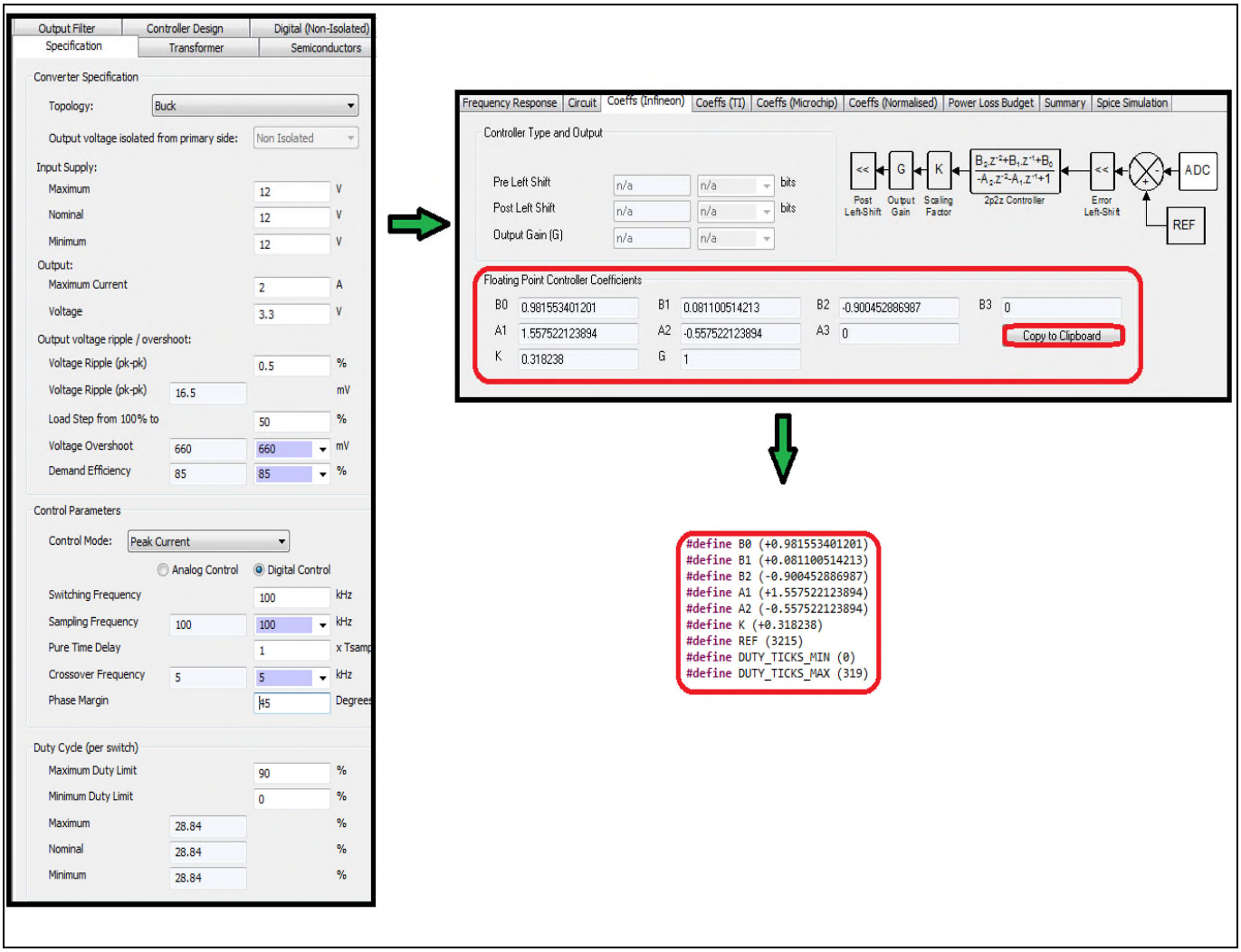

Figure 40 WDS specification and raw floating point coefficients

5.3.2 Software overview

As in the XMC4200 peak current control implementation, the CCU8 timer is used for PWM generation and VADC is used to measure the input and the output voltages.

Connection of the analog comparator output to the CCU8 override status input in the XMC1300 device can be achieved through the ERU (Event Request Unit).

The project is developed in the DAVE™ development platform.

One instance of each of these DAVE™ (Version 4) APPs has been used to ease the peripheral configuration:

- PWM_CCU4 (generates PWM, generates the ADC trigger through the CCU8 peripheral)
- ADC_MEASUREMENT_ADV (output voltage measurement)

- COMP_REF (comparator and DAC emulation for the slope generation(CCU4))
- INTERRUPT (NVIC configuration)

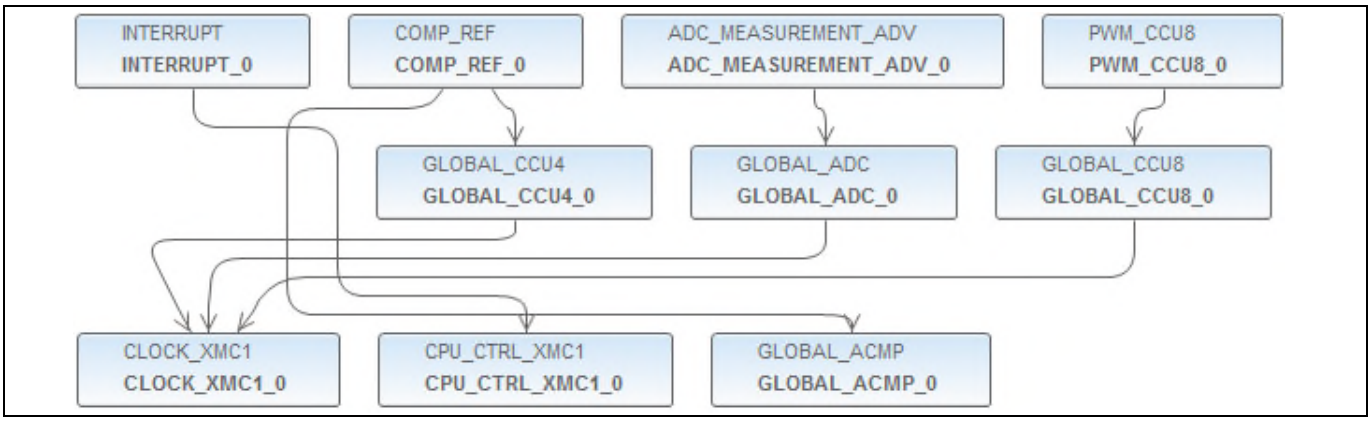

Figure 41 APPs used in the project

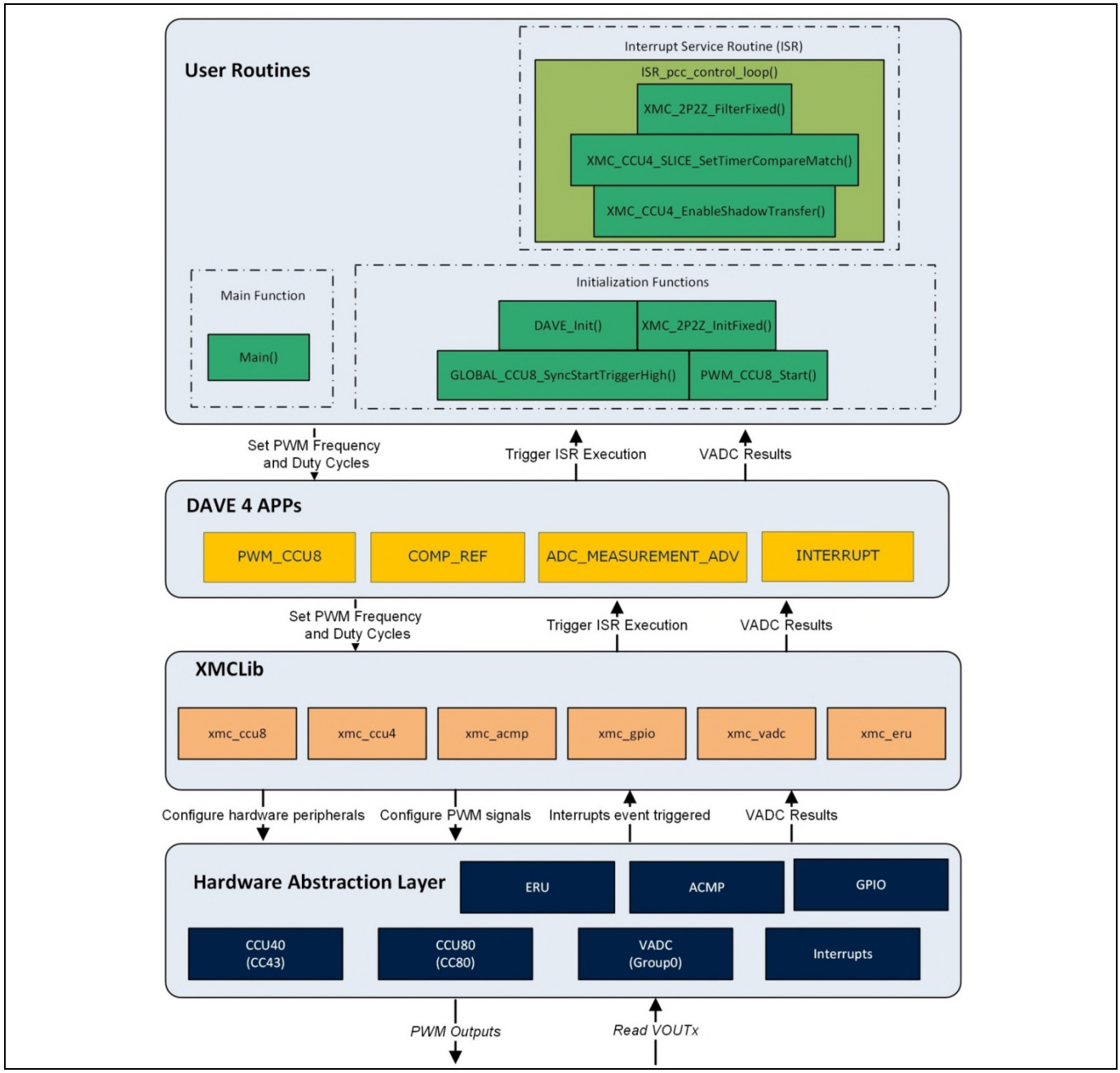

Figure 42 Software overview

5.3.3 2P2Z filter implementation

The current control loop is implemented by a classic 2 poles, 2 zeros filter using fixed point values.

These are the formats chosen for the coefficients:

- **A**: iq 1.16
- **B**: iq-1.20
- **U**: iq9.5

```
__STATIC_INLINE void XMC_2P2Z_FilterFixed(XMC_2P2Z_DATA_FLOAT_t* ptr )
{
    int32_t acc;

    acc = ptr->m_A[2]*ptr->m_U[1]; ptr->m_U[1] = ptr->m_U[0];
```

```
    acc += ptr->m_A[1]*ptr->m_U[0];
    acc = acc >> ptr->m_AShift;
    acc += ptr->m_B[2]*ptr->m_E[1]; ptr->m_E[1] = ptr->m_E[0];
    acc += ptr->m_B[1]*ptr->m_E[0]; ptr->m_E[0] = ptr->m_Ref-((uint16_t)*ptr->m_pFeedBack);
    acc += ptr->m_B[0]*ptr->m_E[0];
    acc = acc >> ptr->m_BShift;
    acc = MIN( acc , ptr->m_KpwmMax );
    acc = MAX( acc , ptr->m_KpwmMaxNeg );
    ptr->m_U[0] = acc;
    acc = acc >> ptr->m_OShift;
    if ( acc < ptr->m_KpwmMin) acc = ptr->m_KpwmMin;
    ptr->m_pOut = acc;
}
```

5.3.4 Interrupt service routine implementation

The ISR_pcc_control_loop () routine is used to apply the filter to the ADC measured value, and update the CCU4 compare value, which in this case, is emulating the DAC operation for the slope compensation as shown in Figure 37.

```
void ISR_pcc_control_loop()
{
  /* Applying the filter to the ADC measured value */
  XMC_2P2Z_FilterFixed(&ctrlFixed);

  /* Set compare value for CC4 phase 0 */
  XMC_CCU4_SLICE_SetTimerCompareMatch(COMP_REF_0.ccu4_config->cc4_slice_ptr, (COMP_REF_0.ccu4_config-
>period_value - (uint16_t) ctrlFixed.m_pOut));

  /* Transfer phase 0 compare value from shadow register to actual register */
  XMC_CCU4_EnableShadowTransfer(COMP_REF_0.ccu4_config->ccu4_module_ptr, COMP_REF_0.ccu4_config-
>shadow_txfr_msk);

}
```

Execution timing of the interrupt service routine and filter

Table 6 shows the experimental results of execution time for the ISR_pcc_control_loop () where the voltage control loop is executed.

Compiler: ARM-GCC

Optimization level: - O3

Table 6 Execution timing with compiler optimization set to the highest level

Functions	Timing
ISR_pcc_control_loop ()	136 cpu cycles (4.25 us)
2P2Z filter function	106 cpu cycles (3.312 us)

5.3.5 Bode plot

The stability of the buck peak current control is checked using the OMICRON Bode 100. The measured phase margin is about 48 degrees and the gain margin is 6 dB. The results are compared with the theoretical results obtained from the specification. In the example in Figure 43, the specification was created on the WDS tool from Biricha Digital™.

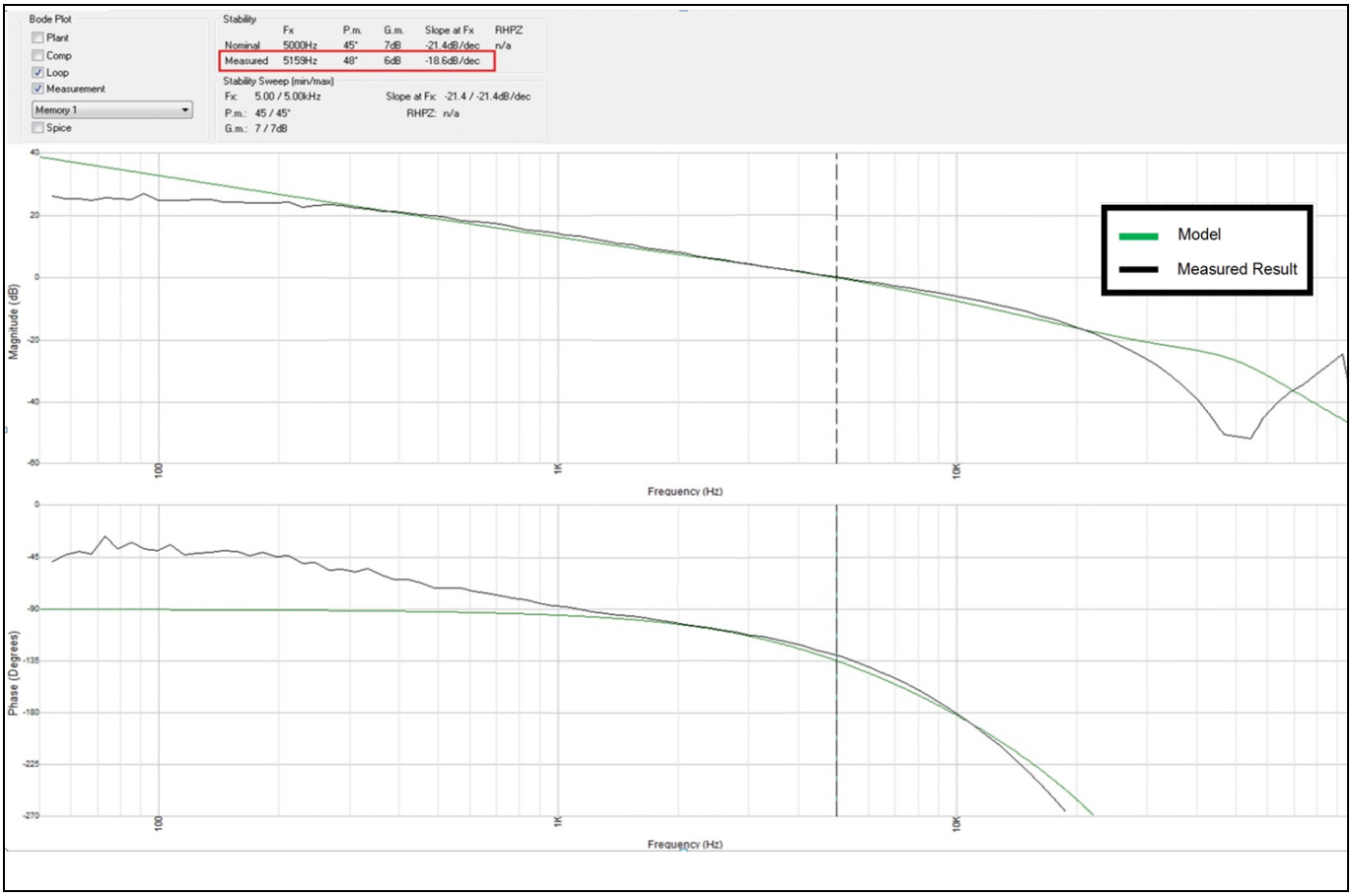

Figure 43 XMC1300 buck peak current control Bode plot

Revision history
Major changes since the last revision

Page or reference	Description of change
2016-05-20	First version

Edition 2016-06-20

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AP32319

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