A/D Converter Supply and PCB Design Guideline

AP32297

AURIX™

TriCore™ 32-bit

Application Note

About this Document

Scope and purpose

This document describes details about PCB design and filter components at A/D converter supply pins. Some architectural differences between the Infineon AUDO™ and AURIX™ family of products require special care when connecting the A/D converter module to the PCB.

The AUDO™ Family is a single core architecture with CPU frequencies up to 180MHz and has a ground concept with separated ground pins for digital and analog modules. The AURIX™ 32 bit microcontrollers have a multi core architecture with up to 300MHz CPU frequency with an integrated cross bar for providing this high performance.

To get more signal pins for AURIX™ 32 bit microcontrollers and because of noise implications, there is only one common internal ground for digital and analog modules. This common ground is realized with an EPad for QFP packages and with a center Vss ball block for BGA packages. Because of the high performance AURIX™ microcontrollers draw a high core supply current. The resulting high ground current in combination with the common GND concept can increase GND noise compared to the AUDO™ Family. Therefore AURIX™ 32 bit microcontrollers require special care in respect to the analog supply and ground concept to get a good noise performance from the A/D converter. When using DC/DC converters for analog supply voltage this also has to be considered for filter components at analog supply and input voltages.

The resolution of a high performance A/D converter is smaller than 1 mV. Care must be taken in the system setup otherwise system noise is measured instead of small signal levels.

The document is split into the following sections:

- Analog Supply Voltage Filter Calculation (V_{DDM})
- Reference Supply Voltage Filter Calculation (V_{AREF})
- Analog Input Filter Calculation (ANx)
- PCB and Design Guidelines

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1 Analog Supply Voltage Filter Calculation (V_{DDM})

The analog supply domain is separated from the main EVR supply domain and can be supplied by separate external regulators or trackers. A mixed supply scheme is possible with a 5 V A/D converter domain (V_{DDM} = V_{AREFx} = 5 V) and the remaining system running on 3.3 V supply (V_{EXT} = V_{DDP3} = 3.3 V).

When sourcing the analog supply voltage V_{DDM} from a DC/DC converter, special care has to be taken to the analog supply filter. In this case the analog supply filter cutoff frequency has to be below the DC/DC converter switching frequency to suppress switching noise. A maximum noise amplitude of about 20 mV is allowed to met the specified A/D converter error values.

1.1 How to calculate an analog Supply Voltage Filter at V_{DDM}?

A low pass RC filter is recommended for the analog supply voltage V_{DDM} as shown in **Figure 1**. When supplying V_{DDM} from a DC/DC converter a RC filter is essential to prevent high noise at the A/D converter results.

Steps for filter calculation

- Determine maximum analog supply rms current I_{DDM} for every single V_{DDM} pin.
  Depending on device type more V_{DDM} pins are provided.
- Check reference voltage maximum specification in the Data Sheet.
  A typical value is: V_{AREF_max} = V_{DDM} + 50 mV.
  This allows a maximum voltage drop at the filter resistor R_{DDM} of V_{RDDM_max} = 50 mV.
- Switching frequency $f_{DC/DC}$ of a DC/DC converter has to be suppressed.
  The cutoff frequency of the RC filter has to be below the DC/DC converter switching frequency.
- Calculate R_{DDM_MAX} value and select appropriate resistor value from E24 table.
- Calculate C_{DDM_MIN} value and select appropriate capacitor value from E24 table.

Note: Select filter component tolerances to the application demands.
Typical Electronic Industries Alliance (EIA) tolerances are:
E12: 10% tolerance, E24: 5% tolerance, E48: 2% tolerance, E96: 1% tolerance

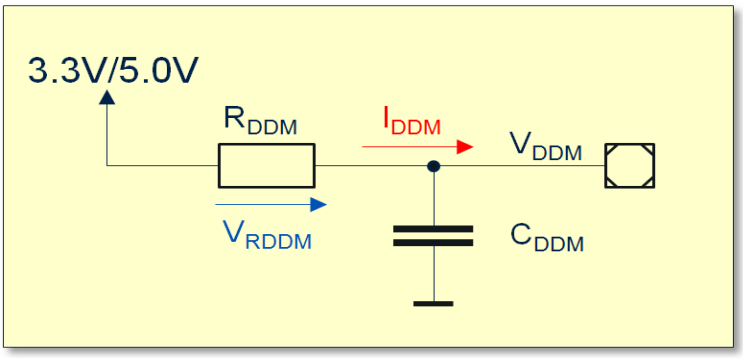

Figure 1 Block Diagram of the Analog Supply RC Filter at V_{DDM}

1.2 Calculation Example

The assumed values for this example are:

V_{AREF}	= 5 V	I_{DDM_max}	= 39 mA	VADC modules	: 4
V_{AREF_max}	= V_{DDM} + 50 mV	I_{REF_DSADC}	= 5.5 µA	DSADC-twin-modulators	: 2
V_{RDDM_max}	= 50 mV	$Error_{AREF}$	= LSB_r / 2	conversion rate	: 1 MHz
V_{RAREF}	= LSB_{12} / 2	E	= 1	resolution r	= 12 bit
Q_{CONV_max}	= 20 pC (with precharge)	$f_{DC/DC}$	= 480 kHz	C_{AREFSW}	= 30 pF
Q_{CONV_max}	= 40 pC (no precharge)	resistor	from E24 table	C_{AINSW_max}	= 7 pF

The value for the external filter resistor is:

R_{DDM_max} = V_{DDM_max} / I_{DDM_max}
R_{DDM_max} = 50 mV / 39 mA = 1.28 Ω
R_{DDM} = 1.2 Ω (value from E24 table)

The value for the external filter capacitor is:

$f_{DC/DC}$ = 1 / (2 * π * R_{DDM} * C_{DDM})
C_{DDM_min} = 1 / (2 * π * R_{DDM} * $f_{DC/DC}$)
C_{DDM_min} = 1 / (2 * π * 1.2 Ω * 480 kHz) = 276 nF
C_{DDM} = 330 nF (value from E24 table) f_{CUTOFF} = 402 kHz

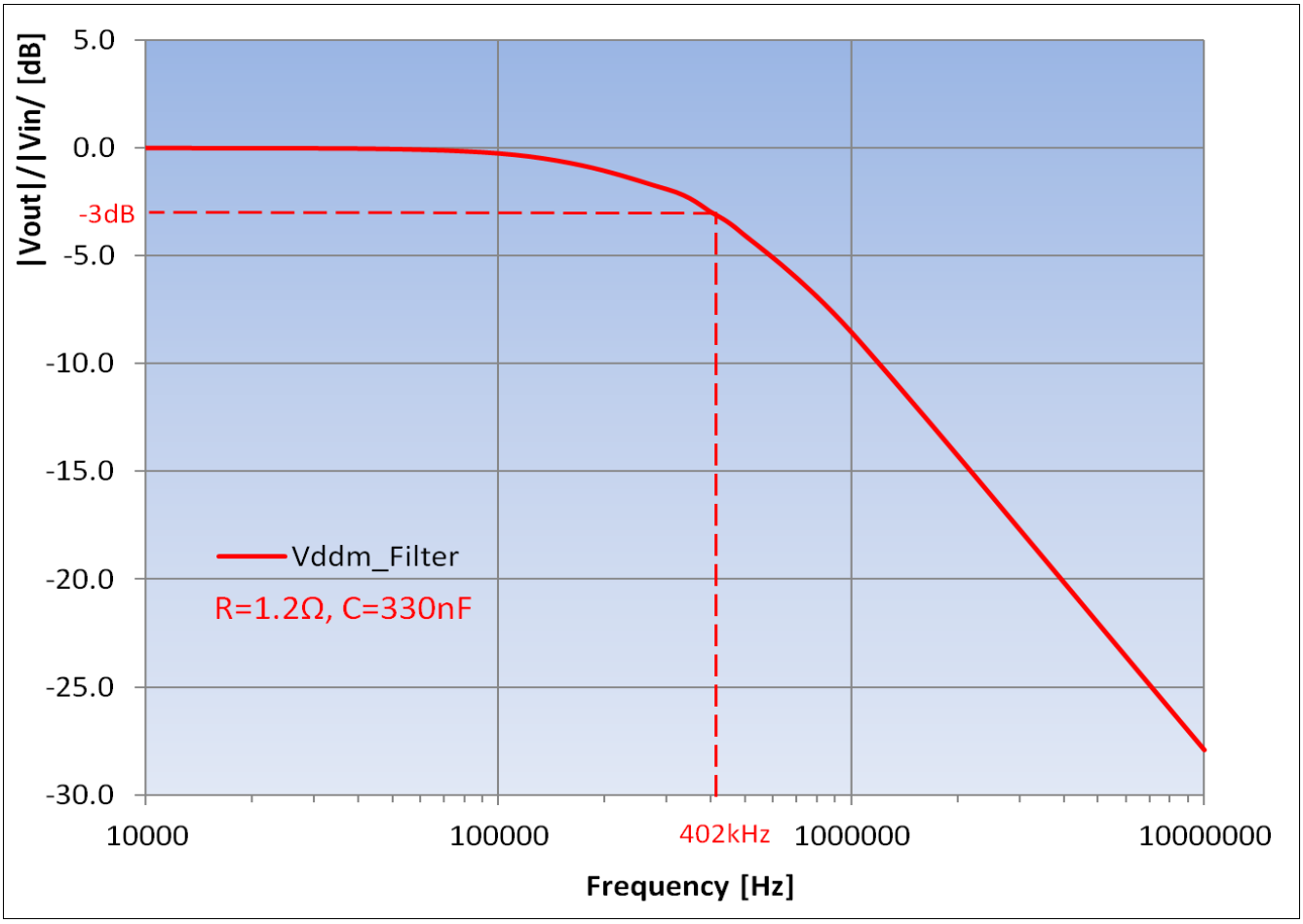

Figure 2 Analog Supply Voltage V_{DDM} RC Filter Curve with R_{DDM} = 6.8 Ω and C_{DDM} = 2.2 µF

2 Reference Supply Voltage Filter Calculation (V_{AREF})

The reference voltage input V_{AREF} is switched to parts of the internal switched capacitor field C_{AREFSW} while the charge redistribution phase of a conversion is performed. A stable and noise-free reference voltage is required to get accurate conversion results. The A/D converter result is more sensitive to noise on V_{AREF} than to noise on V_{DDM} because of the direct V_{AREF} influence to the conversion result via the internal capacitor field. Details of the required filter are shown in **Figure 3**.

Requirements to the reference supply voltage for filter calculation

- Provide maximum required rms current at V_{AREF}
- Provide charge demand for internal switching capacitors
- Suppress DC/DC converter switching noise $f_{DC/DC}$
- Suppress general system noise and/or white noise

2.1 How to calculate an analog Reference Supply Voltage Filter at V_{AREF}?

Steps for filter calculation

- Calculate R_{AREF_max}
  - Determine maximum reference rms current I_{AREF} for every single V_{AREF} pin. Depending on device type more V_{AREF} pins are available
  - Calculate reference current per VADC for a fixed conversion rate via specified charge per conversion Q_{CONV}
  - Determine maximum reference supply current I_{AREF} for every single V_{AREF} pin via number of connected VADC and DSADC modules
  - Define maximum allowed voltage error at R_{AREF} with the assumption: $V_{RAREF} = LSB_{12} / 2$
  - Calculate maximum value for resistor R_{AREF} and select appropriate resistor value from E24 table
- Calculate C_{AREF_min}
  - Calculate precharge factor (precharge feature enabled)
  - Define maximum allowed charging error C_{AREFSW}
- Calculate filter cutoff frequency
  - Check whether calculated values of R_{AREF} and C_{AREF} do suppress DC/DC converter switching noise frequency $f_{DC/CD}$
- Adapt C_{AREF} to suppress system noise
  - Using the maximum accuracy of a 12 bit A/D converter requires not only filtering DC/DC converter switching noise but also white noise and deterministic noise from the system at pin V_{AREF}

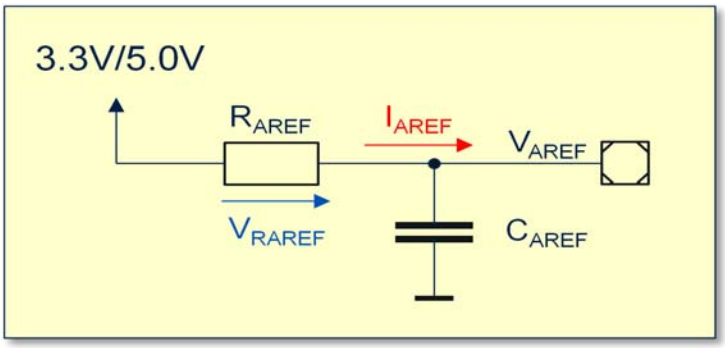

Figure 3 Block Diagram of the Analog Reference Supply RC Filter at V_{AREF}

2.2 Calculation Example

The assumed values for this example:

V_{AREF}	= 5 V	I_{DDM_max}	= 39 mA	VADC modules	: 4
V_{AREF_max}	= V_{DDM} + 50 mV	I_{REF_DSADC}	= 5.5 µA	DSADC-twin-modulators	: 2
V_{RDDM_max}	= 50 mV	$Error_{AREF}$	= LSB_r / 2	conversion rate	: 1 MHz
V_{RAREF}	= LSB_{12} / 2	E	= 1	resolution r	= 12 bit
Q_{CONV_max}	= 20 pC (with precharge)	$f_{DC/DC}$	= 480 kHz	C_{AREFSW}	= 30 pF
Q_{CONV_max}	= 40 pC (no precharge)	resistor	from E24 table	C_{AINSW_max}	= 7 pF

2.2.1 Calculate R_{AREF_max}

The maximum VADC reference current using the precharge feature is:

I_{AREF_max}	= Q_{CONV_max} * conversion-rate	(per VADC)
I_{AREF_max}	= 20 pC * 1 MHz = 20 µA	
$I_{AREF\_max\_sum}$	= 20 µA * 4	(all VADCs)
$I_{AREF\_max\_sum}$	= 80 µA	

DSADC reference current:

$I_{REF\_max\_sum}$	= I_{REF_DSADC} * DSADC-twin-modulators
$I_{REF\_max\_sum}$	= 5.5 µA * 2 = 11 µA
$I_{REF\_max\_sum}$	= 11 µA

Total sum of all reference currents:

I_{AREF_tot}	= $I_{AREF\_max\_sum}$ + $I_{REF\_max\_sum}$ = 80 µA + 11 µA
I_{AREF_tot}	= 91 µA

The assumed maximum allowed charging error of the internal switched capacitors C_{AREFS} corresponds to the voltage drop at R_{AREF}:

V_{RAREF}	= LSB_{12} / 2 = 5 V / 4096 / 2
V_{RAREF}	= 610 µV

Calculation of R_{AREF_max}:

R_{AREF_max}	= V_{RAREF} / I_{AREF_tot} = 610 µV / 91 µA
R_{AREF_max}	= 6.7 Ω
R_{AREF_max}	= 6.8 Ω (value from E24 table)

2.2.2 Calculate C_{AREF_min}

Minimum buffer capacitance C_{AREF} per VADC without using the precharge feature

The relationship between the external capacitance C_{AREF}, the internal C-net C_{REFSW} and the assumed maximum error caused by C_{AREF} is:

(2.1)

$$C_{AREF} \geq 2^{r+E} \cdot \frac{C_{AREFSW}}{2}$$

with:

r = 8 : 8-bit resolution	E = 0 : $Error_{AREF}$ = LSB_r	$Error_{AREF}$ = $LSB_r / 2^E$
r = 10 : 10-bit resolution	E = 1 : $Error_{AREF}$ = $LSB_r / 2$	LSB_r = $V_{AREF} / 2^r$
r = 12 : 12-bit resolution	E = 2 : $Error_{AREF}$ = $LSB_r / 4$	

Note: The maximum voltage error ($Error_{AREF}$) at V_{AREF} caused by C_{AREF} is referenced to the allowed maximum input voltage at ANx ($V_{AINx} = V_{AREF}$). For input voltages at ANx smaller than V_{AREF} the additional in-accuracy at V_{AINx} is proportionally less than the value of $Error_{AREF}$ used in the example calculations. The real additional inaccuracy at V_{AINx} is:
$Error_{AREF\_real} = (V_{AINx} / V_{AREF}) * Error_{AREF}$ with the condition: $V_{AGND} \leq V_{AINx} \leq V_{AREF}$

Precharge factor calculation (PF: Precharge Factor)

The reference voltage precharge feature uses V_{DDM} for precharging the internal conversion capacitor net and V_{AREF} is used for the final adjustment during a conversion.

$$PF = Q_{CONV\_precharge} / Q_{CONV\_no\text{-}precharge}$$
$$PF = 20\ pC / 40\ pC$$
$$PF = 0.5$$

Minimum buffer capacitance C_{AREF} per VADC using precharge feature

Assumed maximum allowed charging error of the internal C-net of $LSB_{12}/2$ results in E = 1
Assumed resolution r = 12 bit

$$C_{AREF\_min} = 2^{r+E} * C_{AREFSW} / 2 * PF$$
$$C_{AREF\_min} = 2^{12+1} * 30\ pF / 2 * 0.5$$
$$C_{AREF\_min} = 61.4\ nF$$

Minimum buffer capacitance C_{AREF} for all VADCs using precharge feature

$$C_{AREF\_tot} = C_{AREF\_min} * \text{VADC-modules}$$

C_{AREF_tot} = 61.4 nF * 4 = 245.6 nF

C_{AREF_tot} = 270 nF (value from E24 table)

A minimum buffer capacitance C_{AREF} = 270 nF is necessary to provide enough charge to the internal conversion capacitor net.

2.2.3 Calculate R_{AREF}/C_{AREF} Filter Cutoff Frequency

When using R_{AREF_max} = 6.8 Ω and C_{AREF_tot} = 270 nF the cutoff frequency is:

f_{cutoff} = 1 / (2 * π * R_{AREF} * C_{AREF})

f_{cutoff} = 1 / (2 * π * 6.8 Ω* 270 nF)

f_{cutoff} = 86.7 kHz

This cutoff frequency suppresses the DC/DC converter switching noise frequency of $f_{DC/DC}$ = 480kHz.

2.2.4 Adapt C_{AREF} to suppress System Noise

Using the maximum accuracy of a 12 bit A/D converter requires filtering the DC/DC converters switching noise and providing enough current for ADC conversion at pin V_{AREF}. The RC filter circuit at the reference input voltage also has to suppress white noise and deterministic noise from the system which is higher than the A/D converter resolution. Therefore the calculated value of C_{AREF} has to be increased to a higher value to get a lower cutoff frequency.

A filter selection with a cutoff frequency of about 10kHz is a recommended setting. It has typically sufficient attenuation to suppress system noise in a system.

C_{AREF} = 1 / (2 * π * R_{AREF} * f_{cutoff})

C_{AREF} = 1 / (2 * π * 6.8 Ω * 10 kHz)

C_{AREF} = 2.34 µF

C_{AREF} = 2.2 µF (value from E24 table)

Using a V_{AREF} filter circuit with R_{AREF} = 6.8Ω and C_{AREF} = 2.2µF has sufficient attenuation to suppress system noise in a typical application. The filter curve is shown in **Figure 4**.

In case of increased noise on the A/D converter results a further cutoff frequency decreasing can help to suppress this noise. This is typically done by increasing the value of C_{AREF}. The ESR (Equivalent Series Resistance) value of the uses ceramic capacitors should be as low as possible.

Note: Increasing R_{AREF} also decreases the cutoff frequency, but this can cause a certain additional gain error to the result because of the increased voltage drop at R_{AREF}.

Reference Supply Voltage Filter Calculation (V_{AREF})

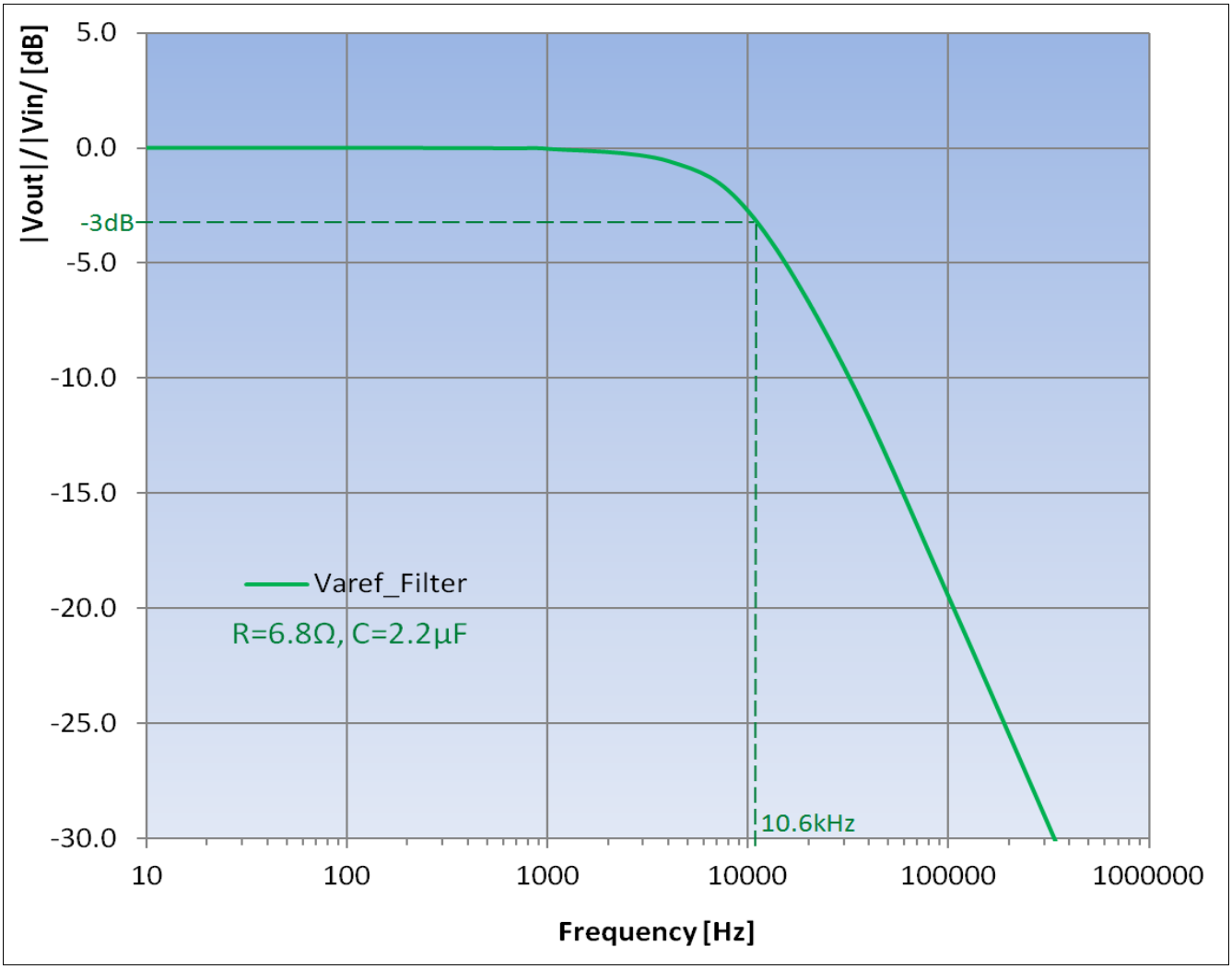

Figure 4 Analog Reference Voltage V_{AREF} RC Filter Curve with R_{AREF} = 6.8 Ω and C_{AREF} = 2.2 µF

3 Analog Input Filter Calculation (ANx)

During the sample phase, the conversion control unit connects the capacitors of the conversion C-net to an analog input channel via a multiplexer. The internal switched capacitor field C_{AINSW} is then charged or discharged to the voltage level of the connected analog input channel.

In typical applications the external capacitance value has to be high enough that the total charge, which is necessary to load the internal capacitor field C_{AINSW} of the A/D converter, is provided by the external capacitor C_{EXT}. The resistance of the analog source has to consider the cycle time, the duration from the start of a conversion to the next conversion start of the same analog channel, and protection of the input in case of an overload situation. The details for how to calculate the circuit at the analog input are described in the application note AP56003 “A Guide to the Analog Part of the A/D converter”.

Because of the common ground concept of the AURIX™ Family some of the periodic system noise can be distributed also to the “analog” ground area of the PCB. If there is no appropriate filter circuit at the analog input, this noise can cause an increased Offset Error!

That is why the calculated external filter circuit based on the charging demands also has to be checked whether it fulfils the Nyquist-Shannon sampling theorem. The filter at the analog input needs a time constant of at least two times the sample time of the considered channel.

Due to the stopband attenuation of a passive low-pass filter, it is recommended to use a time constant τ_{filter} of the external bandwidth limitation filter of at least four times higher than the configured sampling time of the A/D converter. The details are shown in the block diagram below.

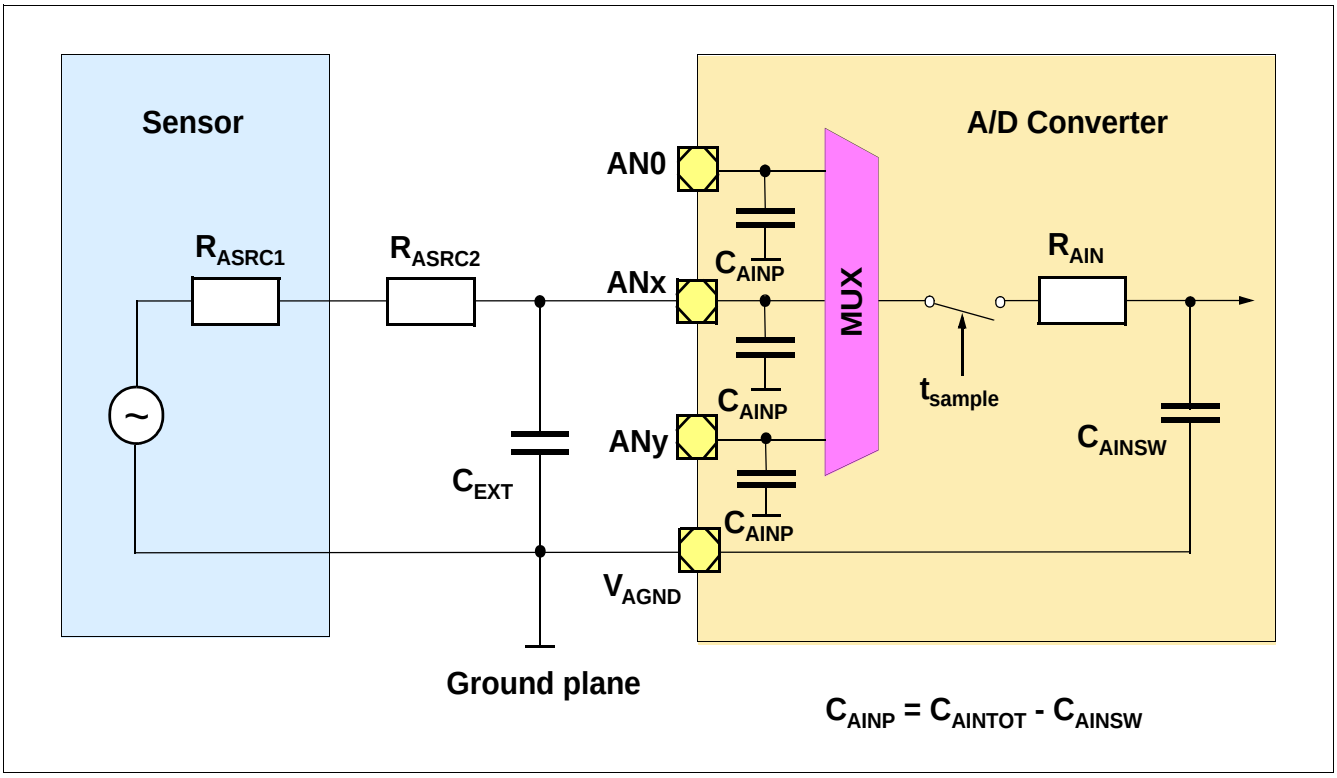

Figure 5 A/D Converter Input and Input Filter at ANx

3.1 How to calculate a Noise Filter at the ANx?

The time constant τ_{ANx} of the external analog input circuitry calculated on the base of AP56003 has to fulfil these conditions:

$$\tau_{filter} \geq 4 * t_{sample}$$
$$\tau_{ANx} = R_{ASRC} * C_{EXT}$$
$$R_{ASRC} = R_{ASRC1} + R_{ASRC2}$$

Note: In typical applications the external analog input filter fulfils the Nyquist-Shannon sampling theorem. Only systems using external op-amps sometimes leave the external capacitor C_{EXT}. In these cases an external capacitance C_{EXT} is required to suppress noise at the analog input.
If the external input capacitance is in the range of $C_{EXT} < (2r * C_{AINSW})$ then the resistance of the analog source and the sampling time have to be adjusted such that the internal capacitor field C_{AREFSW} is charged to a sufficient accuracy. Details are described in AP56003.

3.2 Calculation Example

The assumed values for this example:

C_{AINSW_max}	= 7 pF	t_{sample}	= 100 ns (value from user software)
resolution r	= 12 bit	R_{ASRC}	= 10 kΩ

Based on application note AP56003 with ($C_{EXT} > (2^r-1) * C_{AINSW}$) the conditions for the external tank capacitance are:

$$C_{EXT} > (2^r-1) * C_{AINSW}$$
$$C_{EXT} > (2^{12}-1) * 7\ pF$$
$$C_{EXT} > 28.6\ nF$$
$$C_{EXT} = 33\ nF \text{ (value from E24 table)}$$

The required time constant τ_{filter} is:

$$\tau_{filter} \geq 4 * t_{sample}$$
$$\tau_{filter} \geq 4 * 100\ ns$$
$$\tau_{filter} \geq 400\ ns$$

The time constant τ_{ANx} of the calculated analog input filter is:

$$\tau_{ANx} = R_{ASRC} * C_{EXT}$$
$$\tau_{ANx} = 10\ k\Omega * 33\ nF$$
$$\tau_{ANx} = 330\ \mu s$$

The time constant τ_{ANx} of the used analog input filter with R_{ASRC} = 10 kΩ and C_{EXT} = 33 nF fulfils the requirement of $\tau_{filter} \geq 400$ ns. The filter cutoff frequency is 482 Hz. The curve is shown in **Figure 6**.

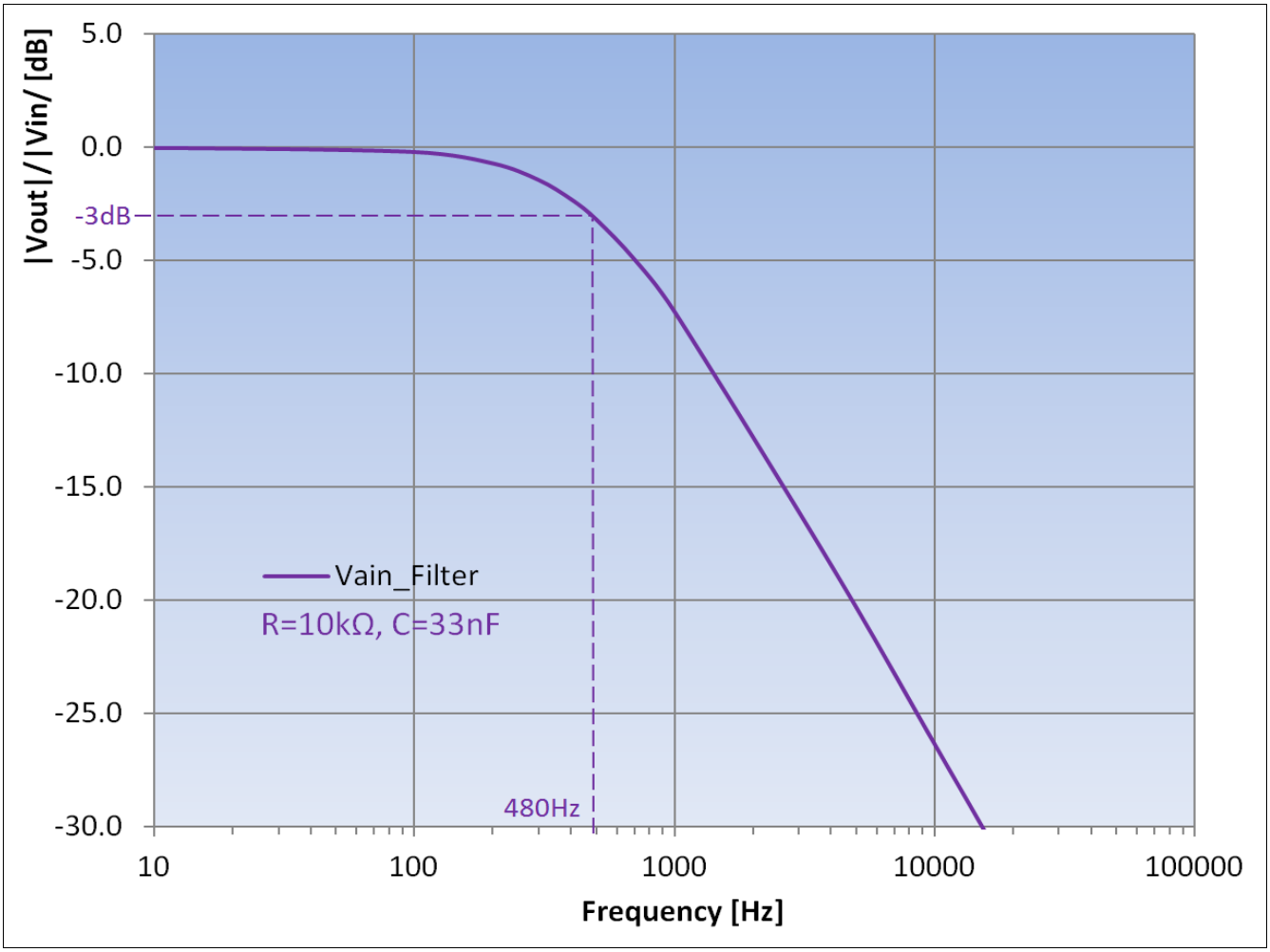

Figure 6 Analog Input ANx RC Filter Curve with R_{ASRC} = 10 kΩ and C_{EXT} = 33 nF

4 Filter Circuit Calculation Example Results Summary

The recommended settings from the example are:

R_{AREF}	= 6.8 Ω	C_{AREF}	= 2.2 µF
R_{DDM}	= 1.2 Ω	C_{DDM}	= 330 nF
R_{ASRC}	= 10 kΩ	C_{EXT}	= 33 nF

The filter block diagram and the filter curves are shown in the figures below:

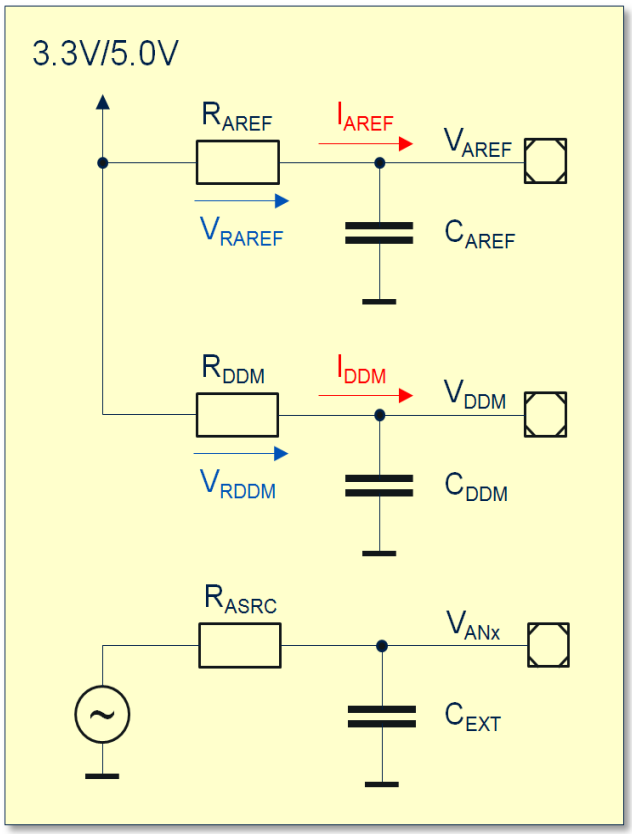

Figure 7 Block Diagram of the RC Filters at V_{DDM} , V_{AREF} and V_{ANx}

Filter Circuit Calculation Example Results Summary

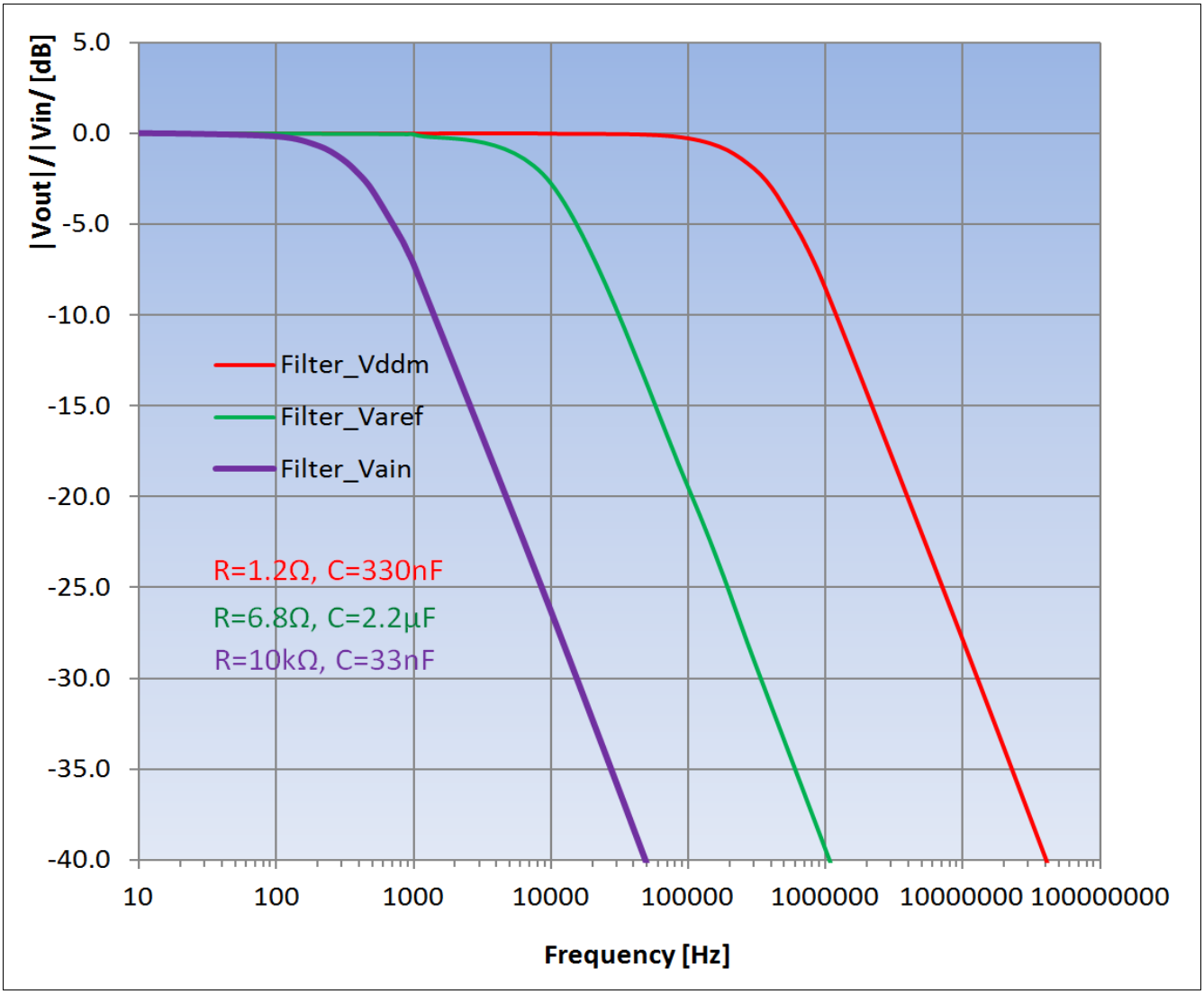

Figure 8 RC Filter Curves for V_{AREF}, V_{DDM} and V_{AINx}

5 PCB and Design Guidelines

Here we provide a short introduction to mixed signal board design and offer a list of guidelines for optimum printed circuit board layout for AURIX™ microcontrollers with special consideration for the A/D converter. A general system wiring of the supply pins is shown in **Figure 9**.

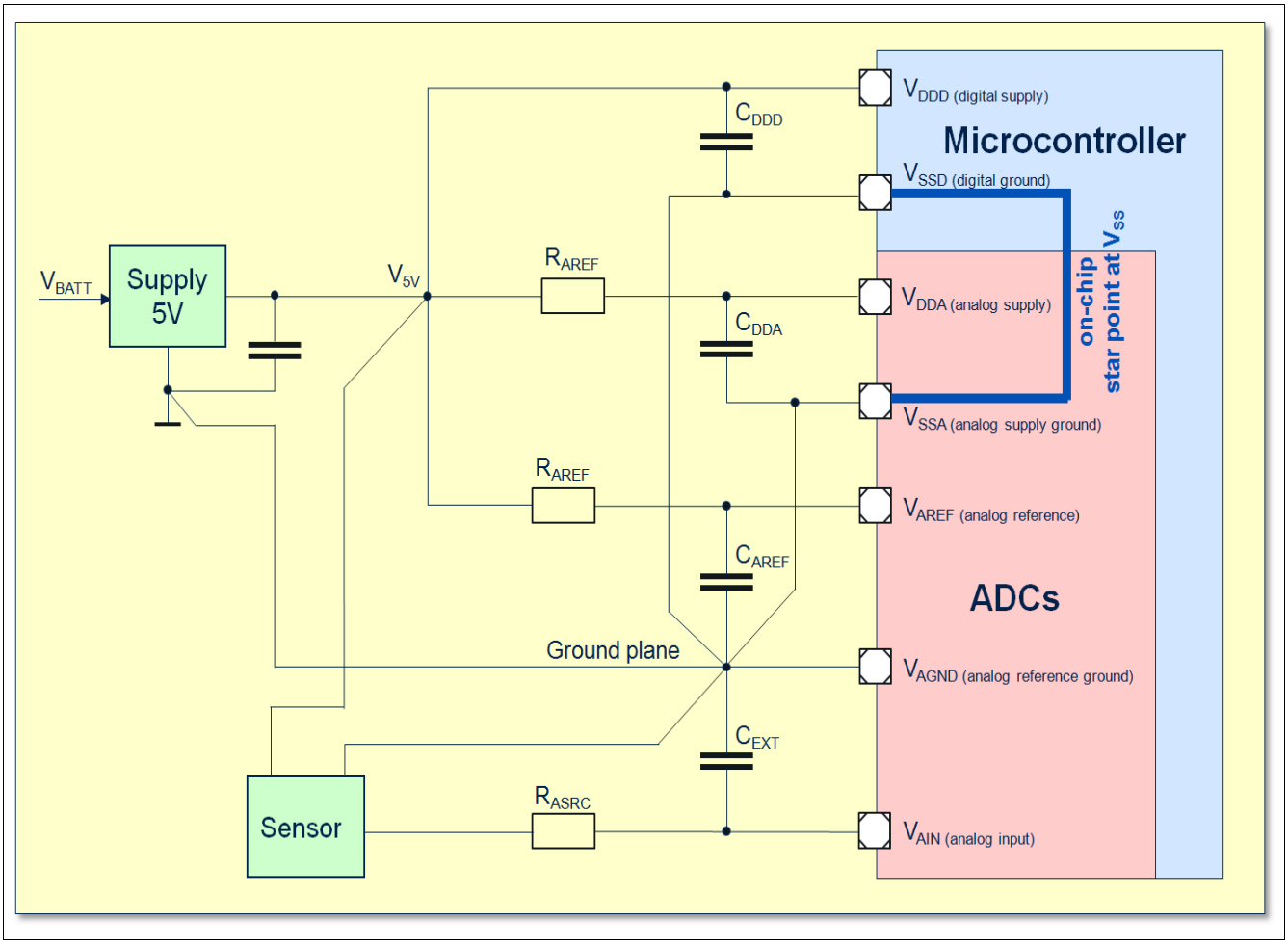

Figure 9 Example how to connect analog and digital Supply on a PCB

5.1 Ground Plane

Inside the AURIX™ microcontrollers the analog ground and the digital ground are already shorted on-chip. Therefore the PCB ground plane is no more separated in an analog and a digital part. AURIX™ microcontrollers require only **one** common ground plane for analog and digital signals on the PCB.

Note: ***This common ground plane is the most important reference point in the system!***

The ground node is an impedance where offsets are caused by static and dynamic currents. This voltage offsets have to be smaller than the desired target resolution of the A/D converter.

Guidelines for the ground plane

- Keep the ground plane impedance as low as possible.
- Use a PCB with a square wave ground plane.

- All chip grounds, analog and digital, have to be connected to the PCB common ground plane.
- The sum of all injected currents to the ground plane is known and must be checked whether it fits to the ground plane impedance.
- Remove noisy system parts from the PCB or reduce ground plane impedance.

5.2 Component Placing

Guidelines:

- Partition the board with all analog components together in one area and all digital components in the other. An example is shown in **Figure 10**.
- Analog and digital signals have to be separated with sufficient spacing between to prevent noise coupling.
- Shielding of sensitive analog signals can suppress noise coupling.
- Mixed signal components, including the microcontroller, should only bridge the analog and digital areas. Rotating the microcontroller can often make this task easier.
- The microcontroller has to be soldered on the PCB. **Do not use a socket**!
- Minimize PCB complexity to keep the PCB to a small size.
- Keep all traces as short as possible.

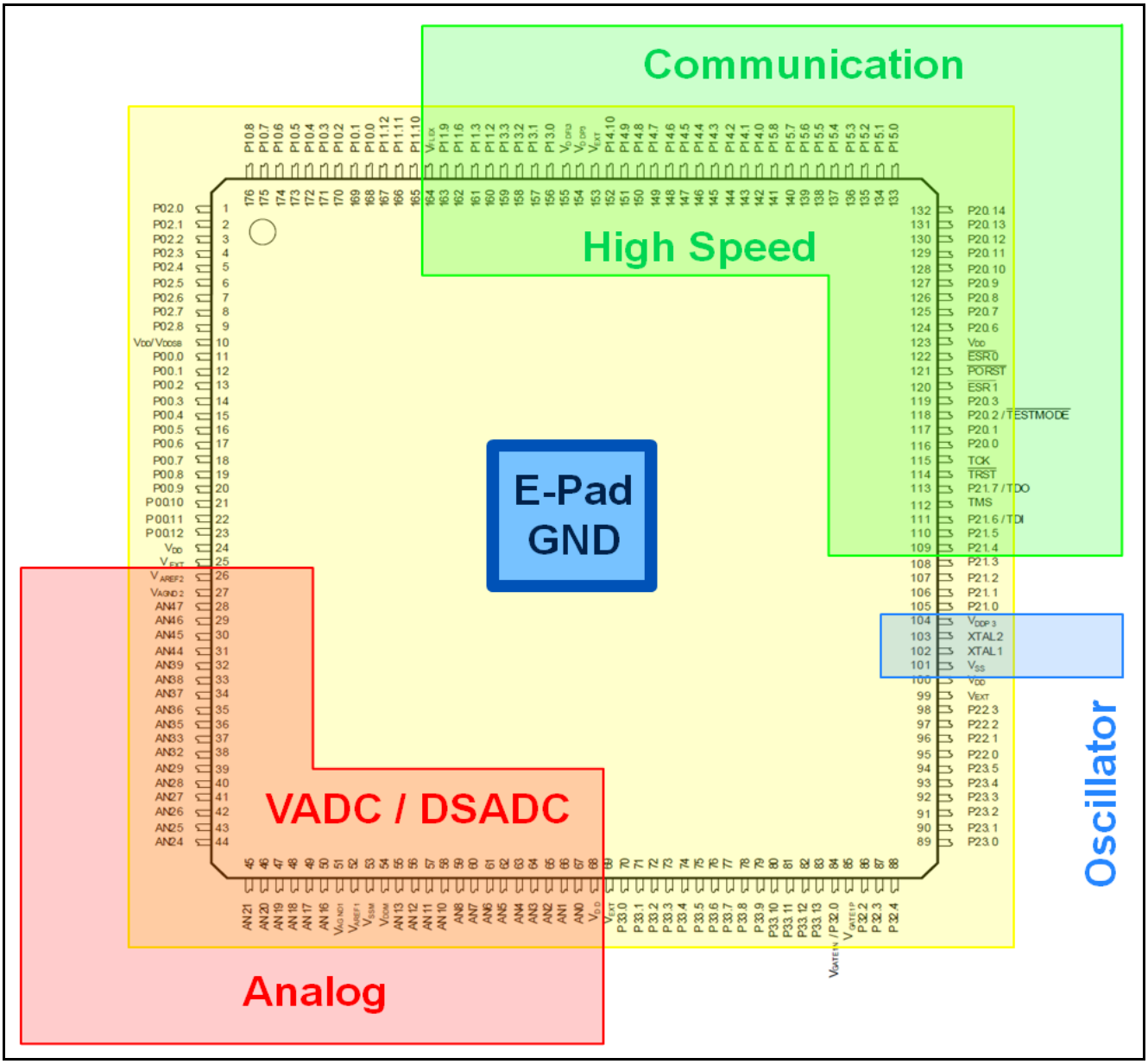

Figure 10 Example for functional Partitioning

5.3 Power Supply and Supply Voltages

Guidelines:

- Place de-coupling capacitors as close as possible to the microcontroller pins, or positioned for the shortest connection to pins with wide traces to reduce impedance.
- If both large and small ceramic capacitors are recommended, position the small ceramic capacitor closest to the microcontroller pins.
- Use capacitors with small ESR values.
- Use separate power supplies for analog and digital modules.
- Prevent power supply noise injection to the GND plane (i.e. switched mode power supplies).
- Use high quality connectors to connect the PCB to an external system to ensure high quality input signals.
- Connections to external system should be as short as possible.

5.4 Signal Traces

Guidelines:

- Analog signal traces are placed in the analog area.
- Digital signal traces are placed in the digital area.
- Regions between analog signal traces and also regions between digital signal traces should be filled with copper, which should be electrically attached to the common ground plane. These regions should not be left floating as this increases interference.

5.5 Clock Generation

Guidelines:

- Locate the quartz crystal, ceramic resonator or external oscillator as close as possible to the microcontroller.
- Use a ground island for oscillator load capacitor ground which is directly connected to oscillator ground.
- Keep digital signal traces, especially the clock signal, as far away as possible from the analog input and voltage reference pins.
- Avoid multiple oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D converter sampling clock.

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