TriCore™ Family

DXCPL DAP over CAN Physical Layer

AP32264

Application Note

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Revision History

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V 1.1, 2014-10-31	
Figure 1-2	SPD protocol now shown with DXCPL signal levels

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1 Introduction

DAP over CAN Physical Layer (DXCPL) enables a tool connection via the regular CAN pins of the ECU connector. This tool connection is robust since it does not require a working flash or any software.

DXCPL is in essence another option to transmit DAP telegrams (**Figure 1-1**).

The CAN bus physical layer is a bidirectional connection with differential encoding on a single pair of wires. An external CAN transceiver translates between the logical level of the TX/RX device pins and the electrically robust signaling of the CAN bus. This direction separated signaling with TX/RX can be used to transmit **SPD (Single Pin DAP)** encoded DAP messages. **Figure 1-1** shows the device internal DXCPL building blocks between CAN pins and DAP module.

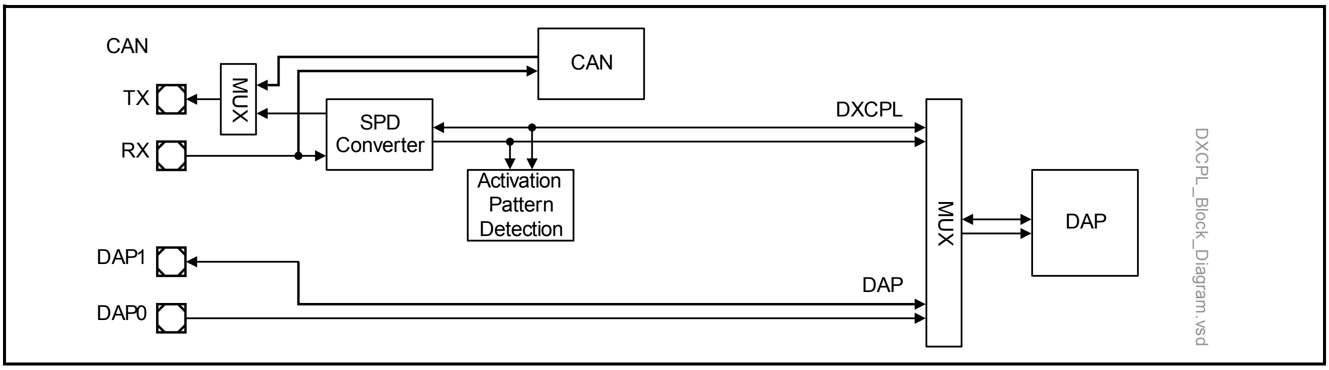

Figure 1-1 DXCPL Block Diagram from CAN Pins to DAP Module

DXCPL Application

Since the CAN bus signals are available at the ECU connector, DXCPL allows tools to be connected without opening the ECU housing.This is very useful for example, for a cost effective analysis of field returns.

After activation the OCDS debug infrastructure is accessible with similar restrictions to those of a regular DAP connection (e.g. access of a locked device only after authentification). As a difference to DAP boundary scan is not possible since the CAN pins are part of the scan chain.

SPD (Single Pin DAP)

The SPD protocol encodes the DAP bits with the distances between the SPD signal edges. For example:

- A DAP1 value of '0' is encoded with a short distance
- A value of '1' will be twice the distance (**Figure 1-2**).

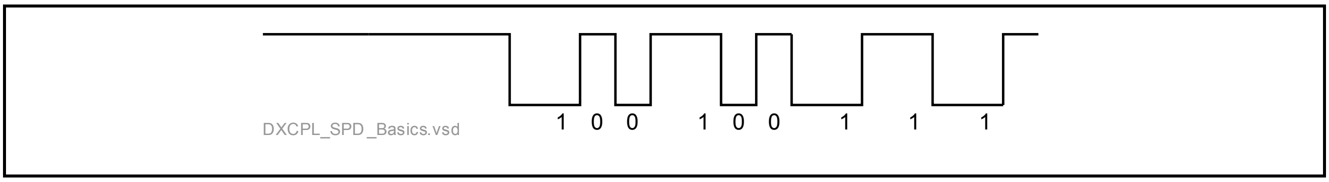

Figure 1-2 SPD Basic Protocol

A typical encoding distance is 0.67µs/1.33µs, which provides the data bandwidth of a 1 MHz regular DAP connection. Please note:

- The SPD protocol is very robust against variations of the clock source from sender and receiver.
- SPD bandwidth figures assume an even distribution of the short '0' and twice as long '1' bits.
- A cycle of an applied "clock" signal contains two edges, which means two SPD bits.

1.1 DXCPL Activation

The DXCPL activation pattern is defined as 1024 consecutive ‘0’-values in SPD format (512 “clock” cycles). This means permanent signal changes below the decision point (**Table 2-1**) of the SPD receiver on the device.

Note: Depending on the situation (for example the EVR oscillator is not trimmed), the devices internal SPD decision point will be biased. In such a case a tool can retry with a 20% shorter/longer edge distance. As soon as the device responds to a DAP sync telegram, the device internal biasing of the decision point can be determined and the tool can adapt accordingly for a robust communication.

*Note: The decision point in **Table 2-1** is the upper limit for detecting a ‘0’-value in SPD format. The lower limit is given by the cut-off frequency of the CAN transceiver. This means that a periodic signal in the MHz range can stimulate the DXCPL activation (**Fault Scenario: Stimulated Oscillating CAN Network**).*

Valid or ‘legal’ CAN traffic has certain features:

- The CAN protocol consists of specific frames (data-, remote- and error-frames) with a maximum length of up to 128 bits, where the last seven End-of-Frame bits are transmitted as ‘1’. At least three more ’1’ bits must follow before the next frame can start.
- CAN data rate is 512 kbit/s, or fastest 1 Mbit/s. So a signal change will not occur faster than every 1-2µs.
- For CAN FD the data payload of maximum 64 bytes is too small to have an unintended activation by a data pattern.

Safeguards are also built into the pattern matcher:

- SPD will assume a ‘1’-value whenever the time between two signal changes is longer than the decision point, which is always the case at the end of every CAN frame.
- Whenever SPD identifies a ’1’ before 1024 ‘0’-values have been seen, the **whole** activation sequence must be restarted.

Last but not least, the behavior of the CAN bus system must be considered, especially when the tool is plugged onto a “live” bus:

- Because the transmission of SPD-conforming ‘0’-values represents a violation of the CAN-protocol, any active CAN-node will react by actively sending an error-frame.
- This is repeated (by the same or another node) until the internal error counter(s) overflow(s).
- Sooner or later all nodes will reach this state and be disabled automatically.
- These error frames may disturb the SPD activation sequence when a ’1’ results from any bus conflict. This may require that more than 1024 ‘0’-values must be transmitted until SPD is activated.

The DXCPL/SPD active operating condition is also indicated to any user software by the SCU register bit **STSTAT.SPDEN**. This means that errors reported by the disconnected CAN module can be ignored.

DXCPL Deactivation

Switching the interface pins back to regular CAN mode is only possible through Power-on Reset.

DXCPL Activation Prevention

DXCPL activation can be suppressed by configuration and by software. The device family specific details are available in **Table 2-1**:

- Activation is already suppressed by the startup software when the **PROCONxxx.DATM** bit is set (irreversible).
- Activation can be (temporarily) suppressed by application software by setting **SYSCON.DATM**.
- Activation is also suppressed when the $\overline{\text{TRST}}$ pin was statically inactive since Power-on Reset.

2 TriCore™ Device Family Differences

The identifier DXCPL was introduced with the AURIX™ family, replacing the term Application Test Mode (ATM) that was previously used in the documentation.

Table 2-1 DXCPL SPD Parameters

	AUDO MAX	AURIX
Devices	TC172x, TC179x	TC2xx
CAN pins	RXDCAN0 TXDCAN0 TC172x: P3.12, P3.13 TC179x: P6.8, P6.9	RXDCAN1B TXDCAN1 P14.1, P14.0
Enabling precondition	$\overline{\text{TRST}}$ pin has been active since Power-on Reset	
Clock source	Crystal (8-20 MHz)	EVR oscillator (100 MHz)
SPD clock	4-10 MHz	6.25 MHz
Edge distance ‘0’ sender	0.50 µs (20 MHz crystal) 1.00 µs (10 MHz crystal)	0.80 µs +/- EVR accuracy
Edge distance ‘1’ sender	1.00 µs (20 MHz crystal) 2.00 µs (10 MHz crystal)	1.60 µs +/- EVR accuracy
Decision point of receiver	0.65 µs (20 MHz crystal) 1.30 µs (10 MHz crystal)	1.04 µs +/- EVR accuracy
Sample error (+/-) of receiver	0.05 µs (20 MHz crystal) 0.10 µs (10 MHz crystal)	0.08 µs +/- EVR accuracy
Activation prevention Permanent By application software	 PROCON2.bit[30] (DATM) SYSCON.bit[8] (DATM)	 PROCONWOP.DATM SYSCON.DATM
Activation prevention (irreversible)	PROCON2.bit[8] (DATM)	PROCONWOP.DATM
Activation status	STSTAT.bit[20] (SPDEN)	STSTAT.SPDEN

3 Usage Hints

3.1 Halt After Reset

It is possible to have a reliable Halt After Reset Request (HARR) with DXCPL. For locked devices the HARR sequence needs to be extended by the password exchange. The tool needs to execute the following steps:

HARR by controlling the $\overline{\text{PORST}}$ Pin

- Release the $\overline{\text{PORST}}$ pin.
- Wait approximately 100 µs for on-board and device internal Power-on Reset release.
- Apply the **DXCPL Activation** sequence (optional shortened to approximately 300 µs with just 0.3 µs edge distance).
- Proceed with the DAP HARR telegram sequence.

HARR without controlling the $\overline{\text{PORST}}$ Pin

It is possible to have a reliable HARR even when the tool does not control the $\overline{\text{PORST}}$ pin.

- The tool periodically sends the **DXCPL Activation** sequence (optional shortened to approximately 300 µs with just 0.3 µs edge distance) and a DAP sync telegram.
- When the device responds to the sync telegram, proceed with the DAP HARR telegram sequence.

3.2 Case: DXCPL CAN Pins also used for ASC Bootloader

If the DXCPL/RXDCAN pin is shared with the ASC and an Alternate Boot Mode (ABM) with ASC interfacing is used, it might happen in the range over approximately 1 MBaud that long sequences of $AAAA_H$ (transmitted as the filling pattern for the Flash for example) are erroneously interpreted as the SPD activation pattern. An enabled SPD interface would then disturb the ASC communication by "replying".

In order to avoid this corner case scenario, it is recommended to temporarily disable the DXCPL interface (see **DXCPL Deactivation**).

3.3 Fault Scenario: Stimulated Oscillating CAN Network

It has been reported that a not properly designed CAN network can oscillate in the MHz range when it is stimulated in the development phase. In this case it may even happen that the time window between internal Power-on Reset release and permanent activation prevention (**PROCONxxx.DATM**) by startup software, is of such a length that DXCPL is already enabled. This means that CAN communication is no longer possible, even when the CAN network has stopped oscillating. To recover from this situation:

- The application software checks at startup if DXCPL has already been activated (**STSTAT.SPDEN**). If it has, then the software should make an entry in the error log and trigger a Power-on Reset of the ECU.

This approach mitigates the fault scenario and detects as a side-effect the (sporadically) oscillating CAN network.

Another option to prevent the DXCPL activation completely is to keep $\overline{\text{TRST}}$ statically inactive. Please note that this activates the DAP interface.

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