TriCore™ AURIX™ Family

32-bit (TC23x, TC22x)

PCB design Guidelines

AP32261

Application Note

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Microcontrollers

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Revision History

Major changes since previous revision

Date	Version	Changed By	Change Description
04.11.2014	V1.1	M.Gökcen	Tables1-5 updated, Fig.-8 added, Chapter 3.1 added.
09.10.2015	V1.2	M. Gökcen	Table-1,-2,-3 updated

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1 About this document

1.1 Scope and purpose

The TC22x and TC23x are part of the AURIX™ family of 32-bit microcontroller products. They are available in TQFP-80, TQFP-100, TQFP144 and LFBGA-292 packages, which requires a PCB carefully designed for electromagnetic compatibility.

This document provides product-specific recommendations and guidelines for the TC22x and TC23x, and should be read in conjunction with the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule information for PCB design.

Note: This document contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by the customer, based on their specific implementation choices.

2 Pinouts

2.1 General Information

The microcontroller has four supply domains which should be decoupled individually:

- VDD = 1.3V for Core
- VDDP3 = 3.3V for I/O Pad
- VDDM = 3.3V, or 5V for ADC

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

2.2 Packages

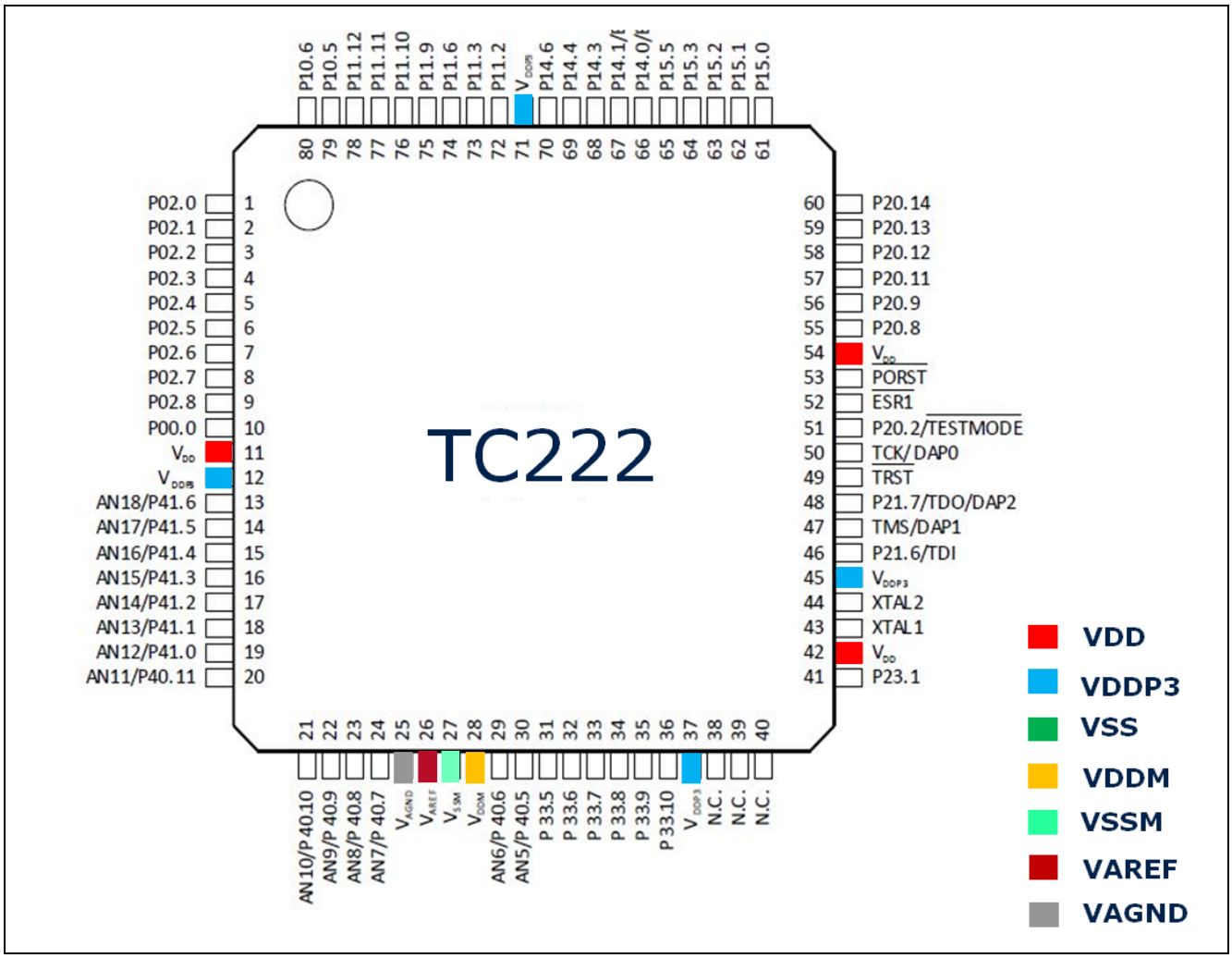

Figure 1 TC222 package

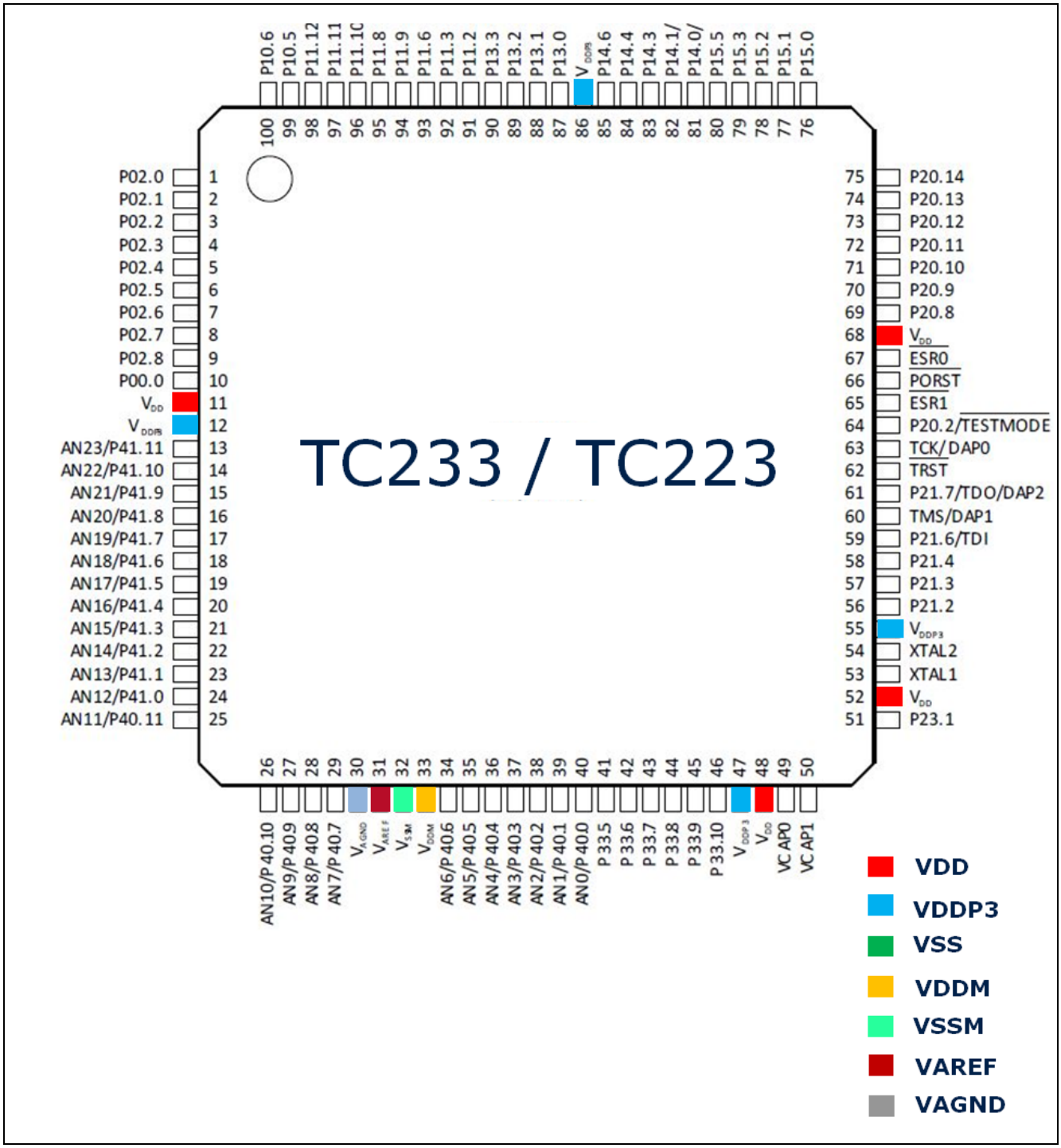

Figure 2 TC233 / TC223 package

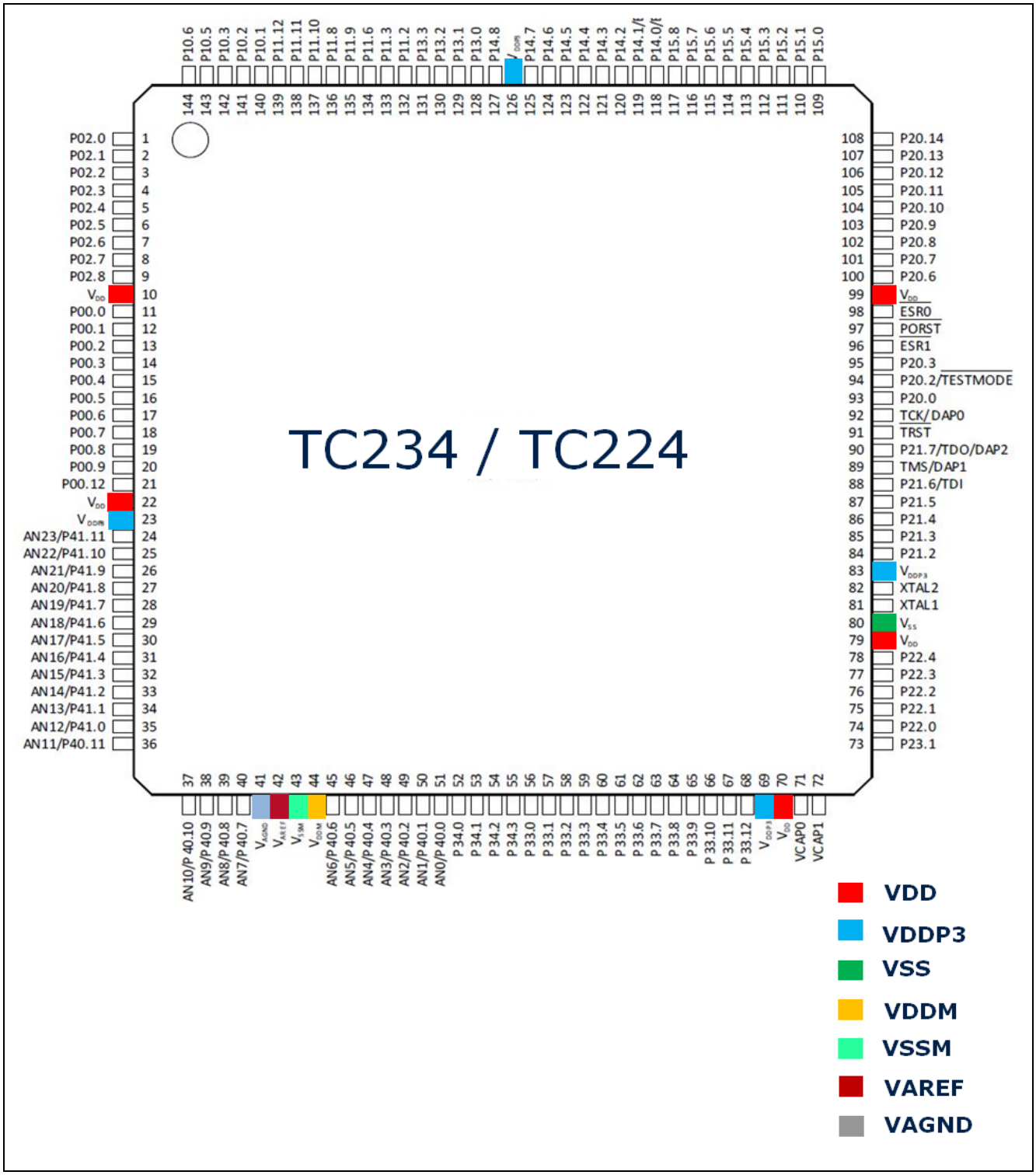

Figure 3 TC234 / TC224 packages

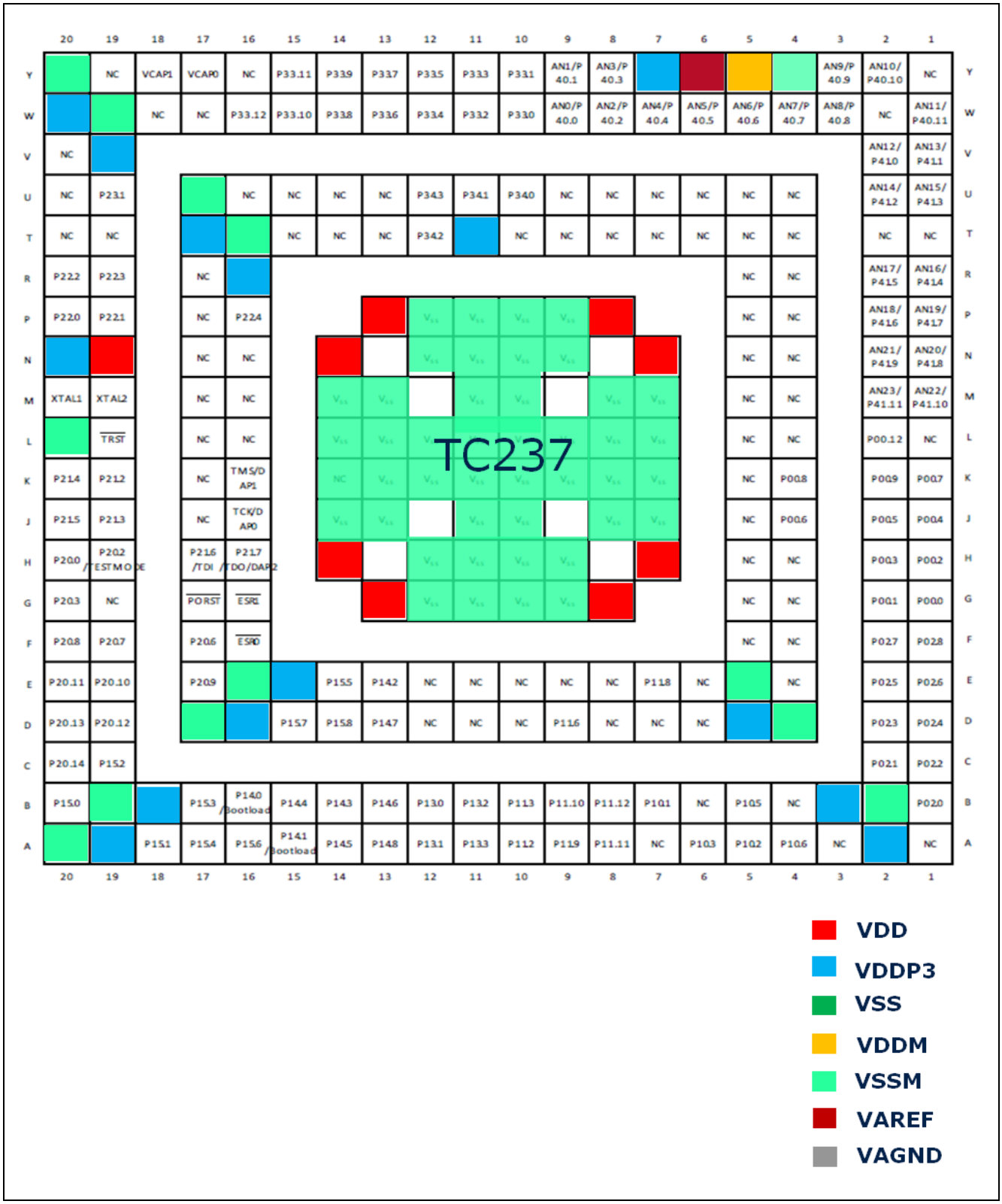

Figure 4 TC237 package

3 PCB Design Recommendations

Decoupling the Power Distribution Network of the microcontroller IC is critical to the PCB design process, because careful selection of the decoupling capacitors and placement has a big influence on the high speed performance of the board, and can reduce the emissions.

The on-board decoupling capacitors have an effective range of 1MHz – 200MHz.

The range above 200MHz can be covered by using power plane capacitance.

The effectiveness of the decoupling capacitors depends on the optimum placement and connection type.

Recommendations

- Place the µC and Connector with high speed signals first, to ensure minimal length of the traces.
- Do not place other components between the Connectors and the µC.
- Place possible noise sources away from the high speed signals.
- Components that communicate with devices outside the board should be placed at the edge of the board.
- Place capacitors as close as possible to the µC.
- Keep the interconnection inductance of capacitors to the µC as low as possible.
- Use low effective series resistance and inductance (ESR and ESL) capacitors.
- Since parasitic inductance is the limiting factor of the capacitor response to high frequency demand of current from the device, the ESL of the capacitor and the connection inductance should be selected so that the optimum value for the design is reached.
- Connect capacitors with vias close to the side of the pads.
- Use side placement of the vias to reduce the current loop.
- Dual vias can be used to reduce the parasitic inductance.
- Solder lands, traces and vias should be optimized for capacitor placement.
- Do not use long traces to connect capacitors to GND or to VDD.
- Always keep the return path of the high frequency current (lowest inductance path) small.
- Select the smallest package available for the capacitors.
- Select capacitors of type: ceramic multilayer X7R or X5R.

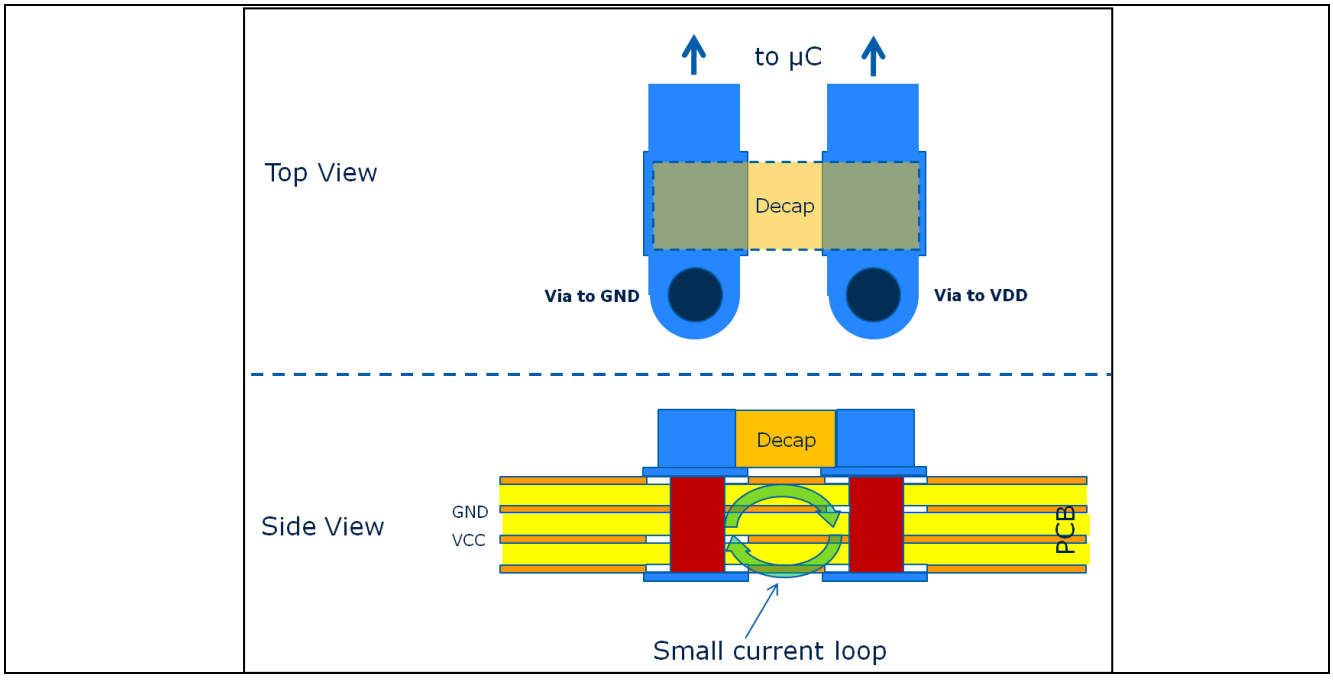

Figure 5 Decaps connection

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for the load capacitors and Xtal should be as short as possible.

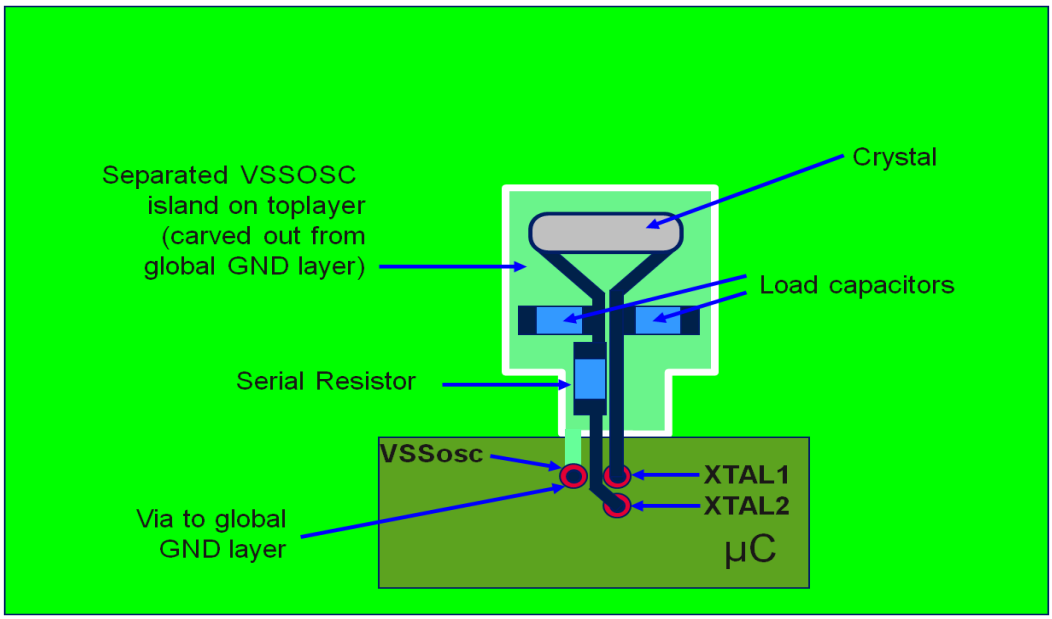

Figure 6 Layout proposals for Oscillator circuit (shown for BGA Package)

- To minimize the EMI radiation on the PCB, the following signals are to be considered as critical:

1. *ERAY Pins*
2. *Ethernet Pins (Only for ADAS & ED)*
3. *QSPI Pins*
4. *External Clock Pins*
5. *Supply Pins*
   - Route these signals with adjacent ground reference and avoid signal and reference layer changes.
   - Route them as short as possible.
   - Routing ground on each side can help to reduce coupling to other signals.
   - The ground system must be separated into analog and digital grounds. The analog ground must be separated into two groups:
   - Ground for OSC / PLL supply pins as common star point.
   - Ground for ADC (VSSM for VDDM) as common star point.
   - The power distribution from the regulator to each power plane should be made over filters.
   - RC Filters can be inserted in the supply paths at the regulator output and at the branching to other module supply pins like VDD and VDDP3 (for osc.) and VDDM.
   - Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net.
   - OCDS must be disabled.
   - Select weakest possible driver strengths and slew rates for all I/Os (see AP32111 “Scalable Pads”).
   - Use lowest possible frequency for SYSCLK.
   - Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

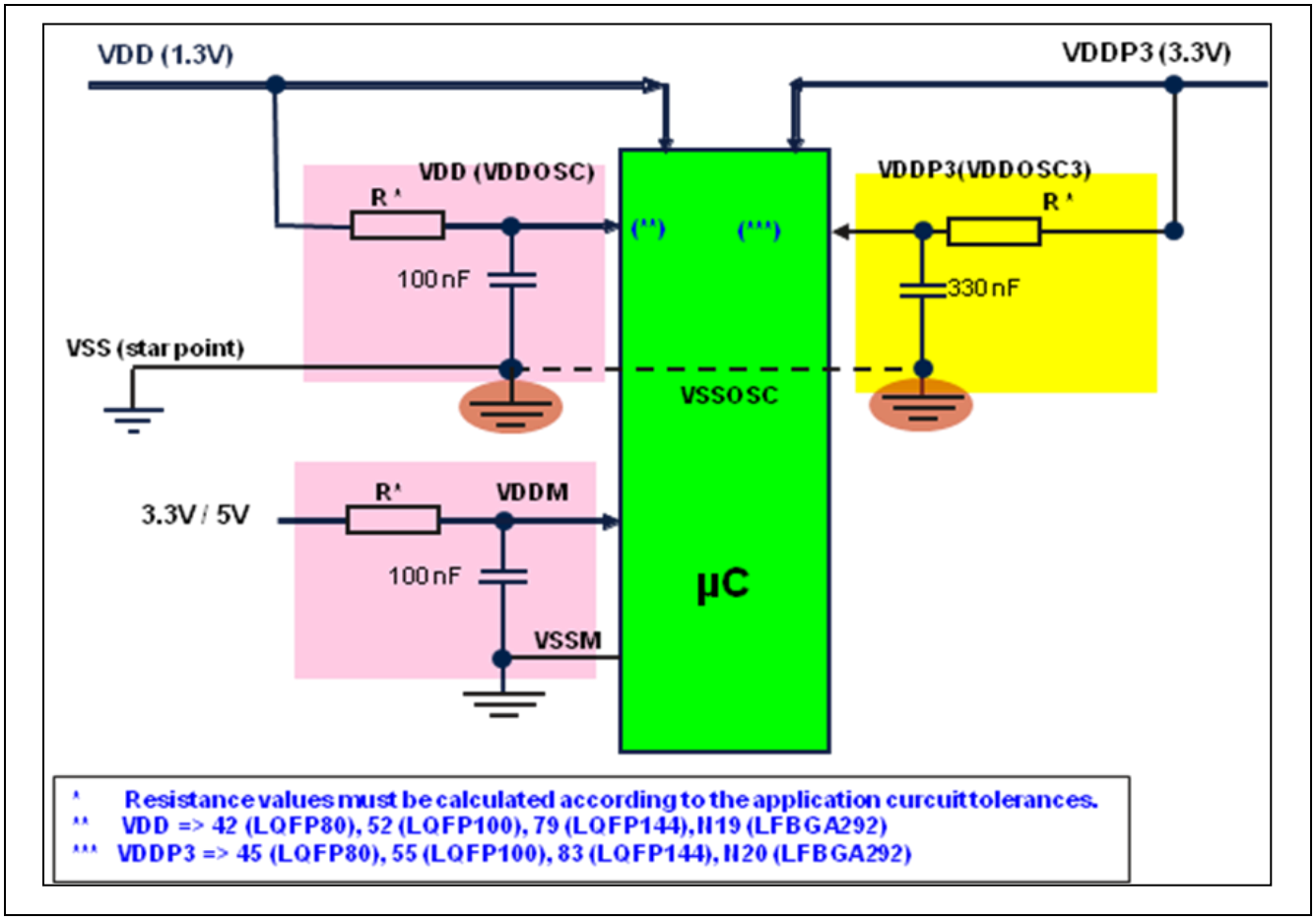

Figure 7 Filtering of VDD, VDDP3 and VDDM supply pins for TC22x – TC23x

3.1 Recommendation for unused pins

In case of not using all I/O-Pins of the microcontroller, it is recommended to take some measures on software and PCB. Table-1 gives an overview of the measures for different I/O-Pins. The measures given in the table are optimized from EMC point of view. If this is not required, other measures are also applicable.

Table 1 Considerations for unused "Output, Supply, Input and I/O" pins

I/O Type:	Measure	Reason
Supply Pins (Modules)	See the User´s Manual.	-
I/O-Pins	Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pull-up or pull-down is also possible. Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).	In case of an emergency stop, it is possible that the I/Os are switched to high state. This leads to a damage of the I/O if it is connected to GND (electro migration stress current). If output is active and the level is defined, no unexpected switching of the input path is possible.
Output Pins including LVDS	Should be driven static in the weakest driver mode. If static output level is not possible, the output driver should be disabled. Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).	Defined potential of the output stage (In some cases multiplexer output as alternate function) reduces leakage current and improves immunity.
Input Pins without internal pull device	For pins with alternate function, see product target specification to define the necessary logic level. Should be connected with a resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).	This avoids the initial current consumption peaks after reset of the device by defined level at inputs. These current peaks can be caused by uncontrolled switching of the Schmitt-trigger of the input due to leakage currents.
Input Pins with internal pull device	For pins with alternate function see product specification to define the necessary logic level Should be configured as pull-down (Exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. Solder pad should not be connected to any other net (isolated PCB-pad only for soldering)	This avoids the initial current consumption peaks after reset of the device by defined level at inputs. These current peaks can be caused by uncontrolled switching of the Schmitt-trigger of the input due to leakage currents.

4 Example Layouts for the AURIX™ Family

The AURIX™ TC22x and TC23x 32-bit microcontroller products are available in the following packages:

- TQFP-80
- TQFP-100
- TQFP-144
- LFBGA-292

The microcontrollers have the following supply domains:

- **VDD=1.3V for Core**
- **VDDP3=3.3V for I/O Pad**
- **VDDM=3.3V or 5V for ADC**

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

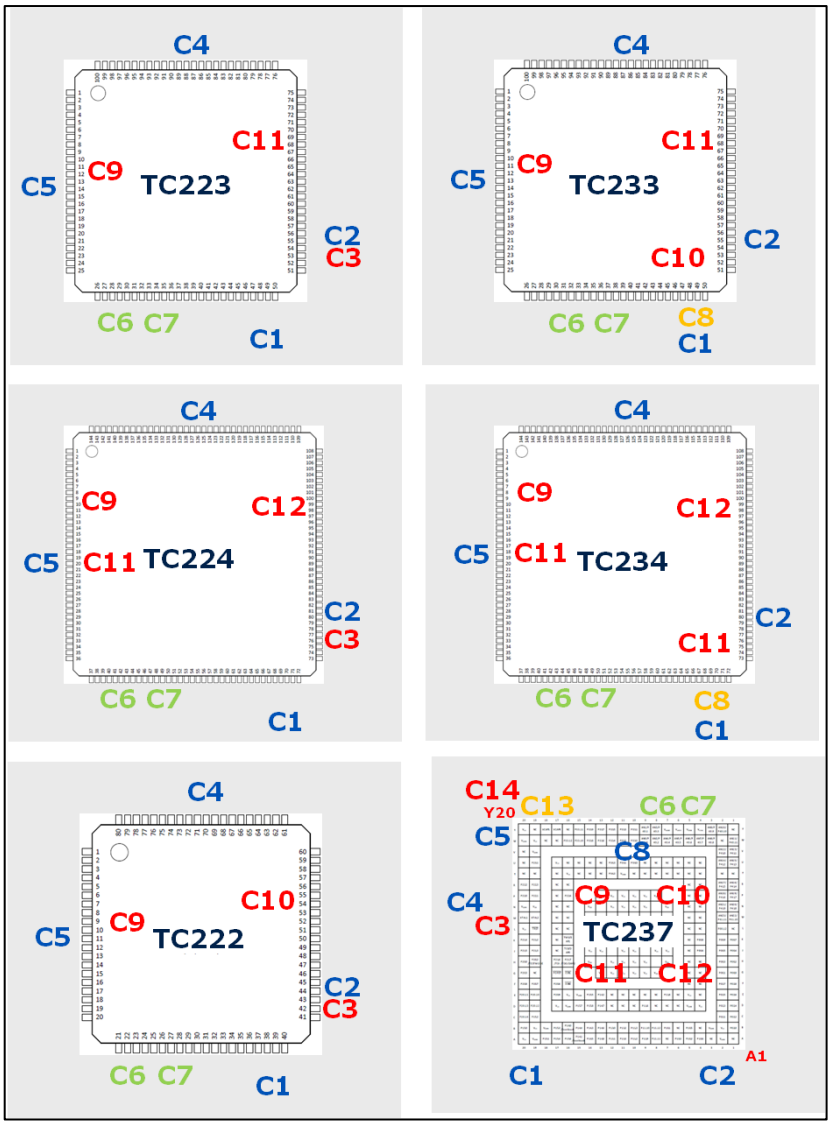

Figure 8 Decoupling capacitor placement overview according to the layout examples for TC22x and TC23x in Figures 9 -12 (C8 / C13: Flying Capacitor for SMPS mode)

4.1 Example Layout for TQFP-80 Package

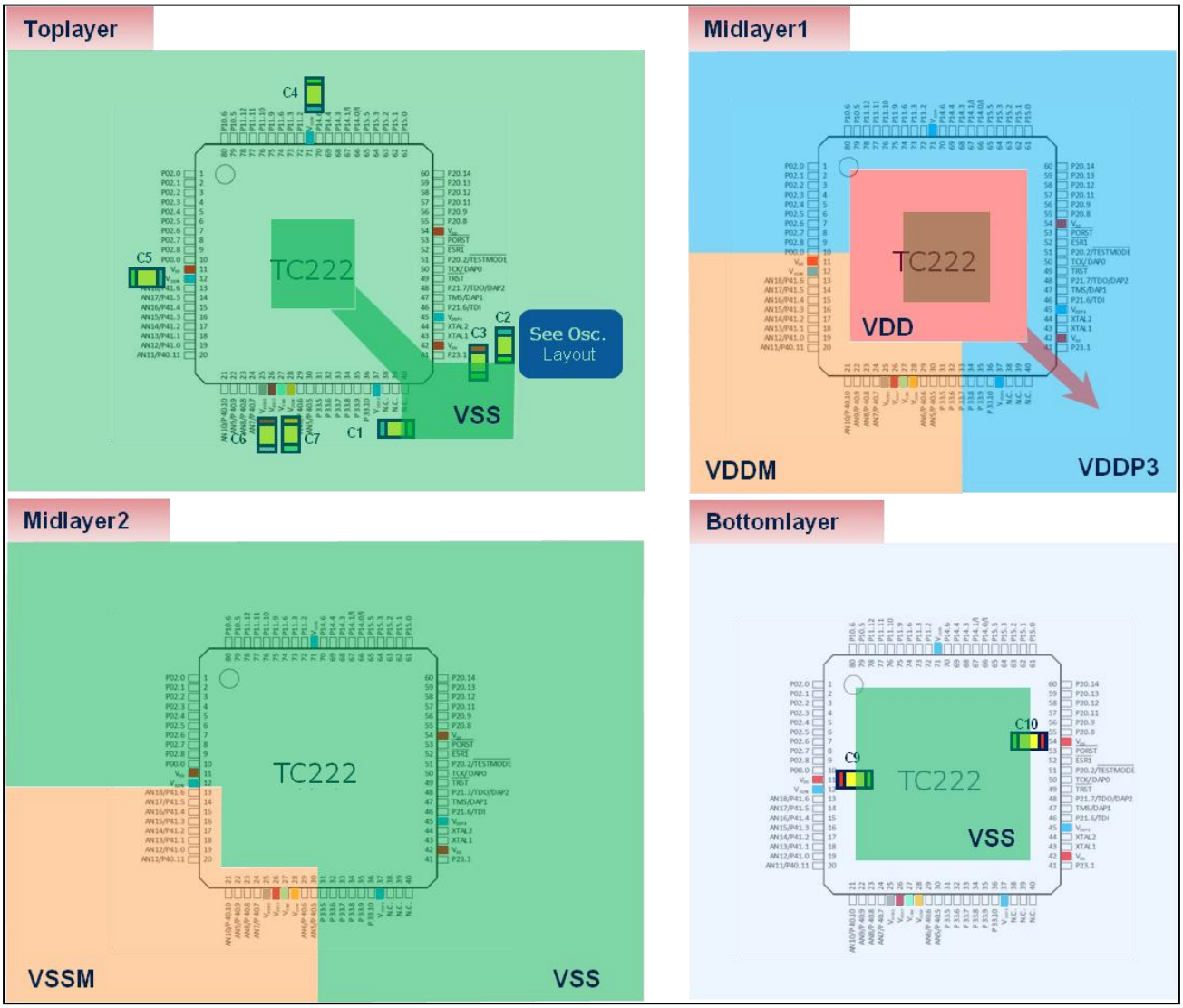

Figure 9 TQFP-80 Package

Table 2 Decoupling Capacitor List for TQFP-80 Package

Capacitor	Value	Supply	TQFP-80 Pin
C9,C10	2 x 100nF	VDD	54, 11
C3	1x 100nF for external supply mode 1x 2.2uF for LDO mode	VDD	42
C4,C5	2 x 100nF	VDDP3	71, 12
C1	1 x 100nF	VDDP3	37
C2	1 x 330nF	VDDP3	45
C6	1 x 100nF	VAREF//VAGND	26//25
C7	1 x 100nF	VDDM//VSSM	28//27

4.2 Example Layout for TQFP-100 Package

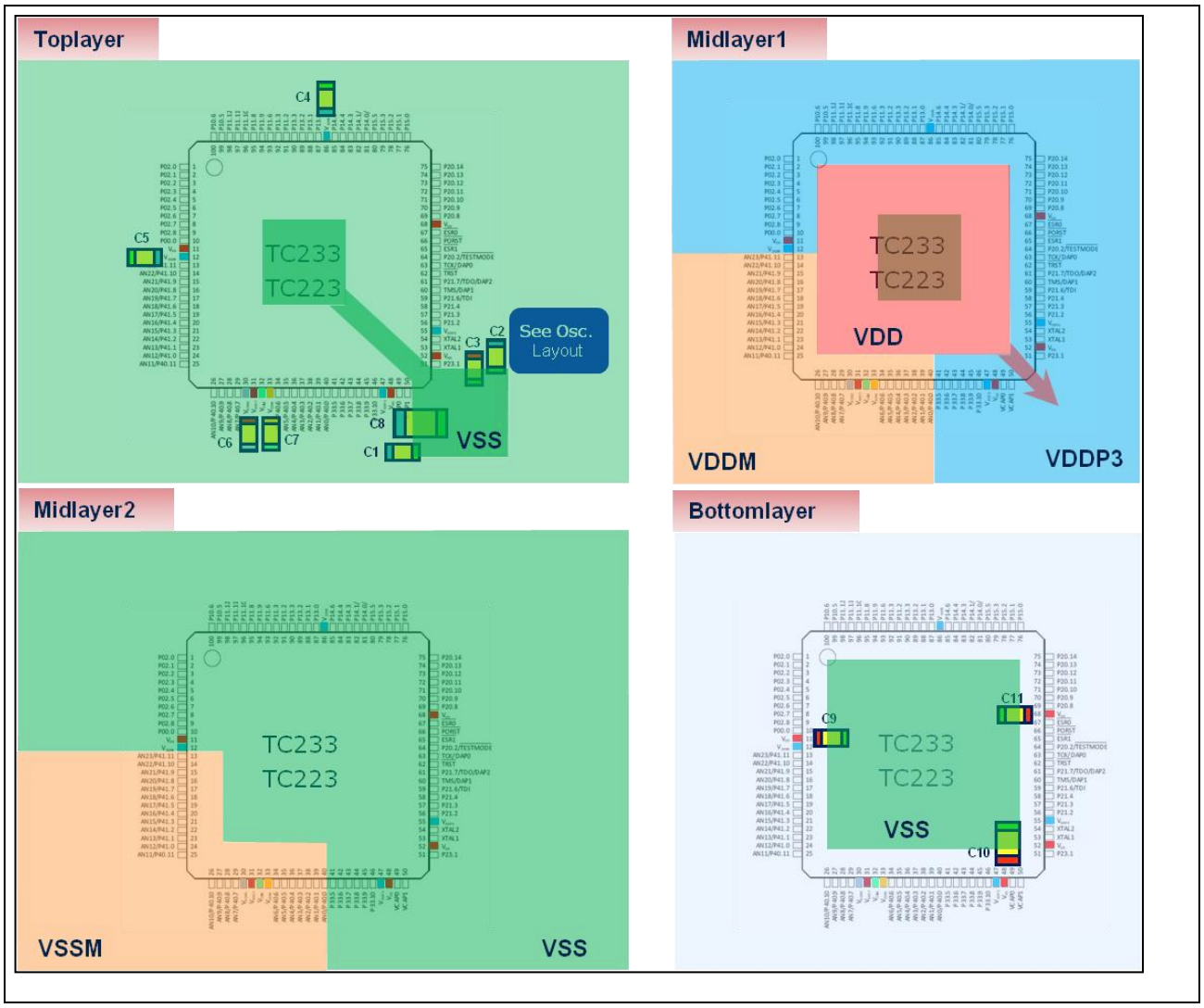

Figure 10 TQFP-100 Package

Table 3 Decoupling Capacitor List for TQFP-100 Package

Capacitor	Value	Supply	TQFP-100 Pin
C9,C11	2 x 100nF	VDD	11,68
C3	1 x 100nF for TC223 in external supply mode 1 x 2.2uF for TC223 in LDO mode	VDD	52
C10	1 x 100nF for TC233 in external supply mode 1 x 2.2uF for TC233 in LDO mode 1 x 10uF for TC233 in SMPS mode	VDD	48
C2	1 x 330nF	VDDP3	55
C4,C5	2 x 100nF	VDDP3	86, 12
C1	1 x 100nF for external supply mode 1 x 4.7uF for SMPS mode	VDDP3	47
C6	1 x 100nF	VAREF//VAGND	31//30
C7	1 x 100nF	VDDM//VSSM	33//32

C8	1 x 1uF only for TC233 in SMPS mode	VCAP0-VCAP1	49,50

4.3 Example Layout for TQFP-144 Package

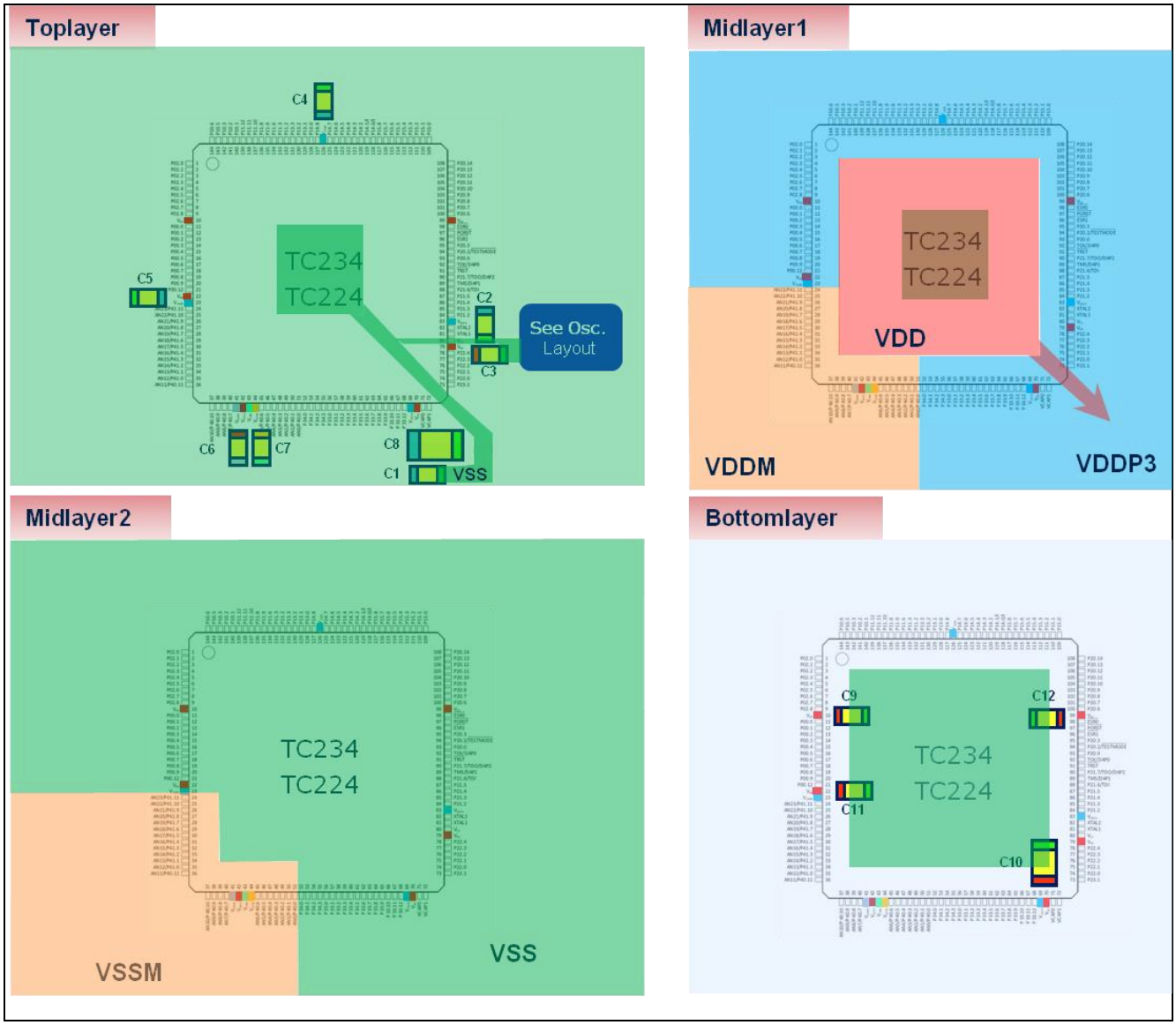

Figure 11 TQFP-144 Package

Table 4 Decoupling Capacitor List for TQFP-144 Package

Capacitor	Value	Supply	TQFP-144 Pin
C12,C9,C11	3 x 100nF	VDD	99, 10 (VDDSB for ADAS Device), 22
C3	1 x 2.2µF for TC224 with LDO mode 1 x 100nF for all other cases	VDD	79
C10	1 x 100nF for TC234 for external supply mode 1 x 2.2uF for TC234 for LDO mode 1 x 10uF for TC234 for SMPS mode	VDD	70
C2	1 x 330nF	VDDP3	83
C1	1 x 4.7uF for TC234 in SMPS mode 1 x 100nF for all other cases	VDDP3	69
C4,C5	2 x 100nF	VDDP3	126, 23
C8	1 x 1uF for TC234 in SMPS mode No cap required for all other cases	VCAP0-VCAP1	71//72
C6	1 x 100nF	VAREF//VAGND	41//42
C7	1 x 100nF	VDDM //VSSM	44//43

4.4 Example Layout for LFBGA-292 Package

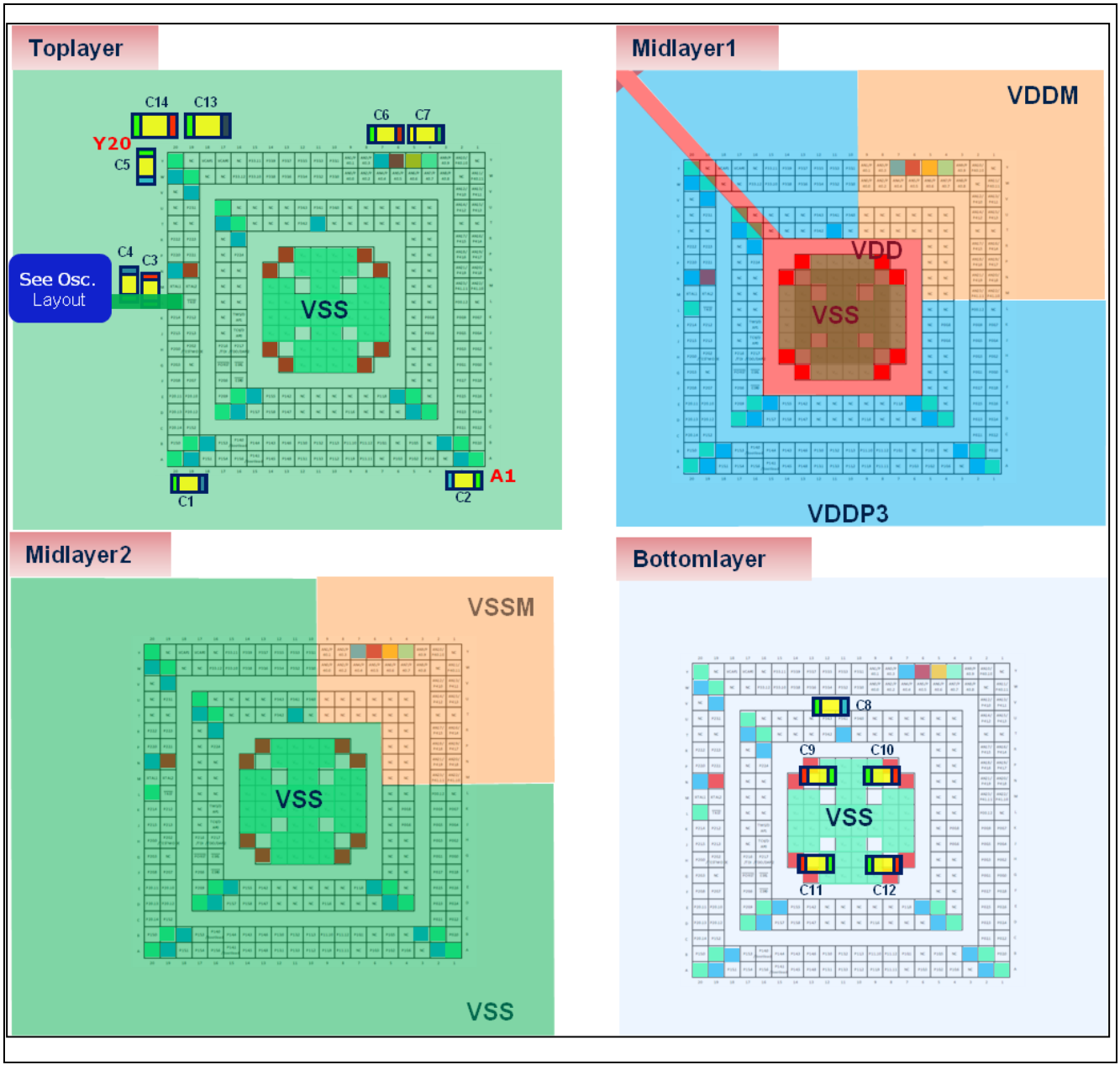

Figure 12 LFBGA-292 Package

Table 5 Decoupling Capacitor List for LFBGA-292 Package

Capacitor	Value	Supply	LFBGA-292 Pin
C3,C9, C10,C11,C12	5 x 100nF	VDD	N19//L20, N14+P13//M13+N12, N7+P8//M8+N9, G8+H7//J8+H9, G13+H14//H12+J14
C14	1 x 2.2uF for LDO mode 1 x 10uF for SMPS mode	VDD	VDD Plane
C4	1 x 330nF	VDDP3	N20//L20
C1	1 x 100nF	VDDP3	A19//A20, B18//B19, D16//D17, E15//E16
C2	1 x 100nF	VDDP3	A2//B2, B3//B2, D5//D4
C5	1 x 100nF for external supply mode 1 x 4.7uF for SMPS mode	VDDP3	W20// Y20, V19//W19
C8	1 x 100nF	VDDP3	T11//P11
C7	1 x 100nF	VDDM / VSSM	Y5//Y4
C6	1 x 100nF	VAREF / VAGND	Y6//Y7
C13	1 x 1uF only for SMPS mode	VCAP0 /VCAP1	Y17//Y18

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