Never stop thinking

TC1784

AP32161

Design Guideline for TC1784 Microcontroller Board Layout

Application Note

V1.2 2012-02

Microcontrollers

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Device1

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Page	Subjects (major changes since last revision)
10	Figure 4 update.

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1 Overview

The TC1784 is a 32-Bit microcontroller in BGA-292 pin package, which requires a carefully designed PCB concerning electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for TC1784 are discussed here.

1.1 General Informations:

The microcontroller has three supply domains (VDD = 1.3V for Core, VDDP = 3.3V for I/O Pad, VDDM = 3.3V or 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1784

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	N.C.2	P10.9	P10.8	P10.6	P10.4	Vssp	P2.12 SSC	P2.11 SSC	P6.2	P6.0	Vssp	P0.12 ERAY	P0.10 ERAY	P0.8 ERAY	P3.13 CAN	P3.15 CAN	P3.4 SSC	P3.2 SSC	P3.8	Vssp
B	Vddp	Vssp	P10.7	P10.5	P10.3	Vddp	P0.15	P2.10 SSC	P6.3	P6.1	Vddp	P0.13 ERAY	P0.11 ERAY	P0.9 ERAY	P3.12 CAN	P3.14 CAN	P3.7	P3.3 SSC	Vssp	Vddp
C	P10.10	Vddp																	Vddp	P3.6
D	P5.0	P10.11		Vssp	P10.2	P10.0	P0.14	P0.6	P2.13	P2.9	P0.2	P0.1	Vddfl3	Vddfl3	P3.0 ASC	P3.1 ASC	Vssp		P3.5	ESR0
E	P5.5 SSC	P5.1		P10.12	Vssp	P10.1	P0.7	P0.5	P0.4	P2.8	P0.3	P0.0	P3.11	P3.9	P3.10	Vssp	P1.1		ESR1	PORST
F	P5.6 SSC	P5.7 SSC		P5.2	P10.13											P1.15	P1.0		TEST MODE	TCK
G	Vssp	Vddp		P9.0 CAN	P5.3			Vdd	Vss	Vss	Vss	Vss	Vdd			P1.6	P1.7		TRST	TDO
H	P5.15 MLI	P5.8 MLI		P9.1 CAN	P5.4		Vdd		Vss	Vss	Vss	Vss		Vdd		P1.5	TMS		TDI	Vddosc
J	P5.10 MLI	P5.9 MLI		P9.3	P9.2		Vss	Vss		Vss	Vss		Vss	Vss		P1.4	Vddpf3		XTAL2	XTAL1
K	P5.12 MLI	P5.11 MLI		P9.4	P9.5		Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss		P1.3	Vddpf		Vddosc	Vssosc
L	P5.14 MLI	P5.13 MLI		P9.6	P9.7		Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss		P1.10	P1.8 SSC		P1.9 SSC	P1.11 SSC
M	Vssp	Vddp		N.C.3	N.C.4		Vss	Vss		Vss	Vss		Vss	Vss		P1.2	P8.14 EBU		Vddp	Vssp
N	Vddmf	Vdda		vfaref	vfagnd		Vdd		Vss	Vss	Vss	Vss		Vdd		P8.13 EBU	P8.12 EBU		P8.11 EBU	P8.4 EBU
P	AN35	Vssa		AN34	AN33			Vdd	Vss	Vss	Vss	Vss	Vdd			P8.10 EBU	P8.9 EBU		P8.8 EBU	P8.7 EBU
R	AN32	AN31		AN30	AN29											Vdd	P7.2 EBU		P8.6 EBU	P8.5 EBU
T	AN28	AN7		AN25	AN24	vagnd0	varef1	AN6	AN2	P1.12 ADC	P2.3 MLI	P2.7 MLI	P4.0	P7.4 EBU	P7.7 EBU	Vss	Vdd		P8.2 EBU	P8.3 EBU
U	AN27	AN26		AN21	AN15	varef0	AN8	AN3	P1.14 ADC	P1.13 ADC	P2.2 MLI	P2.6 MLI	P4.1	P7.3 EBU	P7.8 EBU	P7.0 EBU	Vss		P8.0 EBU	P8.1 EBU
V	AN23	AN22																	Vdd	P7.15 EBU
W	AN20	AN14	AN16	AN18	AN17	AN19	Vssm	AN5	AN1	Vddp	P2.1 MLI	P2.5 MLI	P4.2 EXCLK	P7.6 EBU	P7.9 EBU	Vddp	P7.11 EBU	P7.13 EBU	Vss	Vdd
Y	N.C.1	AN13	AN12	AN11	AN10	AN9	Vddm	AN4	AN0	Vssp	P2.0 MLI	P2.4 MLI	P4.3 EXCLK	P7.1 EBU	P7.5 EBU	Vssp	P7.10 EBU	P7.12 EBU	P7.14 EBU	Vss

Figure 1 Pinout of TC1784 (BGA-292):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - SYSCLK: System clock output
  - Supply pins

  Route these signals with adjacent ground reference and avoid signal and reference layer changes.

  Route them as short as possible.

  Routing ground on each side can help to reduce coupling to other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points must be considered:

1. Supply Pins (Modules) :	• See the User´s Manual.
2. I/O-Pins:	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins :	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device:	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device:	• For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground must be separated into two groups:

    1. Ground for OSC and PLL (VSSOSC for VDDOSC and VDDOSC3) as common star point.
    2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.

PCB Design Recommendations

- To reduce the radiation / coupling from oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Xtal should be as short as possible.
- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDM, VDDMF, VDDAF, VDDPF and VDDPF3. Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net. (See Figure 2).
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32146).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

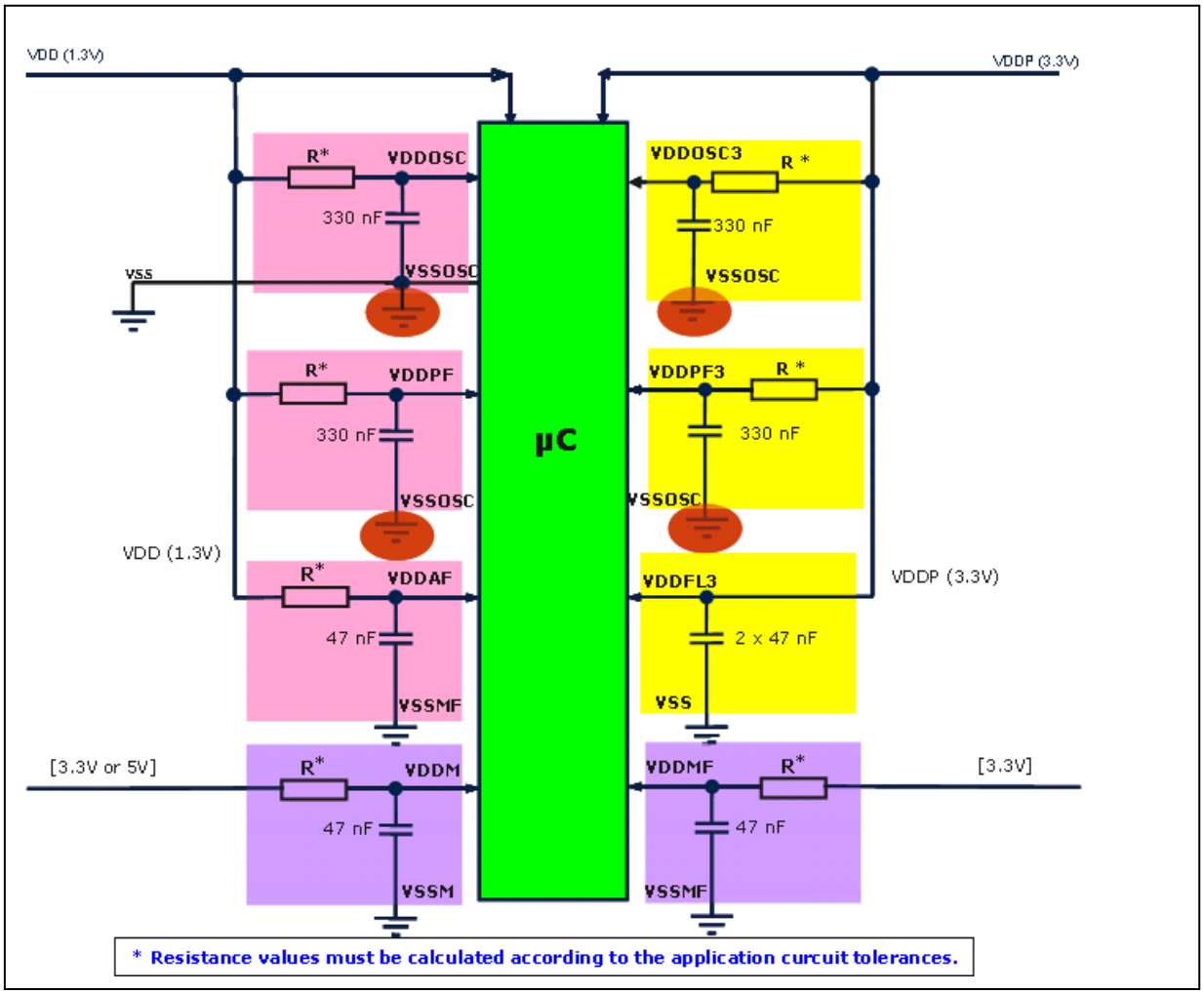

Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDM, VDDMF, VDDAF,VDDPF, VDDPF3 supply pins

2.1 Decoupling

- The two supply domains VDD and VDDP of TC1784 should be decoupled separately. Figure 3 shows an example placement of decoupling capacitors. The decoupling capacitors for VDDC domain should be referenced to the GND area of center pad area in order to get a smaller current loop. The remaining decoupling capacitors for VDDP should be referenced to GND-Balls of the package. (See decoupling layout example in Figure 3).
- If it is required to reduce the count of the capacitors, 100nF can be used instead of 47nF for the pins where two capacitors are connected (see capacitor list on page 11). The total value of decoupling capacitors for the supply domains shall not below 600nF for VDD and 800nF for VDDP.
- Type of capacitors:
  - Values: 47 nF (or 100 nF), 330 nF
  - X7R Ceramic Multilayer (Low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

A power-plane/grounding concept example for a 32-bit microcontroller like TC1784 with BGA-292 package can be seen in Figure 3. Alternative implementations are also acceptable and must be evaluated within application by customer.

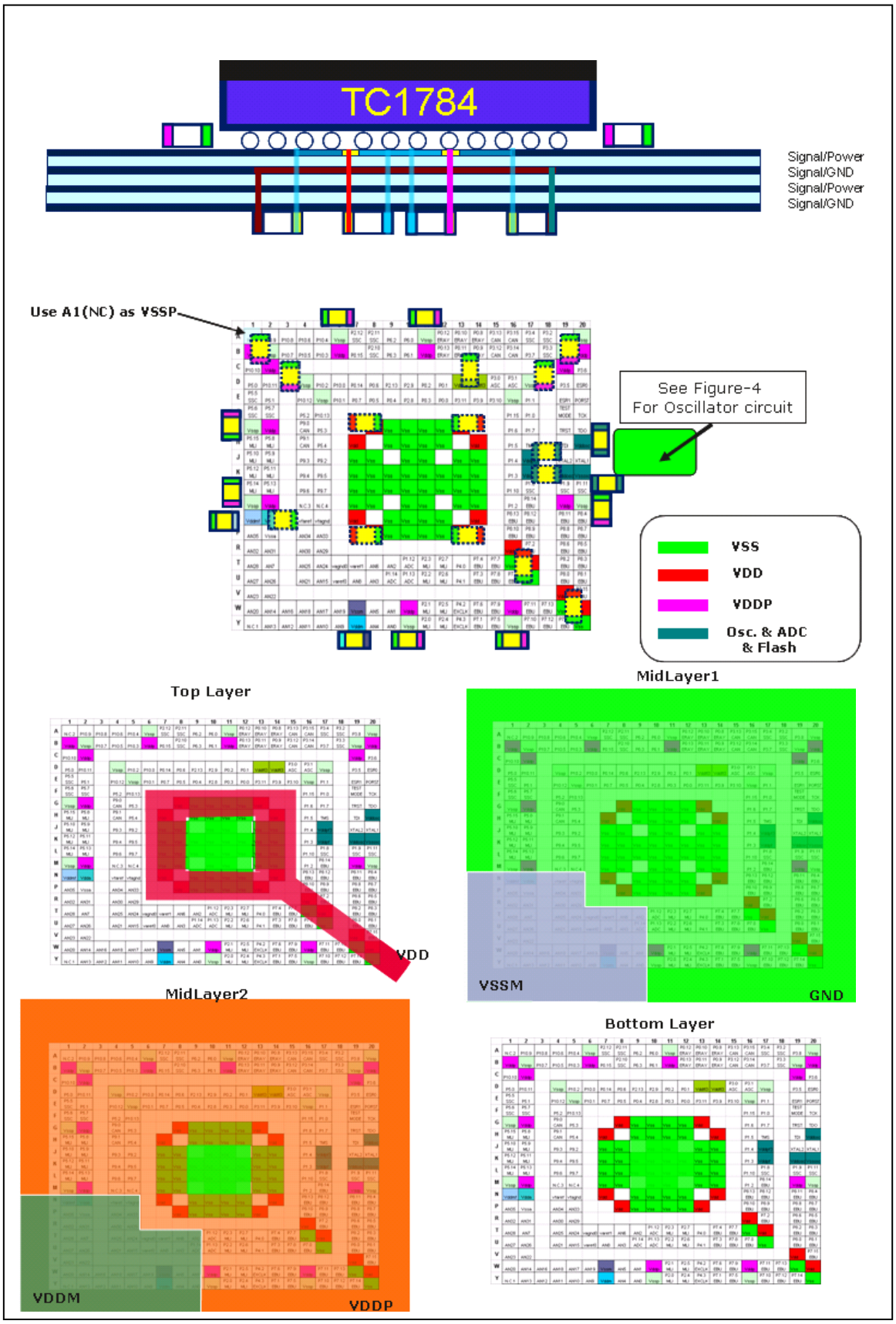

Figure 3 Layout example for decoupling of TC1784 (BGA-292)

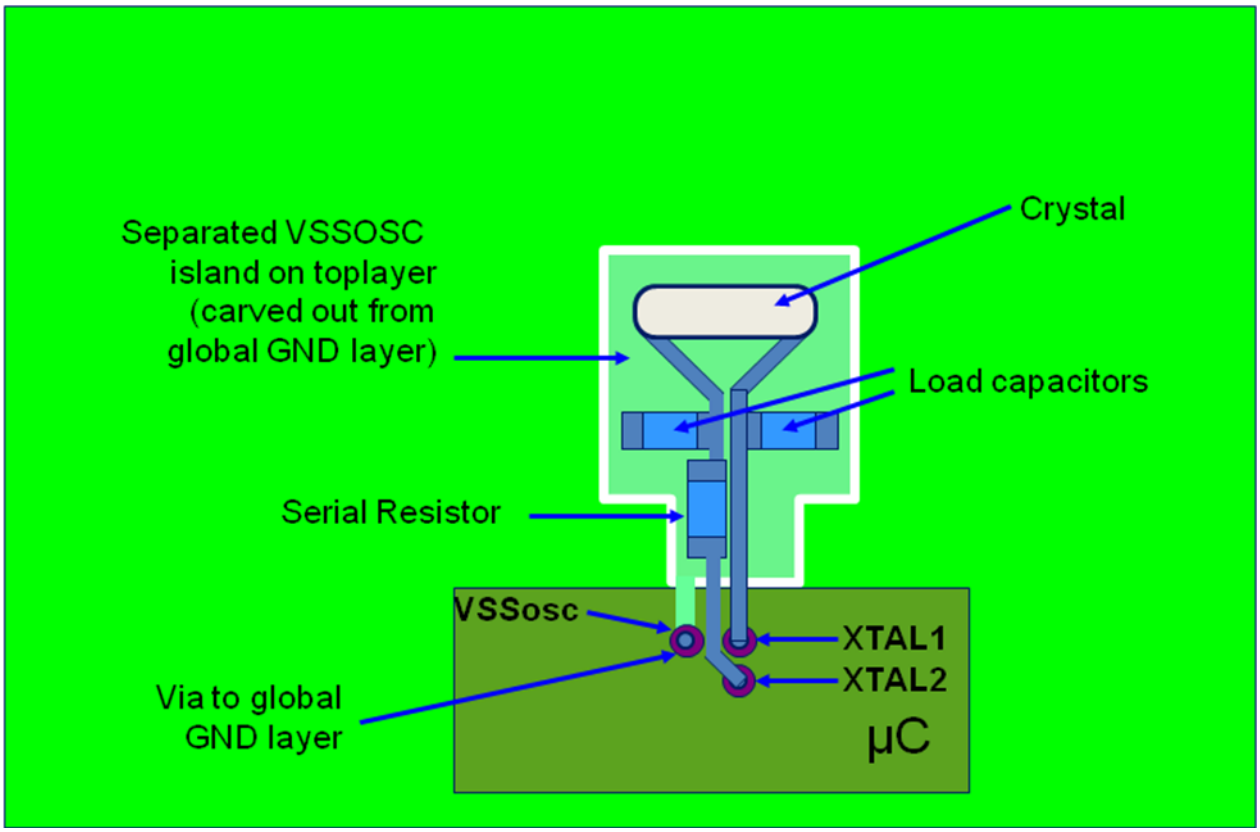

Figure 4 Layout proposal oscillator circuit

2.2 Decoupling Capacitor List:

Number	Capacitor	Supply	Pins(BGA-292)	Comments
C1	47nF	VDDP	W16	
C2	47nF	VDDP	W10	
C3	47nF	VDDP	M2	
C4	47nF	VDDP	G2	
C5	47nF	VDDP	B6	
C6	47nF	VDDP	B1	1x100nF can be used for C6 & C6-1
C6-1	47nF	VDDP	C2	
C7	47nF	VDDP	C19	1x100nF can be used for C7 & C7-1
C7-1	47nF	VDDP	B20	
C8	47nF	VDDP	B11	
C8-1	47nF	VDDP	M19	
C9	47nF	VDD	H7	1x100nF can be used for C9 & C9-1
C9-1	47nF	VDD	G8	
C10	47nF	VDD	H14	1x100nF can be used for C10 & C10-1
C10-1	47nF	VDD	G13	
C11	47nF	VDD	P8	1x100nF can be used for C11 & C11-1
C11-1	47nF	VDD	N7	
C12	47nF	VDD	P13	1x100nF can be used for C12 & C12-1
C12-1	47nF	VDD	N14	
C13	47nF	VDD	T14	1x100nF can be used for C13 & C13-1
C13-1	47nF	VDD	R16	
C14	47nF	VDD	W20	1x100nF can be used for C14 & C14-1
C14-1	47nF	VDD	V19	
C15	47nF	VDDFL3	D13	1x100nF can be used for C15 & C15-1
C15-1	47nF	VDDFL3	D14	
C16	330 nF	VDDOSC	K19	
C17	330 nF	VDDOSC3	H20	
C18	47 nF	VDDAF	N2	
C19	47 nF	VDDMF	N1	
C20	47 nF	VDDM	Y7	
C21	330nF	VDDPF	K17	
C22	330nF	VDDPF3	J17	

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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