Design guideline for XC2000 and XE16x Microcontroller board layout

XC2000 and XE16x family of products

XC2331D, XC2234L, XC2733X, XC2230L, XC2330D, XE162FL, XE162HL, XC2220L, XC2224L, XC2320D, XC2321D, XC2723X, XE161FL, XE161HL, XC2320S, XC2722X, XC2220U, XE161FU, XC2310S, XC2712X, XC2210U, XE160FU

About this document

Scope and purpose

The XC2000 and XE16x families are a 32-/16-Bit microcontroller family in QFP-64, VQFN-48 and TSSOP-38 pin packages. These require a PCB carefully designed for electromagnetic compatibility and power supply system (Exposed Pad connection on the center of the package).

This document provides some product-specific recommendations and guidelines for the XC2000 and XE16x families, and should be read in conjunction with the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design.

Intended audience

Engineers implementing design solutions incorporating the XC2000 and XE16x products.

Table of Contents

1 Overview

The microcontroller has one supply domain VDDPB for the range 3.3 V – 5.0 V, which should be decoupled with capacitors. There is another one core supply domain (VDDIM), which can be generated by the on-chip voltage regulator or can be fed externally. For the discussion in this document it is assumed that on-chip voltage regulators deliver these voltages. Even though the voltage is generated on chip, it should be decoupled with external decaps on the application board. Special care should be given to the decap connections for VDDIM pins.

1.1 Pinout of XC2000 and XE16x

Note: These pinouts apply to both the XC2000 and XE166 families.

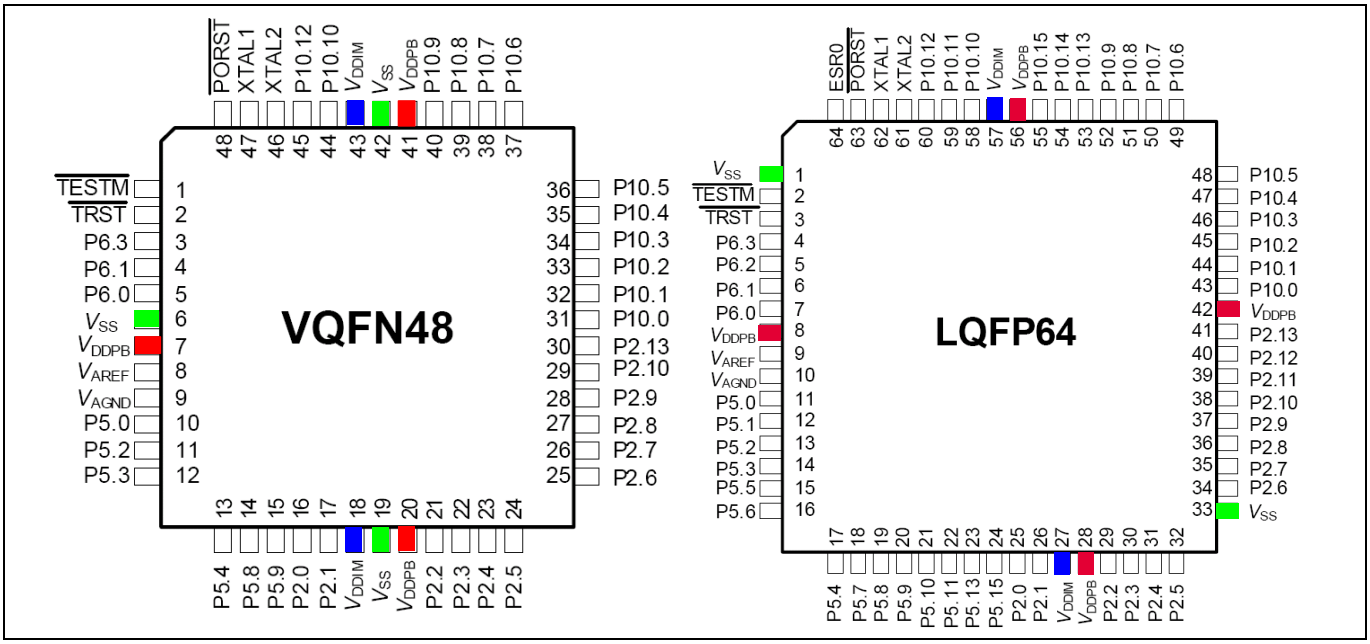

Figure 1 Pinout of XC2000 (64 and 48 pin packages)

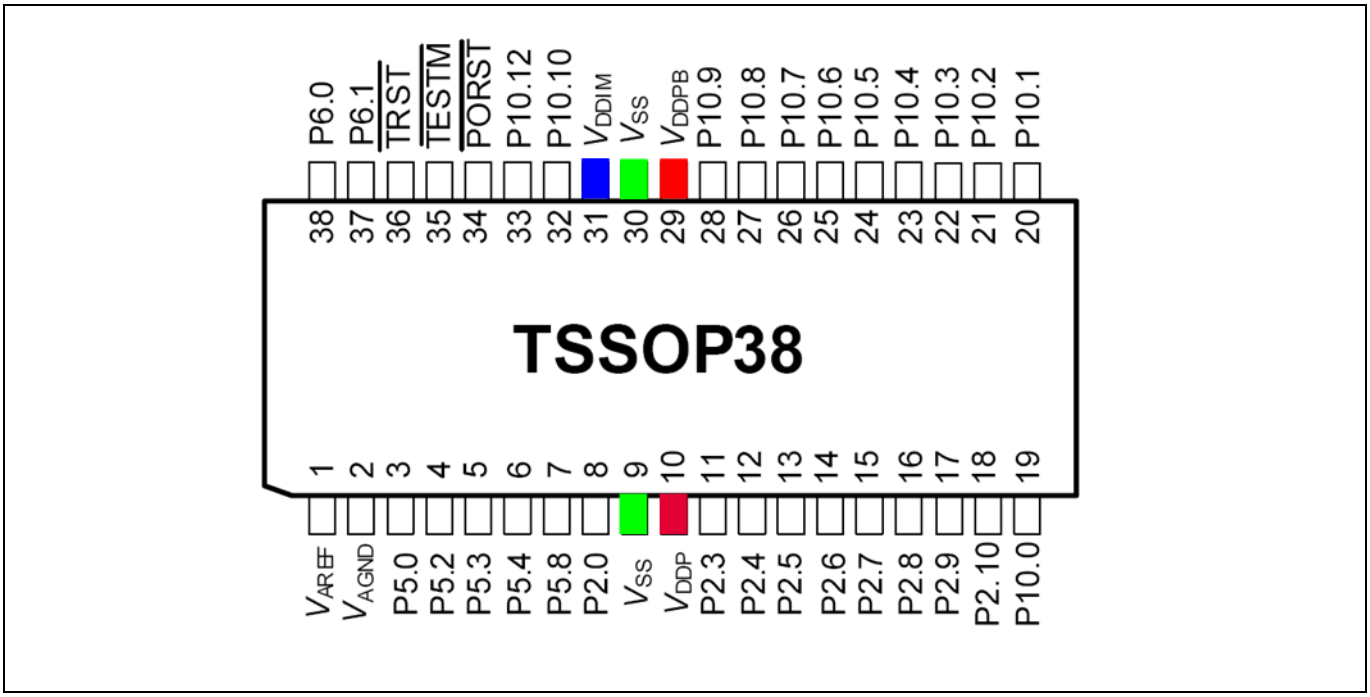

Figure 2 Pinout of XC2000 & XE16x (TSSOP-38 pin package)

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - P2.8 / System clock output (use reduced driver mode if possible)
  - Supply pins (for SYSCLK specially VDDIM)

Note the following:

  - Route these signals with adjacent ground reference and avoid signal and reference layer changes.
  - Route them as short as possible.
  - Routing ground on each side can help to reduce coupling to the other signals.

- For unused “Output, Supply, Input and I/O“ pins following points must be considered:

1. Supply Pins (Modules)	• See the Users´s Manual.
2. I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4. Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg). • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current)
5. Input Pins with internal pull device	• For pins with alternate function see product specification to define the necessary logic level. • Should be configured as Pull-down (exception: if the Users´s Manual requires high level for alternate functions). • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering).
6. External oscillator pins	• For the use case of internal oscillator, connect XTAL1 with pull-down or directly to GND, leave XTAL2 open.

- The ground system must be designed as follows:
  - Separate analog and digital grounds.
  - The analog ground must be separated into two groups:
    - Ground for OSC (GND Island)
    - Ground for ADC (VAGND)
- To reduce the radiation / coupling from oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load

capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Crystal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- A low inductance value for the connection of decoupling capacitors to the supply pins is required.
- Inductance/ferrite beads in the range L ~5-10µH should be inserted in the supply paths at the regulator output.
- Select weakest possible driver strengths and slew rates for all I/Os.
- Use lowest possible frequency for the SYSCLK driver.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.
- Depending on power dissipation (refer to the Data Sheet) the exposed pad must be connected to sufficient GND area on both layers.

2.1 Decoupling

- All supply domains of XC2000 & XE16x should be decoupled separately (see decoupling layout examples in Figures 3, 4, and 5).
- Type of capacitors:
  - Values: 100 nF, 470 nF, 1 µF, 2.2 µF
  - X7R Ceramic Multilayer (Low ESR and low ESL)
- All power pins (supplied from Voltage Regulator) should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer (see layout examples).
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC (single side placement).
- Multiple vias can be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

A power-plane/grounding concept example for the XC2000 & XE166 microcontrollers can be seen in Figures 3, 4 and 5.

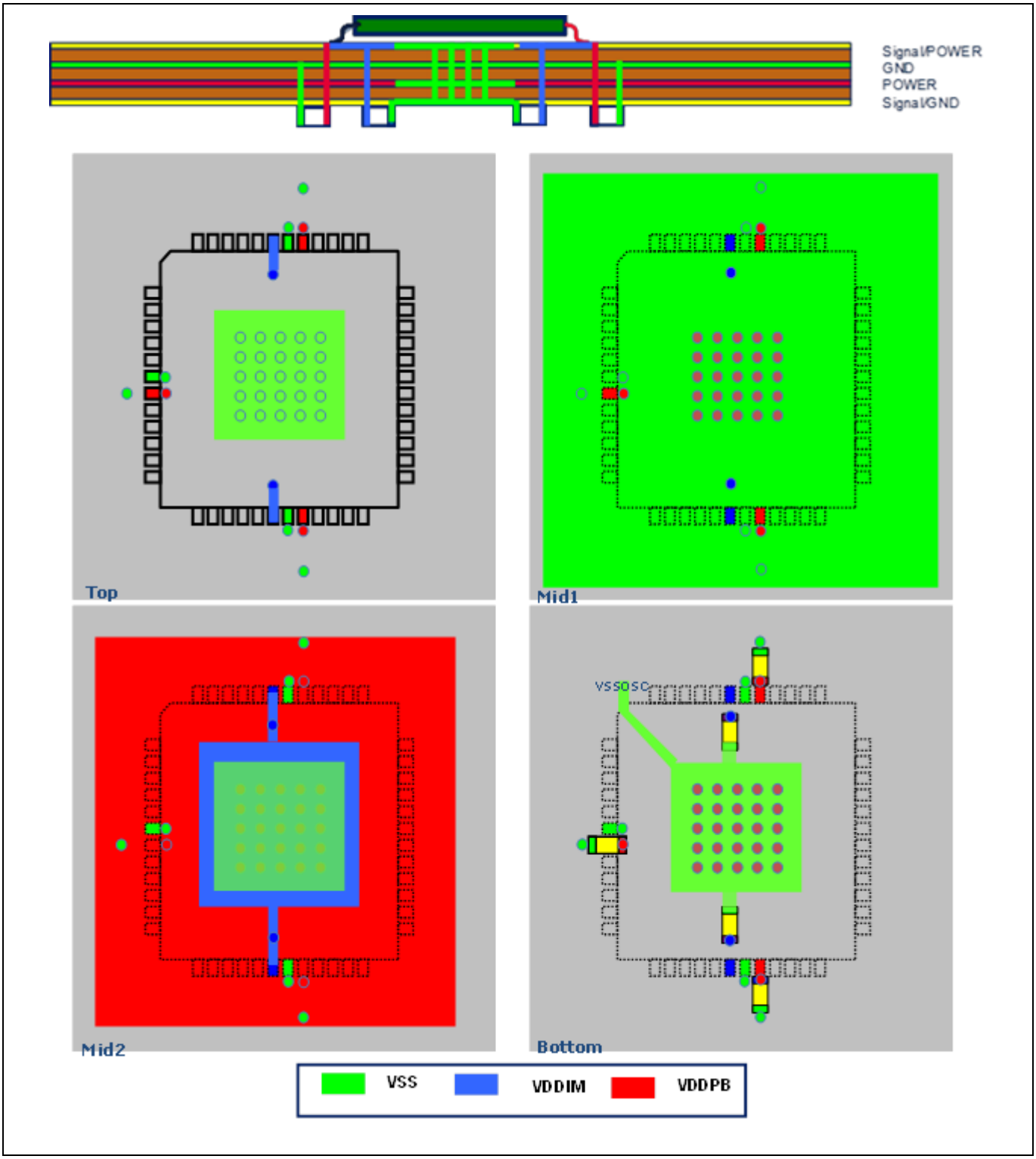

Figure 3 **4-layer PCB layout example for decoupling of XC2000 (VQFN48-pin, double-sided placement)**

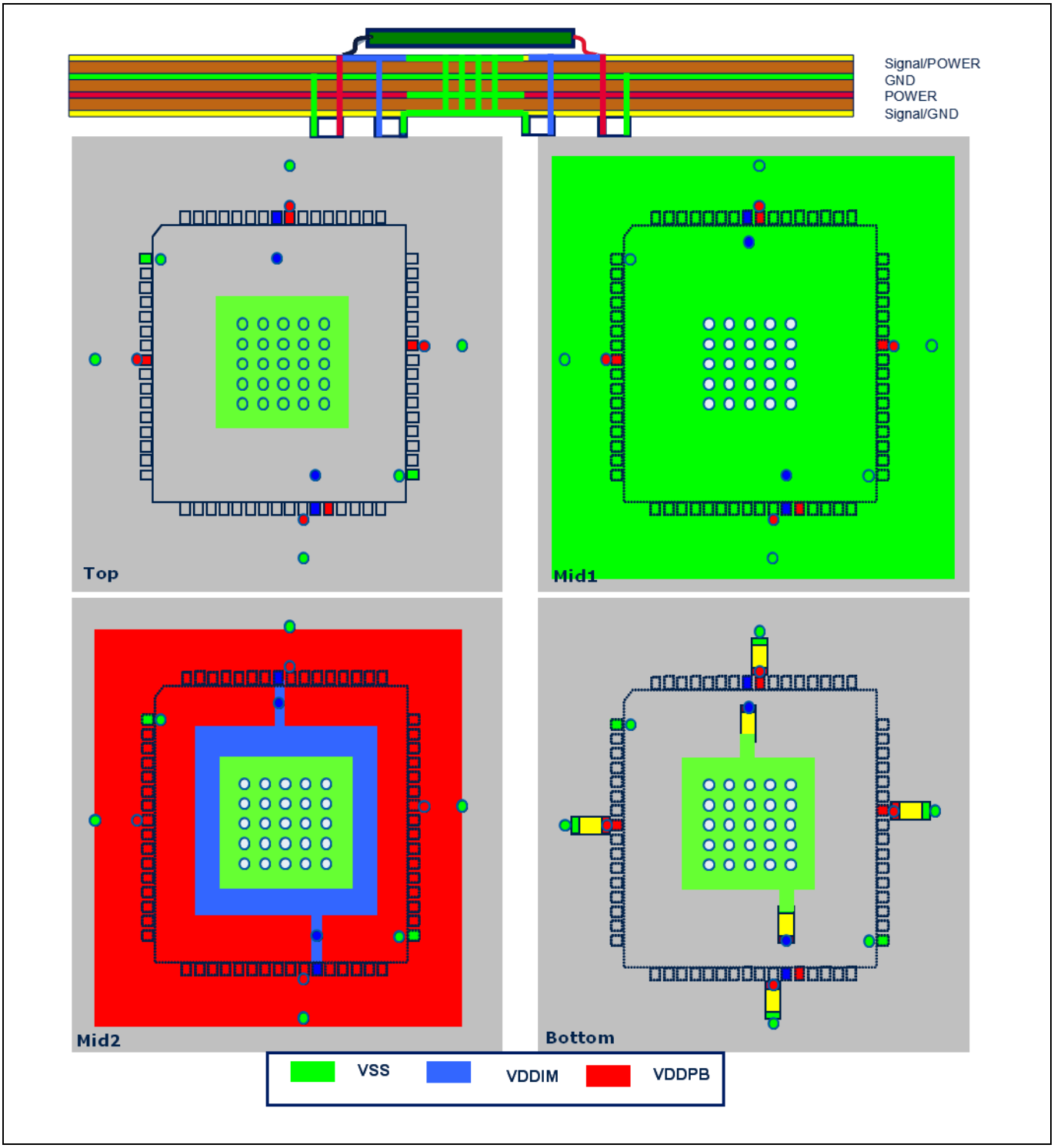

Figure 4 **4-layer PCB layout example for decoupling of XC2000 (QFP64-pin, double-sided placement)**

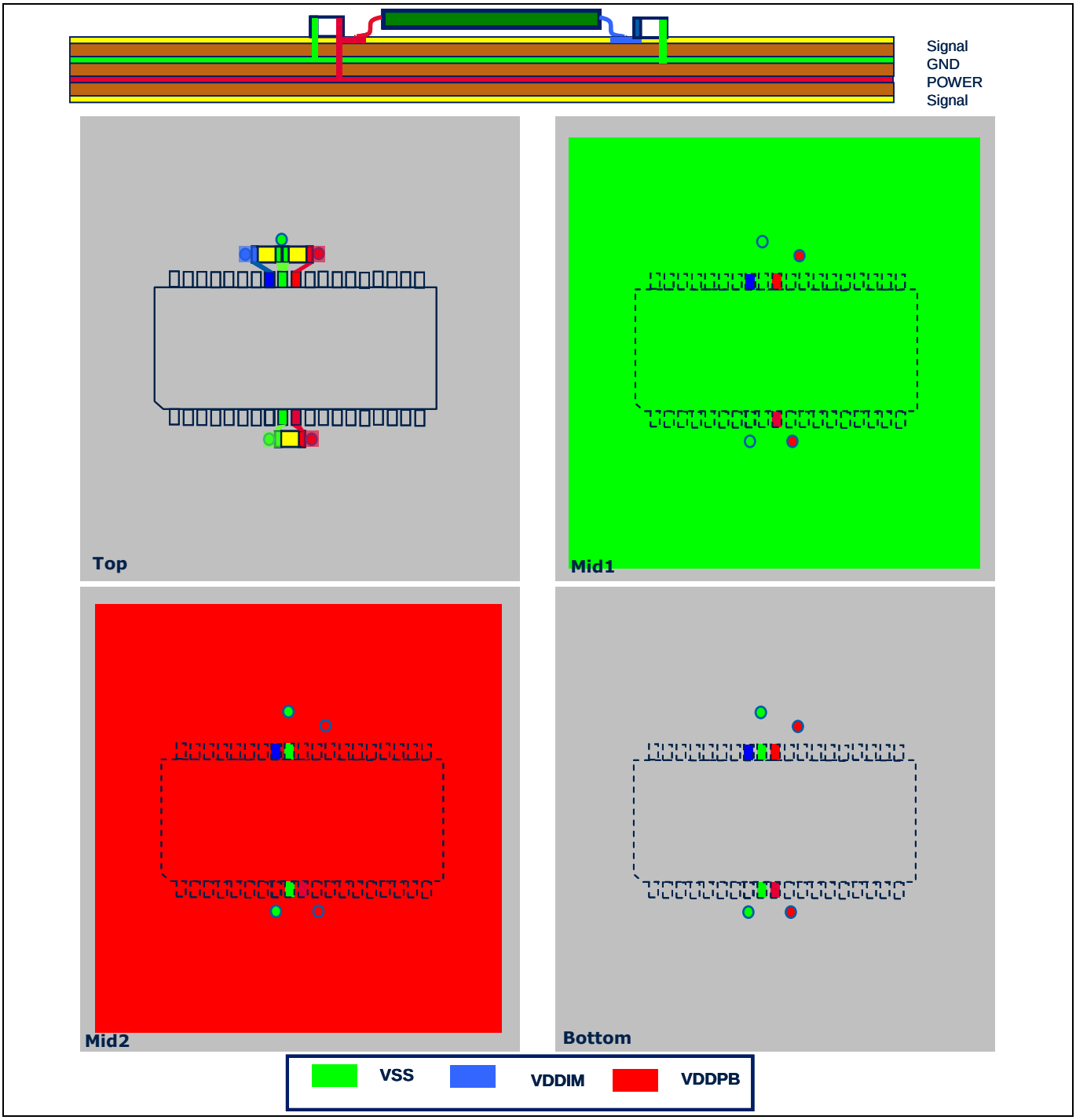

Figure 5 **4-layer PCB layout example for decoupling of XC2000 (TSSOP38-pin, single-sided placement)**

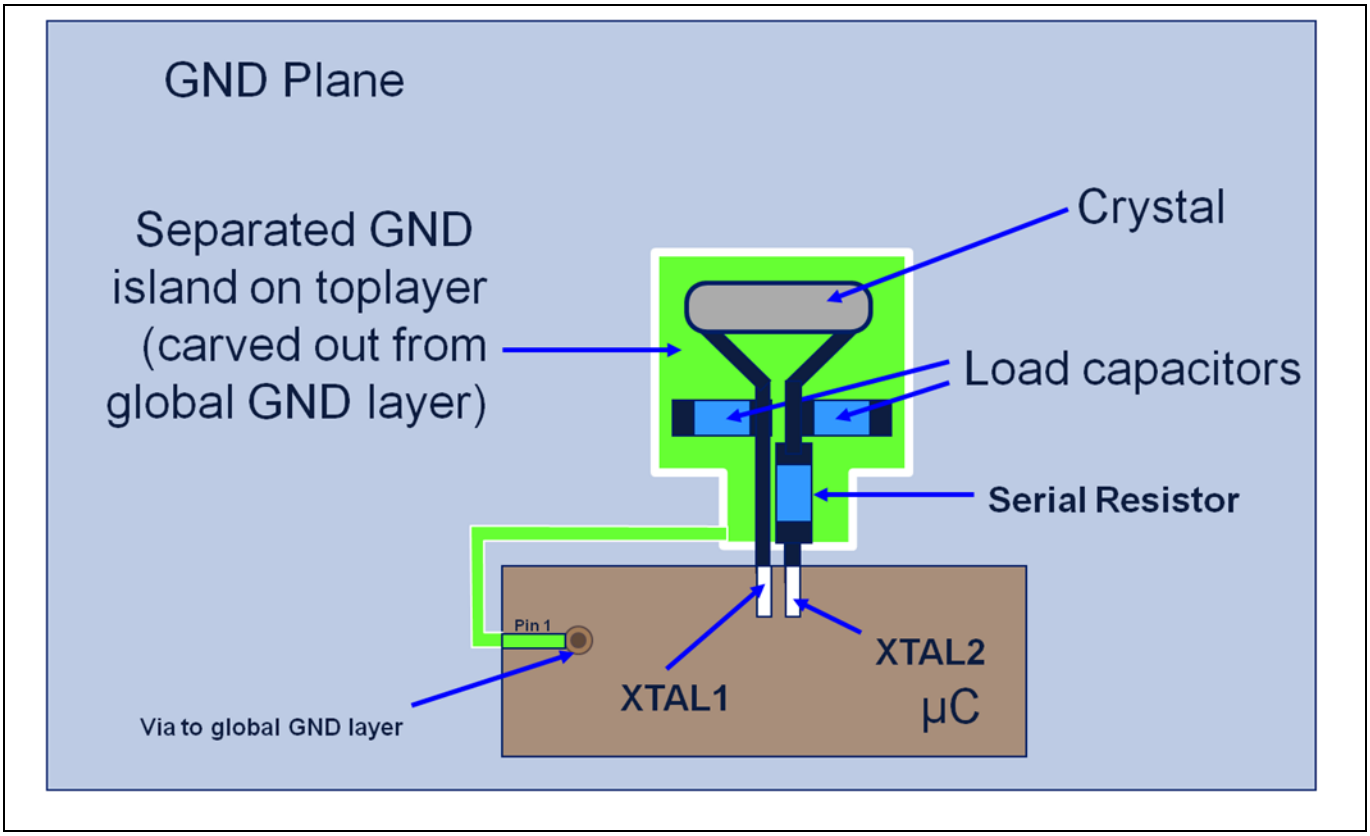

Figure 6 Layout example for oscillator circuit

2.2 Decoupling Capacitor List

Capacitor	Supply	Pins(VQFN-48)	Pins(QFP-64)	Pins (TSSOP-38)
100 nF	VDDPB	7	8	10
100 nF	VDDPB	20	28	29
100 nF	VDDPB	41	42	-
100nF	VDDPB	-	56	-
≥470 nF *	VDDIM	18	27	31**
≥470 nF *	VDDIM	43	57	-

* Total capacitance value on VDDIM must be in range of 2 x 470 nF up to 2 x 2.2 µF.

** Use ≥ 1µF up to 2.2µF.

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices. Other design implementations can also be applied.

Revision History

Major changes since the last revision

Page or Reference	Description of change
9, 10	Figure-3 & 4 updated
9	Figure-3 corrected
All pages	Transferred to latest Infineon template
1	New ‘Scope and Purpose’ (previsouly part of ‘Overview’) New ‘Intended audience’

Edition 2016-07

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AP16185

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.