10W 12 V SMPS Demo Board with ICE3RBR4765JG

AN-DEMO-3RBR4765JG

About this document

Scope and purpose

This document is an engineering report that describes universal input 10 W 12 V off-line flyback converter power supply using Infineon CoolSET™ F3R family, ICE3RBR4765JG (DSO16/12). The converter is operated in Discontinuous Conduction Mode, 65 kHz fixed frequency, low standby power and various mode of protections for a high reliable system. This demo board is designed to evaluate the performance of ICE3RBR4765JG in ease of use.

Intended audience

This document is intended for power supply design/application engineer, students, etc.) who wish to design low cost and high reliable systems of off-line Switched Mode Power Supply (SMPS) for enclosed adapter, blu-ray/DVD player, set-top box, game console, smart meter, auxiliary power supply of white goods, PC, server, etc.

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1 Abstract

This document is an engineering report of an universal input 10 W 12 V off-line flyback converter power supply utilizing F3R CoolSET™ ICE3RBR4765JG. The application demo board is operated in Discontinuous Conduction Mode (DCM) and is running at 65 kHz fixed switching frequency. It has a single output voltage with secondary side control regulation. It is especially suitable for small power supply such as enclosed adapter, blu-ray/DVD player, set-top box, game console, smart meter or open frame auxiliary power supply of white goods, PC, server, etc. Besides having the basic features of the F3 CoolSET™ such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for serious fault (Vcc over voltage protection, Vcc under voltage protection, over temperature, over-load, open loop and short opto-coupler), it also has the BiCMOS technology design, built-in soft start time, built-in and extendable blanking time, frequency jitter feature with built-in jitter period and external auto-restart enable, etc. The key features of this product are the best-in-class low standby power and the good EMI performance.

2 Demonstrator board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

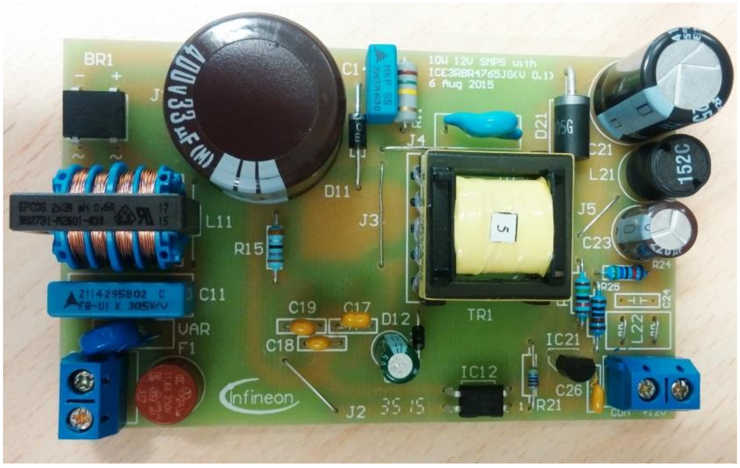


Figure 1 DEMO-3RBR4765JG (Top View)

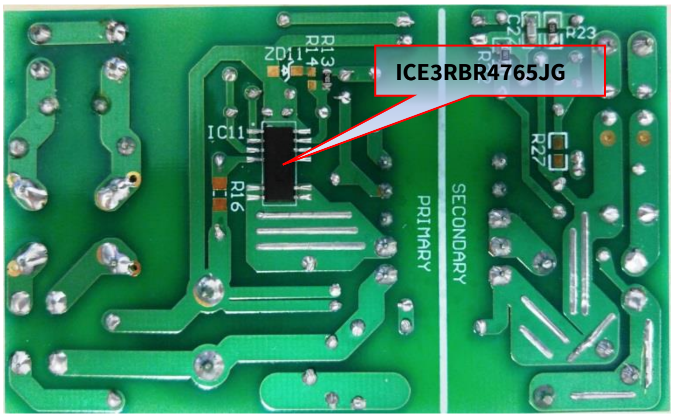


Figure 2 DEMO-3RBR4765JG (Bottom view)

3 Specifications of Demonstrator Board

Table 1 Specifications of DEMO-3RBR4765JG

Input voltage and frequency	85 V_{AC} (60 Hz) ~ 265 V_{AC} (50Hz)
Output voltage, current and power	12 V, 0.83 A, 10 W
Dynamic load response (10% to 100% load, slew rate at 1.5 A/µs, 100 Hz)	±3% of nominal output voltage ($V_{ripple\_p\_p}$< 130 mV)
Output ripple voltage (full load, 85 V_{AC} ~ 265 V_{AC})	±1% of nominal output voltage ($V_{ripple\_p\_p}$< 50 mV)
Active mode four point average efficiency (25%, 50%, 75%, 100% load) (EU CoC Version 5, Tier 1) 10% load efficiency (EU CoC Version 5, Tier 1)	> 84% at 115 V_{AC} and 230 V_{AC} > 74% at 115 V_{AC} and 230 V_{AC}
No load power consumption (EU CoC Version 5, Tier 1)	< 50 mW at 265 V_{AC}
Conducted emissions (EN55022 class B)	Pass with 6 dB margin
ESD immunity (EN61000-4-2)	Level 3 (±8 kV for contact discharge)
Surge immunity (EN61000-4-5)	Installation class 3 (±1 kV for line to line and ±2 kV for line to earth)
Form factor case size (L x W x H)	(90 x 55 x 26) mm^3

4 Circuit description

4.1 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L11, X2-capacitors C11 and Y1-capacitor C15 act as EMI suppressors. Optional spark gap device SG1, SG2 and varistor VAR can absorb high voltage stress during lightning surge test. After the bridge rectifier BR1 and the input bulk capacitor C13, a voltage of 100 to 375 V_{DC} is present which depends on input voltage.

4.2 Start up

Since there is a built-in startup cell in the ICE3RBR4765JG, no external start up resistor is required. The startup cell is connecting the drain pin of the IC. Once the voltage is built up at the drain pin of the ICE3RBR4765JG, the startup cell will charge up the VCC capacitor C16 and C17. When the VCC voltage exceeds the turn on threshold 18 V, the IC starts up. Then the VCC voltage is bootstrapped by the auxiliary winding to sustain the operation.

4.3 Operation mode

During operation, the VCC pin is supplied via a separate transformer winding with associated rectification D12 and buffering C16 and C17.In order not to exceed the maximum voltage at VCC pin due to poor coupling of transformer winding, an external zener diode ZD11 and resistor R14 can be added.

4.4 Soft start

The soft start is a built-in function and is set at 20 ms.

4.5 RCD clamper circuit

While turns off the CoolMOS™, the clamper circuit R11, C14 and D11 absorbs the current caused by transformer leakage inductance once the voltage exceeds designed clamp voltage. Finally drain to source voltage is lower than the maximum break down voltage of CoolMOS™.

4.6 Peak current control of primary current

The CoolMOS™ drain source current is sensed via external shunt resistors R14 and R14A which determine the tolerance of the current limit control. Since ICE3RBR4765JG is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle. Besides, the patented propagation delay compensation is implemented to ensure the maximum input power can be controlled in an even tighter manner. The demo board shows approximately ±0.86% of average maximum input power (Figure 12).

4.7 Output stage

On the secondary side the power is coupled out by a schottky diode D21. The capacitor C21 provides energy buffering following with the LC filter L21 and C23 to reduce the output voltage ripple considerably. Storage capacitor C21 is selected to have an internal resistance as small as possible (ESR) to minimize the output voltage ripple. The optional common mode choke L22 and ceramic capacitor C24 can be added to suppress the high voltage electrostatic static charge during ESD test.

4.8 Feedback and regulation

The output voltage is controlled using a TL431 (IC21). This device incorporates the voltage reference as well as the error amplifier and a driver stage. Compensation network C26, C27, R24, R25, R26 and R27 constitutes the external circuitry of the error amplifier of IC21. This circuitry allows the feedback to be precisely matched to dynamically varying load conditions and provides stable control. The maximum current through the optocoupler diode and the voltage reference is set by using resistors R21 and R22. Optocoupler IC12 is used for floating transmission of the control signal to the "Feedback" input via capacitor C19 of the ICE3RBR4765JG control device. The optocoupler used meets DIN VDE 884 requirements for a wider creepage distance.

4.9 Active burst mode

At light load condition, the SMPS enters into Active Burst Mode. At this start, the controller is always active and thus the VCC must always be kept above the switch off threshold $V_{CCoff} \geq 10.5$ V. During active burst mode, the efficiency increases significantly and at the same time it supports low ripple on V_{OUT} and fast response on load jump. When the voltage level at FB falls below 1.35 V, the internal blanking timer starts to count. When it reaches the built-in 20 ms blanking time, it will enter Active Burst Mode. The Blanking Window is generated to avoid sudden entering of Burst Mode due to load jump.

During Active Burst Mode the current sense voltage limit is reduced from 1.03 V to 0.34 V so as to reduce the conduction losses and audible noise. All the internal circuits are switched off except the reference and bias voltages to reduce the total VCC current consumption to below 450 µA. At burst mode, the FB voltage is changing like a saw tooth between 3 and 3.5 V. To leave Burst Mode, FB voltage must exceed 4 V. It will reset the Active Burst Mode and turn the SMPS into Normal Operating Mode. Maximum current can then be provided to stabilize V_{OUT}.

4.10 Jittering and soft gate drive

In order to reduce the emissions of electromagnetic interference (EMI) due to switching noise, the ICE3RBR4765JG is implemented with frequency jittering and soft gate drive. The jitter frequency is internally set to 65 kHz (± 2.6 kHz) and the jitter period is 4 ms.

4.11 Protection function

Protection is one of the major factors to determine whether the system is safe and robust. Therefore sufficient protection is necessary. ICE3RBR4765JG provides all the necessary protections to ensure the system is operating safely. The protections include VCC over voltage, over load/open loop, VCC under voltage/short optocoupler, over temperature, external protection enable and brownout. When those faults are found, the system will go into auto restart which means the system will stop for a short period of time and restart again. If the fault persists, the system will stop again. It is then until the fault is removed, the system resumes to normal operation. A list of protections and the failure conditions are showed in the below table.

Table 2 Protection function of ICE3RBR4765JG

Protection function	Failure condition	Protection Mode
Vcc Overvoltage	1. V_{VCC} > 20.5 V and FB > 4.0 V & during soft start period 2. V_{VCC} > 25.5 V	Auto Restart
Overtemperature (controller junction)	T_J > 130°C	Auto Restart
Overload / Open loop	V_{FB} > 4.0 V, last for 20 ms and extended blanking time (Extended blanking time counted from charging V_{BA} from 0.9 V to 4.0 V)	Auto Restart
Vcc Undervoltage / Short Optocoupler	V_{VCC} < 10.5 V	Auto Restart
Auto Restart enable	V_{BA} < 0.33 V	Auto Restart

5 Circuit diagram

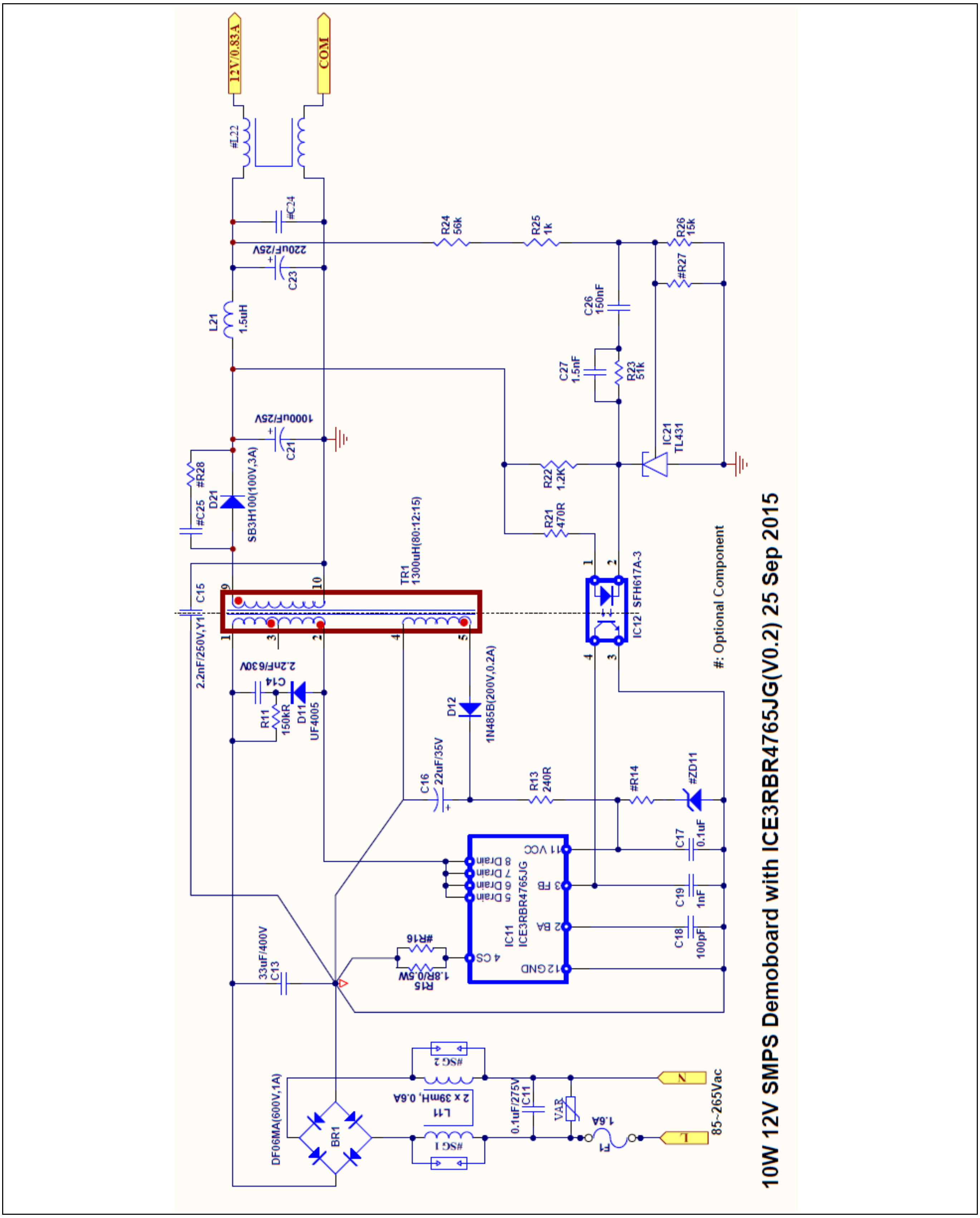


Figure 3 Schematic of DEMO-3RBR4765JG

Note: General guideline for layout design of Printed Cirduit Board (PCB):

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 seperately in one point. It can reduce the switching noise going into the sensitive pins of CoolSET™ device effectively. The primary star ground can be split into five groups as follows,*
    i. *Signal ground includes all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C17, C18, C19 and opto-coupler ground.*
    ii. *VCC ground includes the VCC capacitor ground C16 and the auxiliary winding ground, pin 4 of the power transformer.*
    iii. *Current Sense resistor ground includes current sense resistor R15 and R16.*
    iv. *EMI return ground includes Y capacitor C15.*
    v. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: Filter capacitors, C17, C18 and C19 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High voltage traces clearance: High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.*
    i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm*
    ii. *600V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5 mm*
4. *Recommended minimum 232mm^2 copper area at drain pin to add on PCB for better thermal performance.*
5. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (Pin 1 and 2), IC11 Drain pin, IC11 CS pin and current sense resistor R15/R16) should be as small as possible to minimize the switching emission.*

6 PCB layout

6.1 Top side

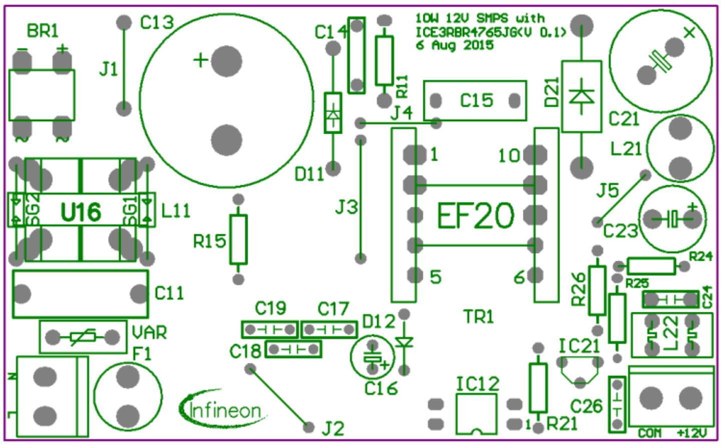


Figure 4 Top side component legend

6.2 Bottom side

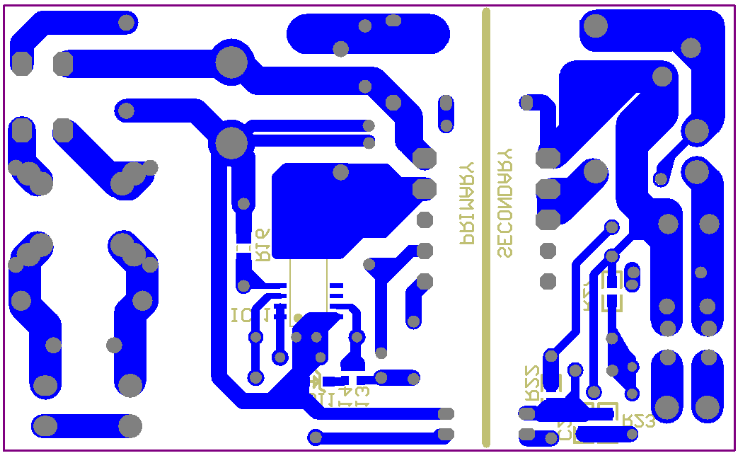


Figure 5 Bottom side copper and component legend

7 Bill of material

Table 3 Bill of material (V0.2)

No.	Designator	Description	Part Number	Manufacturer	Quantity
1	BR1	DF06MA(600 V,1 A)			1
2	C11	0.1 uF/305 V(X1 cap)			1
3	C13	33 uF/400 V			1
4	C14	2.2 nF/630 V	B32560J8222K000	EPCOS	1
5	C15	2.2 nF/250 V(Y1 cap)	DE1E3KX222MA4BL01	MURATA	1
6	C16	22 uF/35 V	B41821A6106M000	EPCOS	1
7	C17	0.1 uF	RPER71H104K2K1A03B	MURATA	1
8	C18	100 pF/50 V			1
9	C19	1 nF/50 V			1
10	C21	1000 uF/25 V			1
11	C23	220 uF/25 V			1
12	C26	150 nF/50 V			1
13	C27	1.5 nF/50 V(SMD0805)			1
14	D11	UF4005(600 V,1 A)	UF4005		1
15	D12	1N485B(200 V,0.2 A)			1
16	D21	SB3H100(100 V,3 A)	SB3H100-E3/54		1
17	F1	1.6 A			1
18	IC11	ICE3RBR4765JG	ICE3RBR4765JG	INFINEON	1
19	IC12	SFH617A-3			1
20	IC21	TL431			1
21	J1,J2,J3,J4,J5,L22	Jumper			6
22	L11	2 x 39 mH, 0.6 A	B82731M2601A030	EPCOS	1
23	L21	1.5 uH			1
24	R11	150 kR/2 W			1
25	R13	240 R(SMD 0805)			1
26	R15	1.8 R(0.5 W,1%)			1
27	R21	470 R			1
28	R22	1.2 k(SMD 0805)			1
29	R23	51 k(SMD 0805)			1
30	R24	56 k			1
31	R25	1 k			1
32	R26	15 k			1
33	TR1	1300 uH(80:12:15) EE20/10/6, TP4A	750342992	Wurth Electronics	1
34	VAR	300 V/0.25 W	B72207S2301K101	EPCOS	1

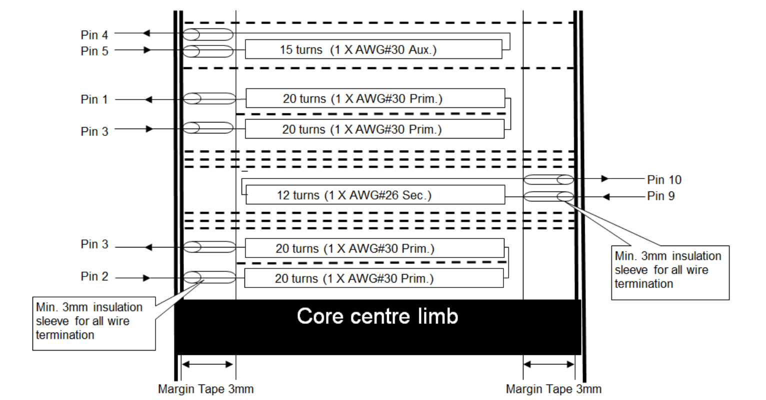
8 Transformer construction

Core and material: EE20/10/6(EF20), TP4A (TDG)

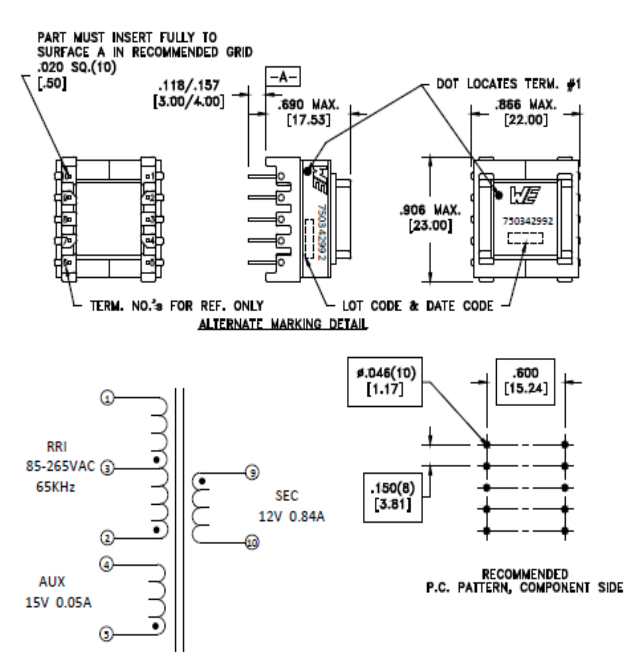
Bobbin: 070-4989(10-Pins, TH-T, Vertical version)

Primary Inductance, LP=1300 µH (±5%), measured between pin 1 and pin 2

Manufacturer and part number: Wurth Electronics Midcom (750342992)



Start	Stop	No. of turns	Wire size	Layer
2	3	40	1XAWG#30	$^1/_2$ Primary
9	10	12	1XAWG#26	Secondary
3	1	40	1XAWG#30	$^1/_2$ Primary
5	4	15	1XAWG#30	Auxiliary



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2-1	@20°C	1.120 ohms max.
D.C. RESISTANCE	5-4	@20°C	0.270 ohms max.
D.C. RESISTANCE	9-10	@20°C	0.080 ohms max.
INDUCTANCE	2-1	50kHz, 100mV, Ls	1300.0µH ±10%
LEAKAGE INDUCTANCE	2-1	tie(4+5+9+10),100kHz, 100mV, Ls	15µH max.
DIELECTRIC	1-10	tie(3+4), 5000VDC, 1 minute	
DIELECTRIC	1-core	tie(3+4), 2500VDC, 1 minute	
DIELECTRIC	10-core	2500VDC, 1 minute	
TURNS RATIO		(2-1):(9-10)	6.67:1, ±2%
TURNS RATIO		(2-1):(5-4)	5.33:1, ±2%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.
Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:
- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, Overvoltage Category II.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tray	Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750342992
ENG	YGD	PKG-0736	Fractions: ±1/64 Footprint: ± .001 [.03]		
REV.	00	CONVENTION PLACEMENT	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		SPECIFICATION SHEET 1 OF 1
DATE	8/14/2015	www.we-online.com/midcom			

Figure 6 Transformer structure

9 Test results

9.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation & output ripple

Input (V_{AC}/Hz)	P_{in} (W)	V_{out} (V_{DC})	I_{out} (A)	V_{out_RPP} (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85 V_{AC}/60 Hz	0.0313	11.93	0.00	31				14.6	1
	1.24	11.93	0.08	36	0.99	79.85			
	2.87	11.93	0.20	9	2.39	83.14	83.70		
	5.83	11.93	0.42	12	4.95	84.92			
	8.84	11.93	0.62	15	7.40	83.67			
	11.92	11.93	0.83	17	9.90	83.07			
115 V_{AC}/60 Hz	0.0320	11.93	0.00	32				14.4	1.01
	1.24	11.93	0.08	37	0.95	76.97			
	2.87	11.93	0.20	9	2.39	83.14	84.53		
	5.78	11.93	0.42	12	4.95	85.66			
	8.72	11.93	0.62	15	7.40	84.82			
	11.72	11.93	0.83	17	9.90	84.49			
230 V_{AC}/50 Hz	0.0444	11.93	0.00	33				14.35	1.02
	1.28	11.93	0.08	40	0.95	74.56			
	2.95	11.93	0.20	9	2.39	80.88	84.08		
	5.82	11.93	0.42	12	4.95	85.07			
	8.70	11.93	0.62	15	7.40	85.02			
	11.60	11.93	0.83	17	9.90	85.36			
265 V_{AC}/50 Hz	0.0459	11.93	0.00	33				14.45	1.02
	1.30	11.93	0.08	40	0.95	73.42			
	3.00	11.93	0.20	10	2.39	79.53	83.47		
	5.86	11.93	0.42	13	4.95	84.49			
	8.74	11.93	0.62	15	7.40	84.63			
	11.62	11.93	0.83	17	9.90	85.21			

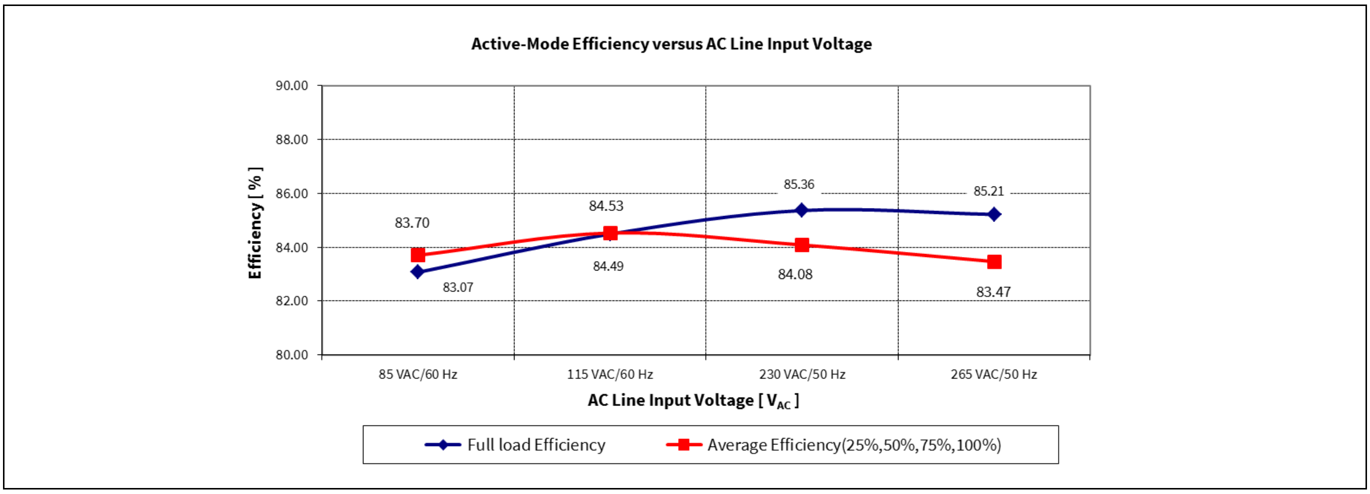


Figure 7 Efficiency vs AC line input voltage

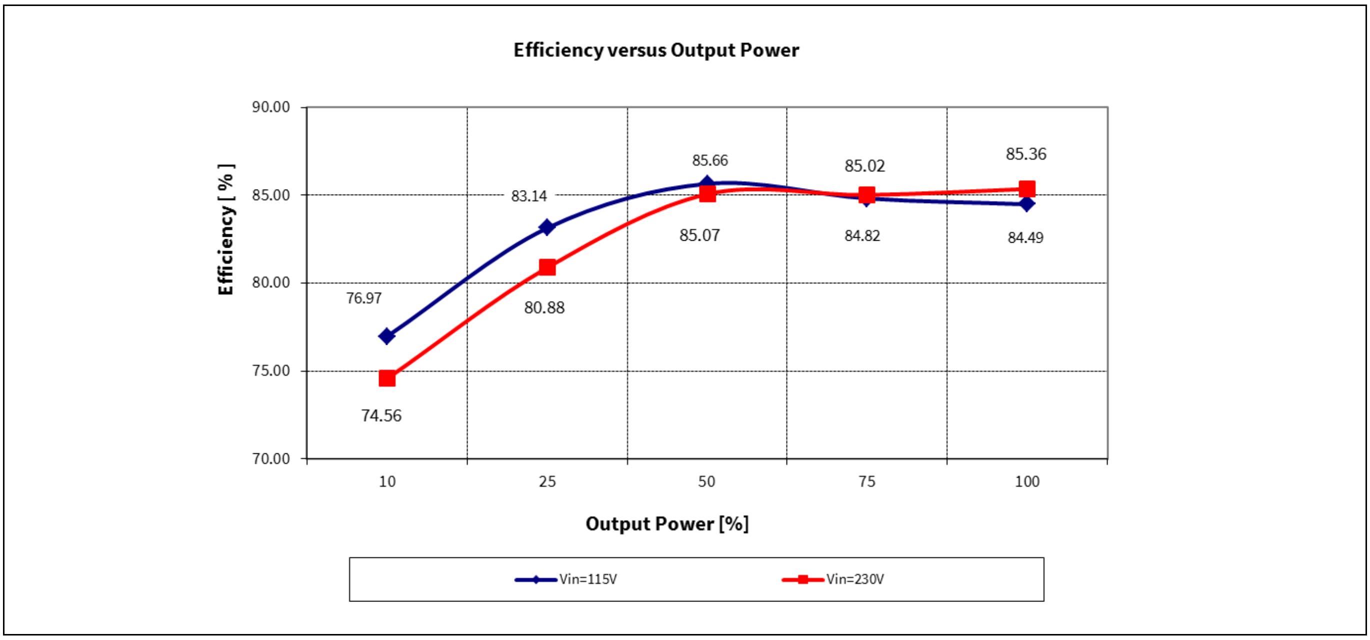


Figure 8 Efficiency vs output power at 115 V_{AC} and 230 V_{AC} line

9.2 Standby power

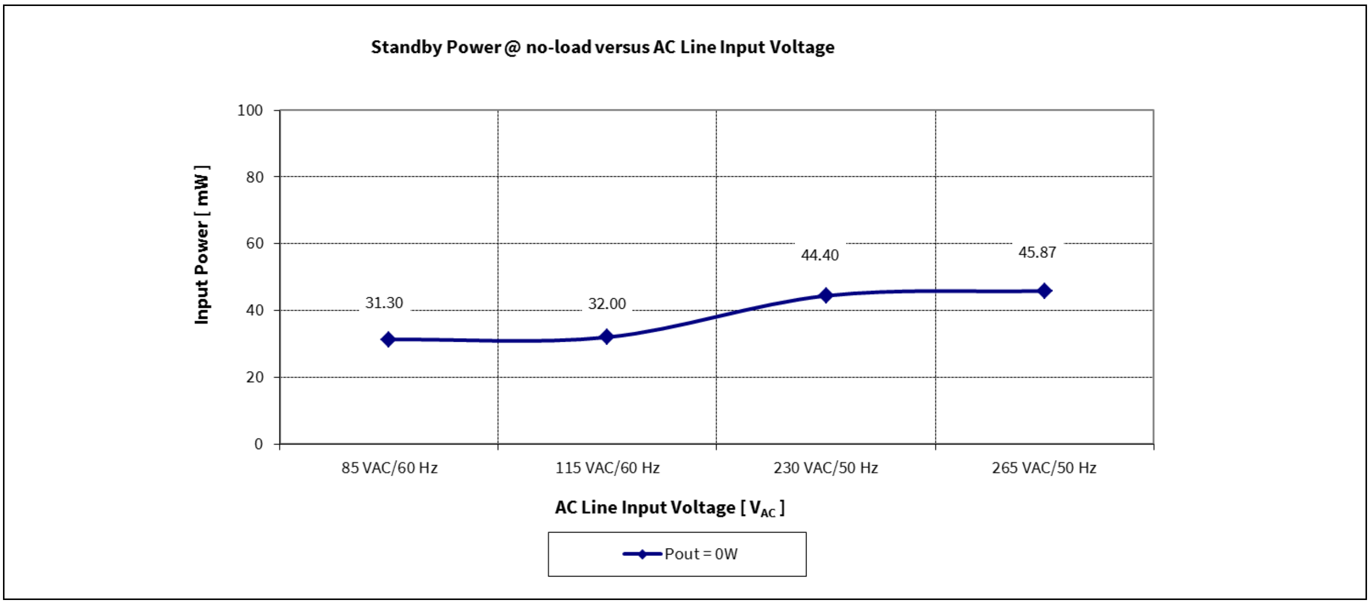


Figure 9 Standby power at no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

9.3 Line regulation

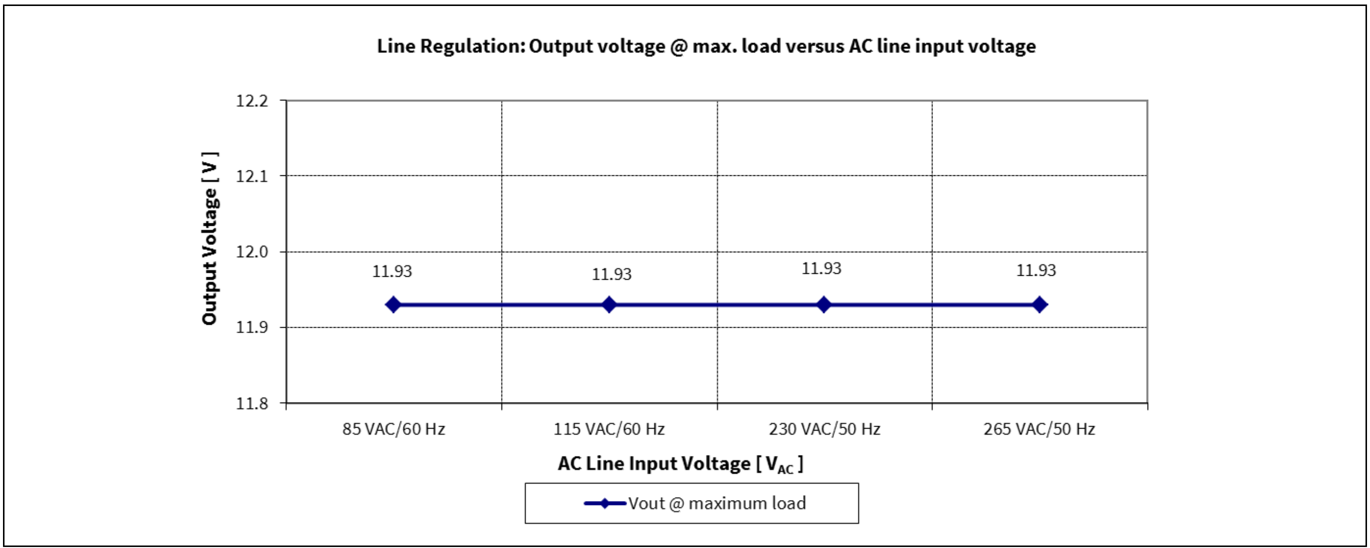


Figure 10 Line regulation Vout at full load vs AC line input voltage

9.4 Load regulation

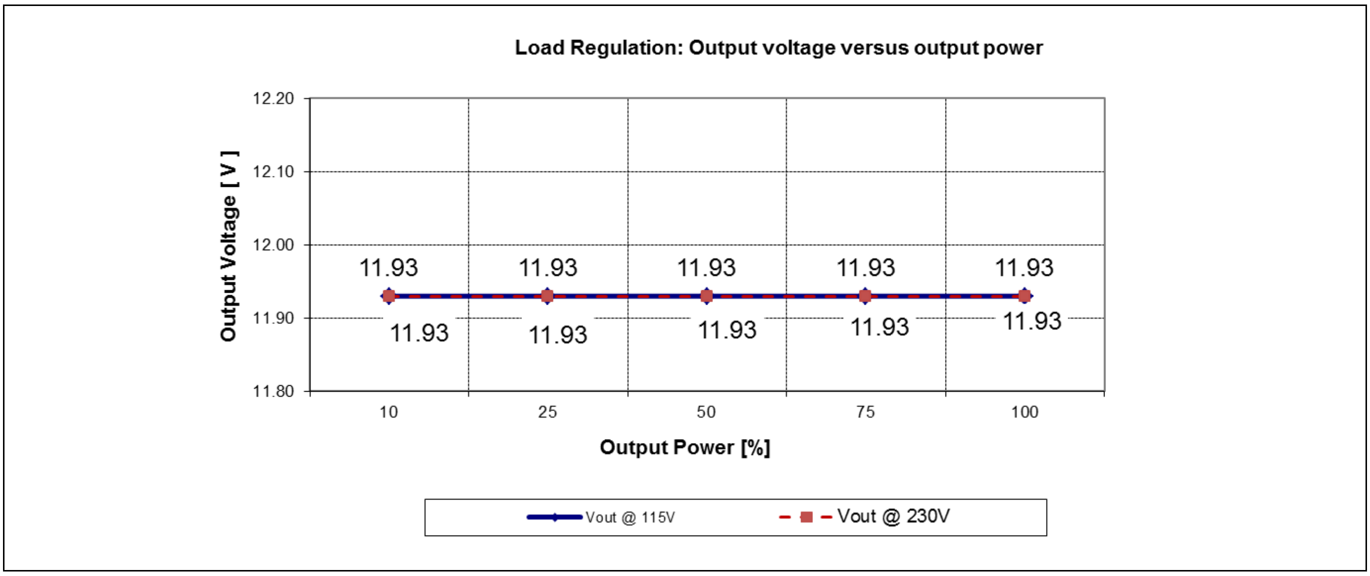


Figure 11 Load regulation V_{out} vs output power

9.5 Maximum input power

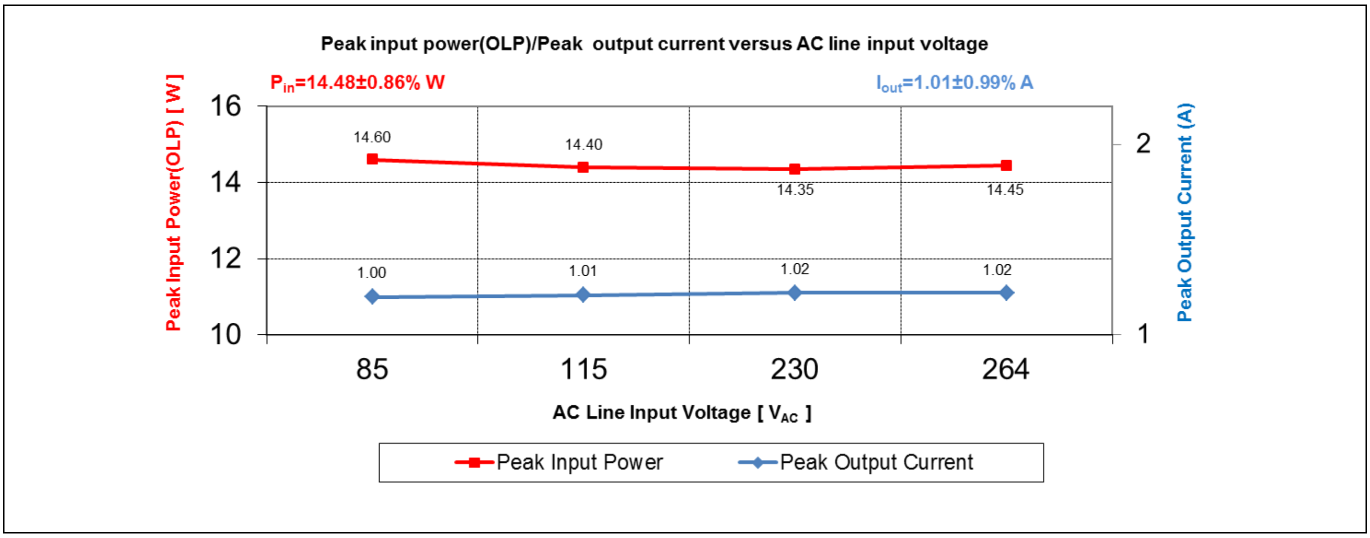


Figure 12 Maximum input power (before over-load protection) vs AC line input voltage

9.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 Level 4 (±8 kV for both contact and air discharge).

9.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 3 (±1 kV for line to line and ±2 kV for line to earth).

9.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (10 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

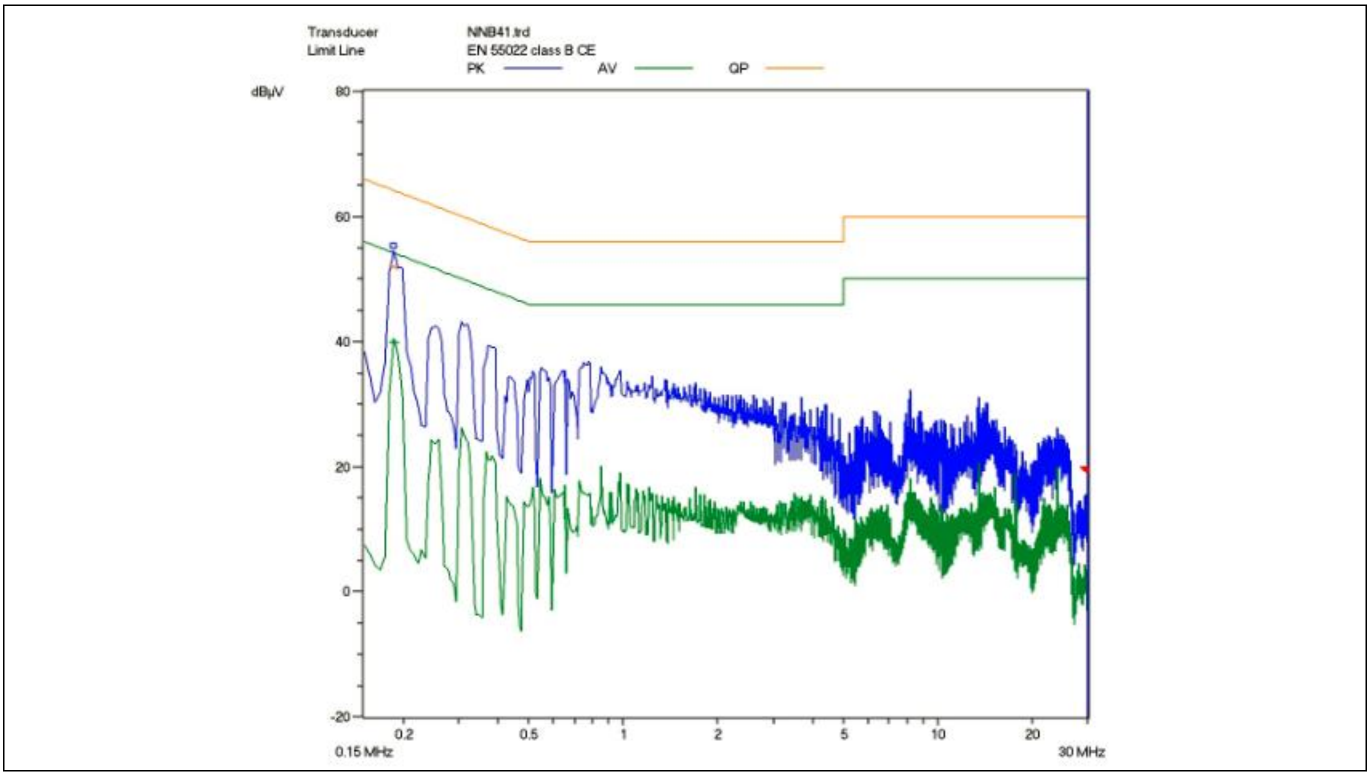


Figure 13 Conducted emissions(Line) at 115 V_{AC} and maximum Load

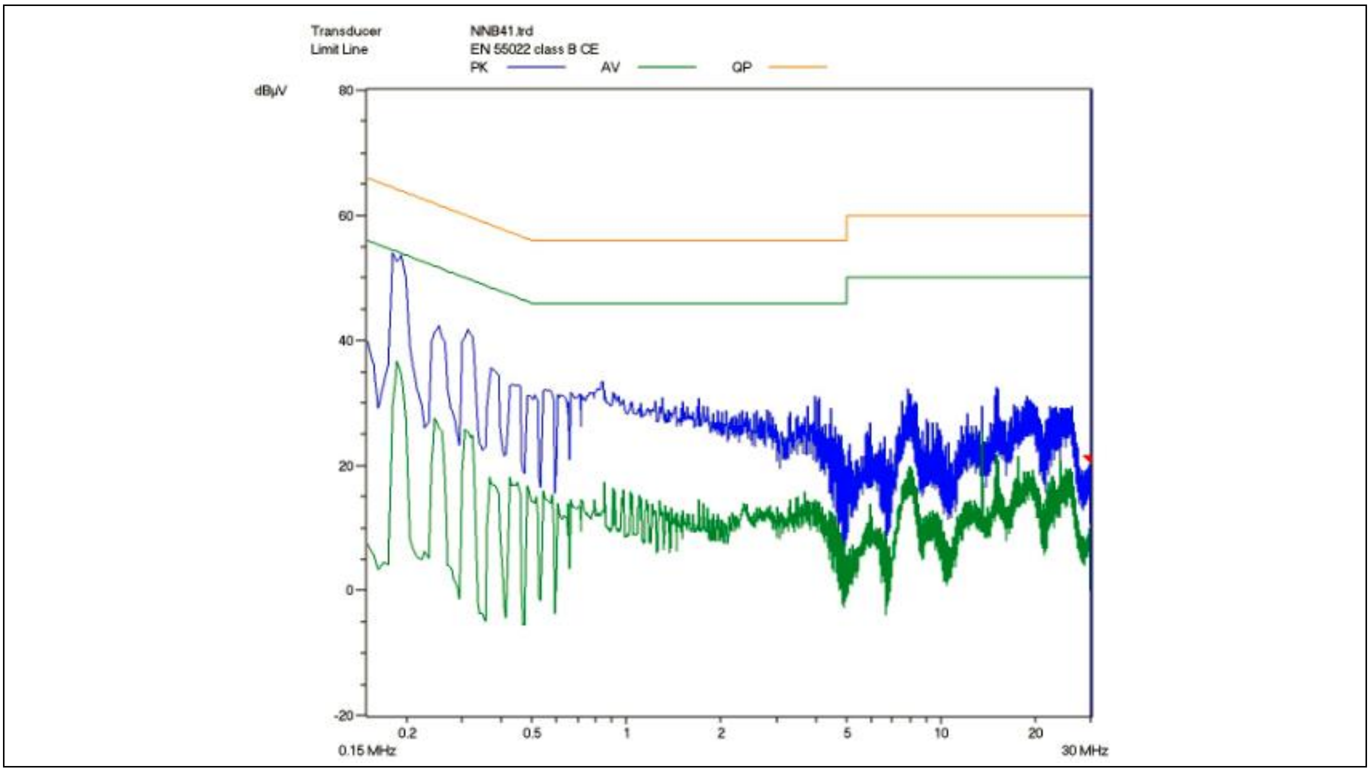


Figure 14 Conducted emissions(Neutral) at 115 V_{AC} and maximum Load

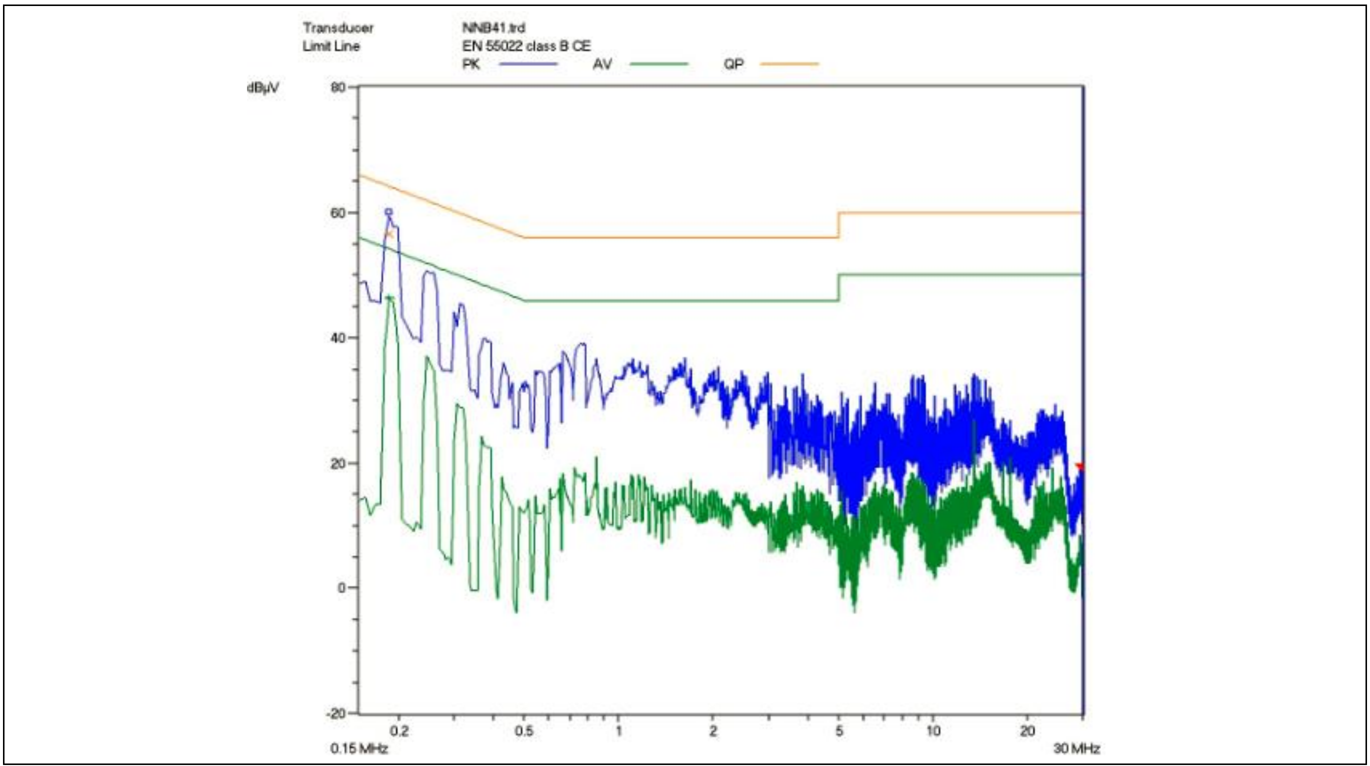


Figure 15 Conducted emissions(line) at 230 V_{AC} and maximum Load

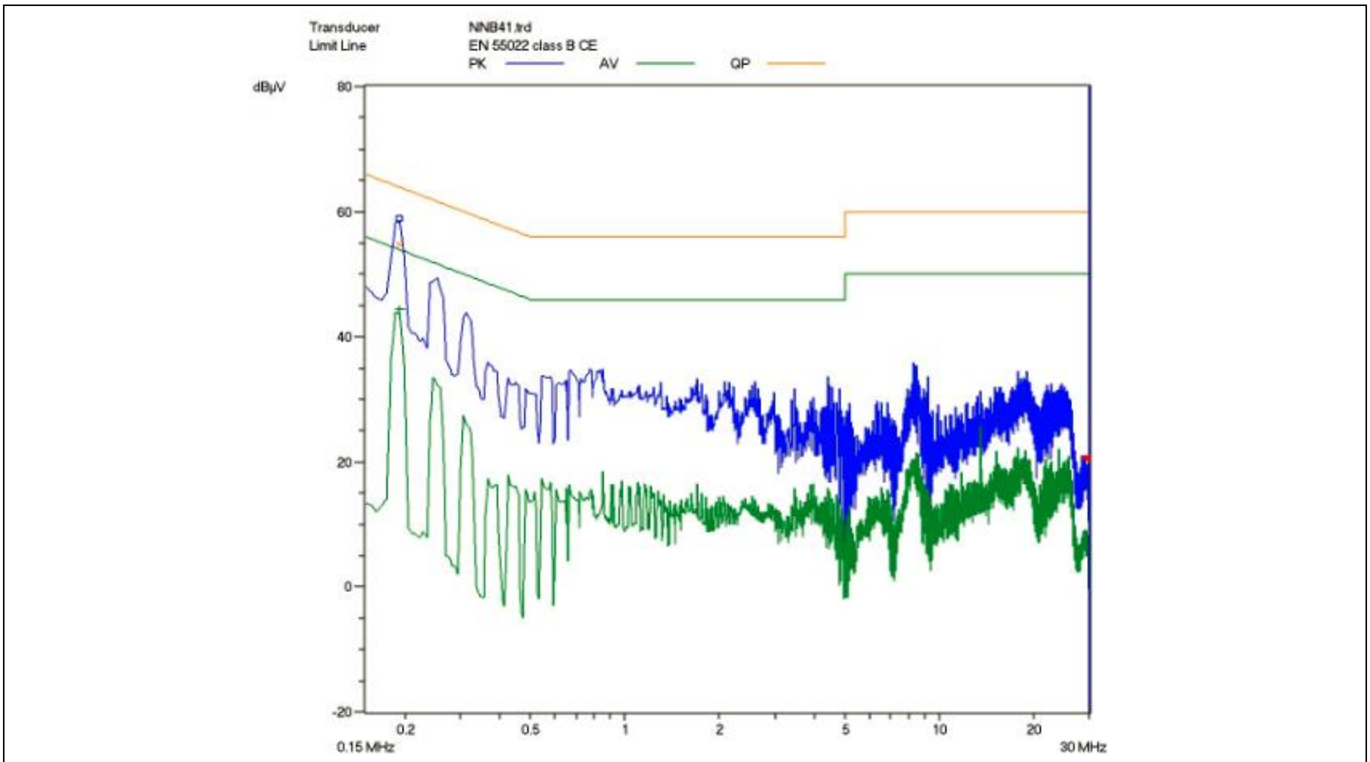


Figure 16 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

Figure 17 Pass conducted emissions EN55022 (CISPR 22) class B with 6 dB margin.

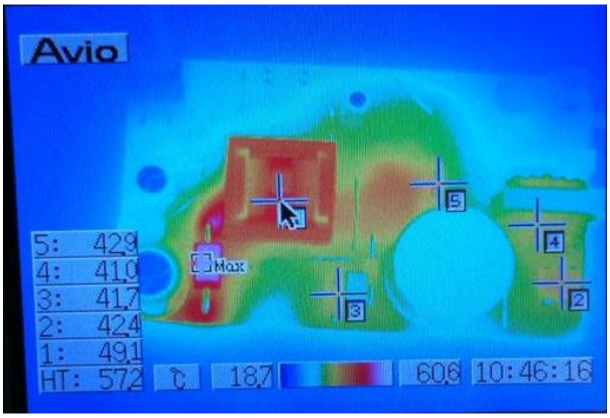
9.9 Thermal measurement

The thermal test of open frame demo board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25°C. The measurements were taken after two hours running at full load.

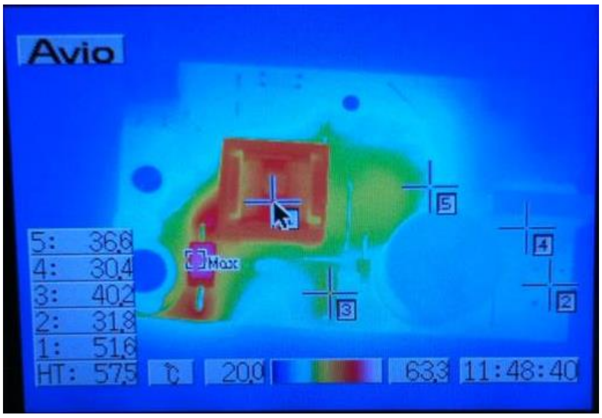
Table 5 Hottest temperature of demo board

No.	Major component	85 V_{AC} (°C)	265 V_{AC} (°C)
1	IC11 (ICE3RBR4765JG)	46.7	43.0
2	BR1	42.4	31.8
3	L11	41.0	30.4
4	TR1	49.1	51.6
5	D21	57.2	57.5
6	R15	42.9	36.6
7	Ambient	25	25

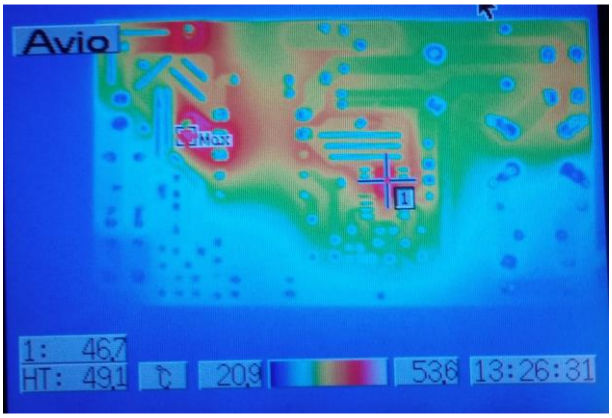
85 V_{AC} full load and 25°C ambient	265 V_{AC} full load and 25°C ambient



PCB top side



PCB top side



PCB bottom side

PCB bottom side

Figure 18 Infrared thermal image of DEMO-3RBR4765JG

Figure 19

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

10.1 Startup at low/high AC line input voltage with maximum load

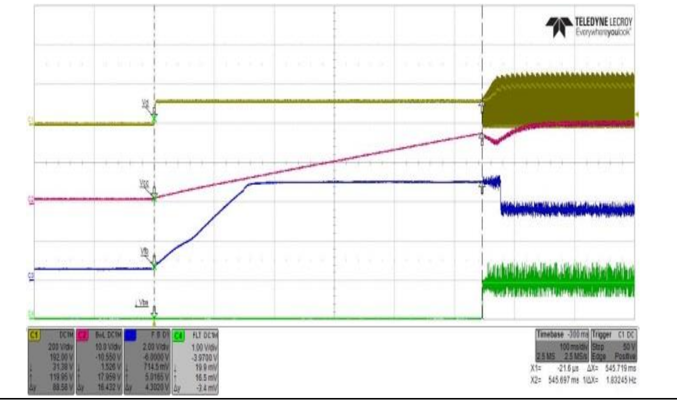
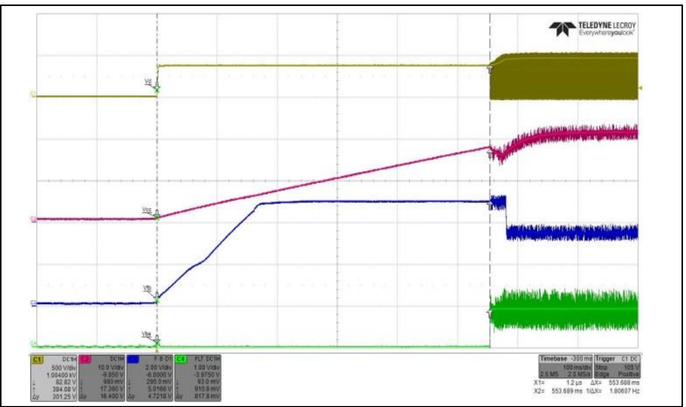
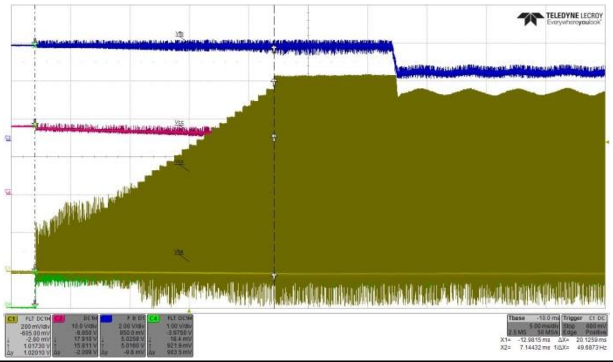
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : BA voltage (V_{BA})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : BA voltage (V_{BA})
Startup time at 85 V_{AC} & maximum load ≈ 550 ms	Startup time at 265 V_{AC} & maximum load ≈ 550 ms

Figure 20 Startup

10.2 Soft start

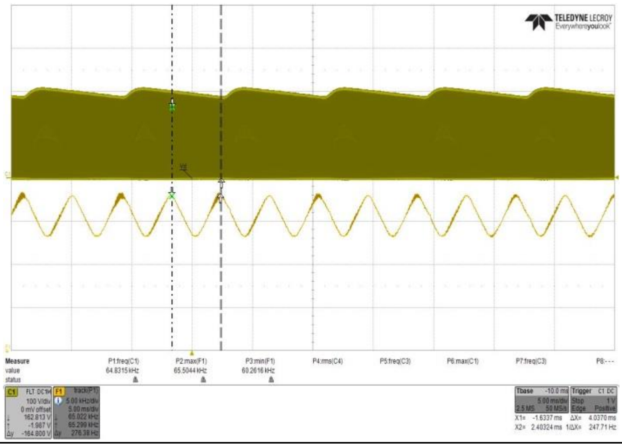


C1 (Yellow) : Current sense voltage (V_{CS})
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : BA voltage (V_{BA})

Soft start time at 85 V_{AC} and maximum load ≈ 20 ms

Figure 21 Soft start

10.3 Frequency jittering



C1 (Yellow) : Drain voltage (V_{Drain})
F1 (Yellow) : Frequency track of C1

Frequency jittering at 85 V_{AC} and maximum load ≈ 64 kHz ~ 69 kHz, Jitter period is ≈ 3.8 ms

Figure 22 Frequency jittering

10.4 Drain and current sense voltage at maximum load

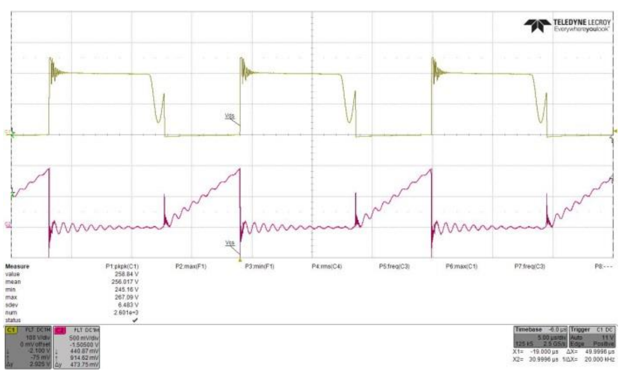
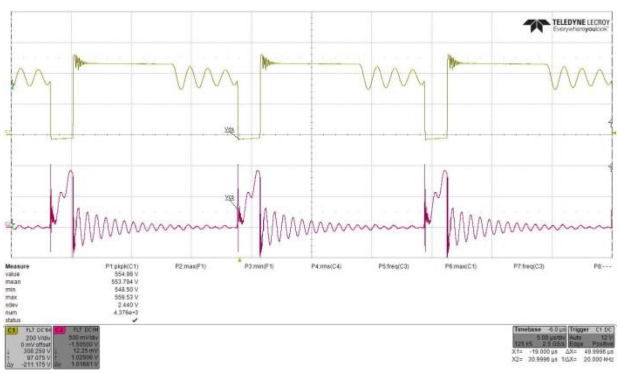
	
C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})
V_{Drain_peak} at 85 V_{AC} ≈ 267 V	V_{Drain_peak} at 265 V_{AC} ≈ 559 V

Figure 23 Drain and current sense voltage at maximum load

10.5 Load transient response (Dynamic load from 10% to 100%)

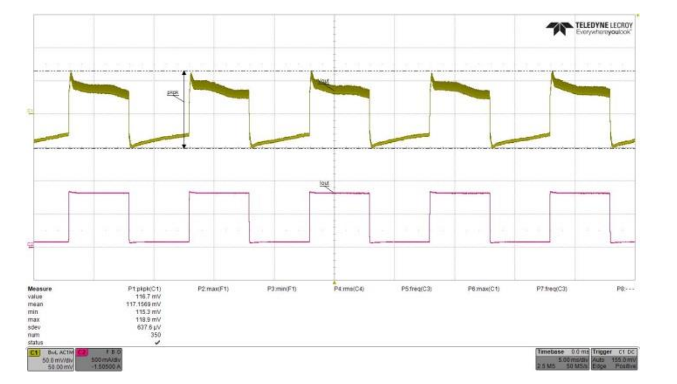
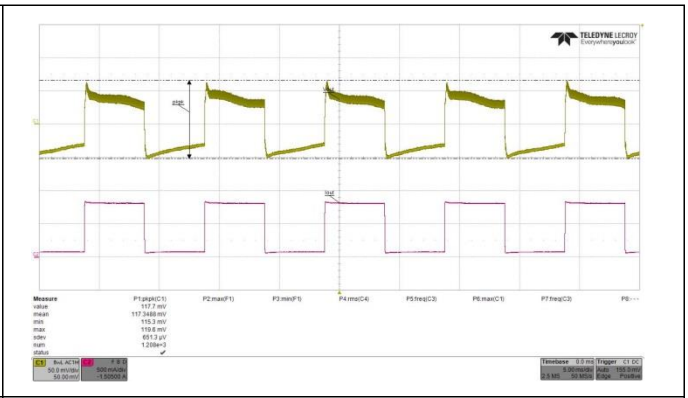
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 120 mV (Load change from 10% to 100% at 85 V_{AC},100 Hz,0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 120 mV (Load change from10% to 100% at 265 V_{AC},100 Hz,0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 24 Load transient response

10.6 Output ripple voltage at maximum load

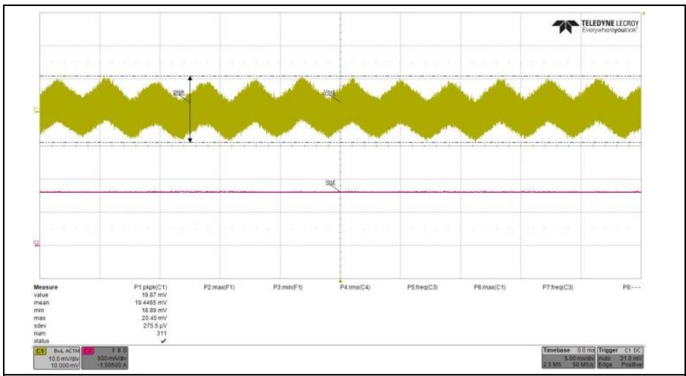
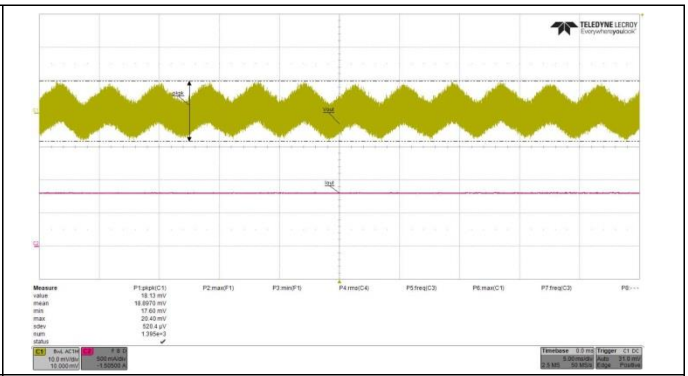
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 20 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 20 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 25 Output ripple voltage at maximum load

10.7 Output ripple voltage at burst mode 1 W load

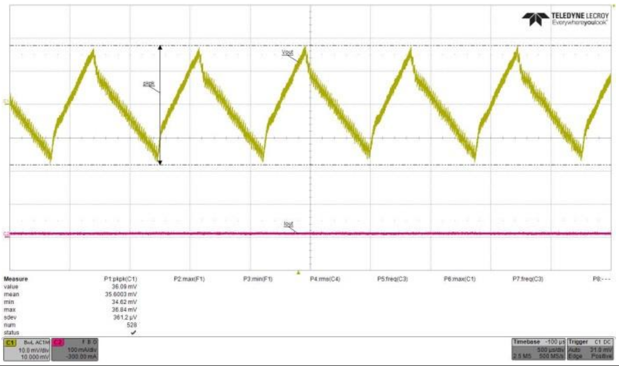
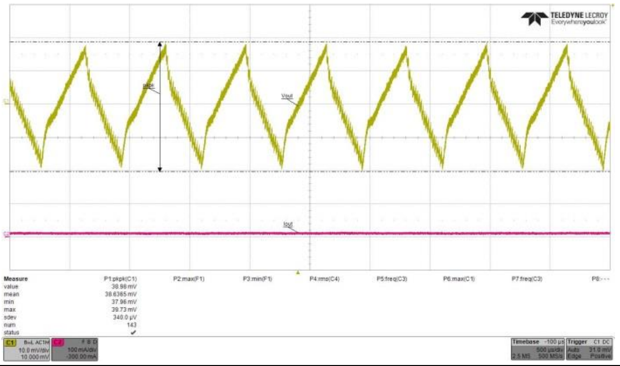
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 36 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 39 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 26 Output ripple voltage at burst mode 1 W load

10.8 Active burst mode

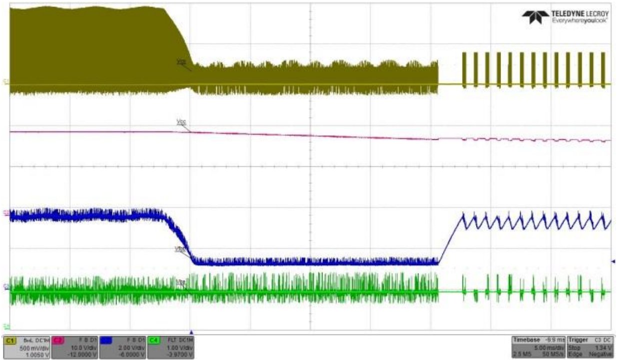
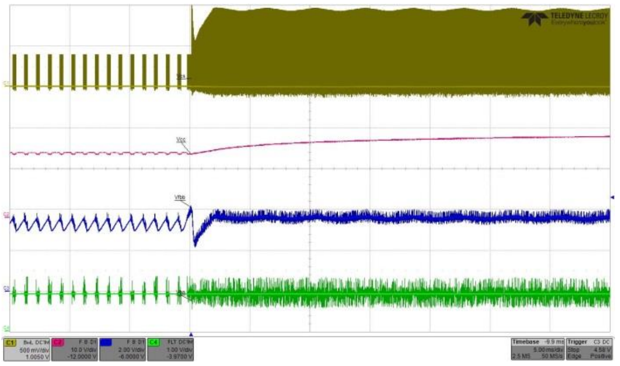
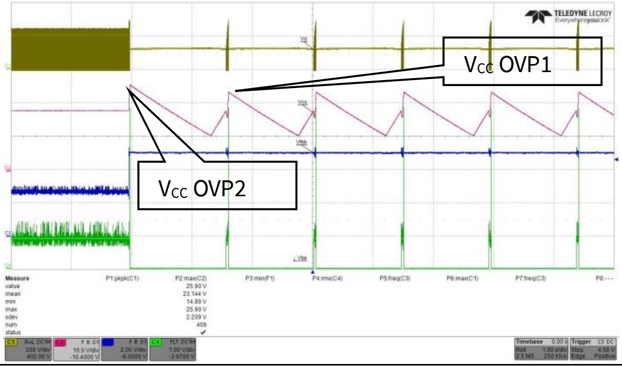
	
C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : BA voltage (V_{BA})	C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : BA voltage (V_{BA})
Condition to enter burst: V_{FB} < 1.35 V and last for 20 ms (load change form full load to 1 W load)	Condition to leave burst: V_{FB} > 4.0 V (load change form 1 W load to full load)

Figure 27 Active burst mode at 85 V_{AC}

10.9 VCC over voltage protection

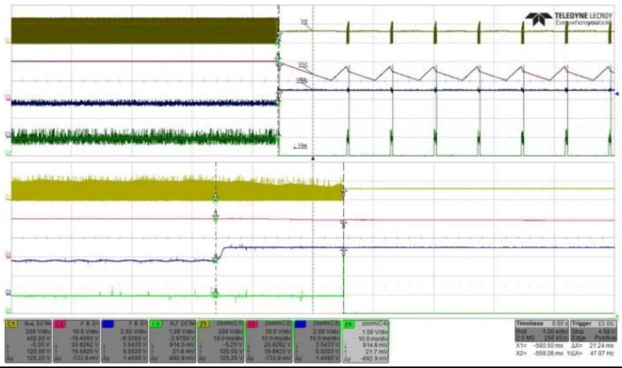


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : BA voltage (V_{BA})

Condition to enter VCC over voltage protection: V_{CC} > 25.5 V
V_{CC} > 20.5 V and V_{FB} > 4.0 V and during soft start
(Short the diode of optocoupler(Pin 1 and 2 of IC12) during system operating at 85 V_{AC}, 0.4 A load)

Figure 28 VCC overvoltage protection

10.10 Over load protection

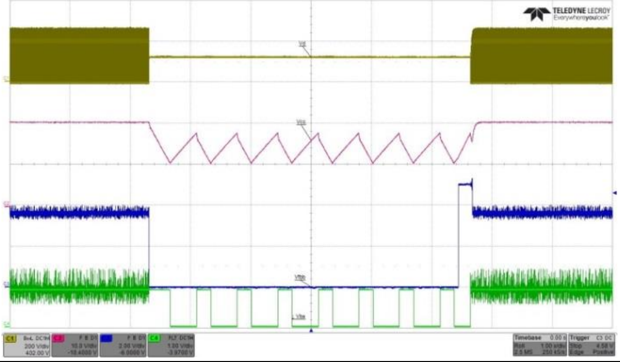


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : BA voltage (V_{BA})

Condition to enter over load protection: V_{FB} > 4.0 V, last for 20 ms and extended blanking time
(output load change from full load to 2 A at 85 V_{AC})

Figure 29 Over load protection

10.11 VCC under voltage/Short optocoupler protection

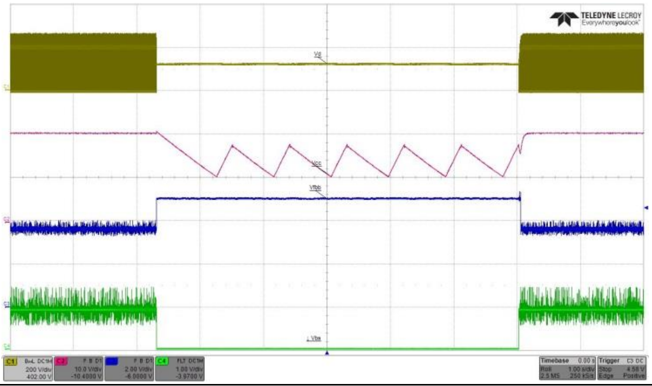


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : BA voltage (V_{BA})

Condition to enter VCC under voltage protection: $V_{CC} < 10.5$ V
(short the transistor of optocoupler(Pin 3 and 4 of IC12) during system operating at full load and release at 85 V_{AC})

Figure 30 VCC under voltage/short optocoupler protection

10.12 External auto restart enable



C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FBB})
C2 (Green) : BA voltage (V_{BA})

Condition to enter external protection enable: $V_{BA} < 0.33$ V
(short BA pin to Gnd by 10 Ω resistor during system operating at full load and 85 V_{AC})

Figure 31 External auto restart enable

11 References

[1] ICE3RBR4765JG datasheet, Infineon Technologies AG

[2] AN-PS0025-CoolSET F3R DIP-8, DIP-7, DSO-16/12 new jitter version design guide-V2.2

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First release.

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