Battery-powered BLDC motor drive design using the 6EDL71x1 series

Design guide and recommendations

Author: Peter B. Green

About this document

Scope and purpose

This document discusses the design of three-phase motor drive inverters primarily for battery-powered brushless DC (BLDC) motor drives, based on the 6EDL71x1 series of three-phase smart gate drivers. The focus of this document is on system design and recommended practices to achieve best performance and avoid potential issues.

The purpose of this document is to provide designers with a useful design guide, which also describes how to use Infineon's motor control design software tools tailored to this smart gate driver family. In addition, hardware design and component selection recommendations are provided as well as PCB layout guidelines to help achieve best performance and avoid known system issues.

Intended audience

This document addresses the market for cordless power tools, outdoor power equipment (OPE), robotics and other battery-powered BLDC motor drive applications. It is intended for design engineers, applications engineers and students working on BLDC motor drive designs.

Table of contents

Table of contents

1 Introduction

1.1 Brushless DC motors and drives

The basic construction of a BLDC motor (also known as an electronically commutated or EC motor) consists of a stator containing multiple wound coils and a rotor containing permanent magnets forming one or more pole pairs. Unlike brushed DC (BDC) motors, BLDC motors are commutated by controlled switching of the inverter connected to the stator windings instead of using mechanical brushes in contact with the rotor. The windings are arranged in two or three phases and energized in a determined sequence to generate a rotating magnetic field. The rotor permanent magnet attempts to align with the stator field, producing torque and rotary motion. Maximum torque is produced when the rotor and stator field vectors are positioned at 90 degrees to each other. Hall effect or other sensor types are often embedded in the stator to detect the rotor angular position, which may or may not be required depending on the control scheme used.

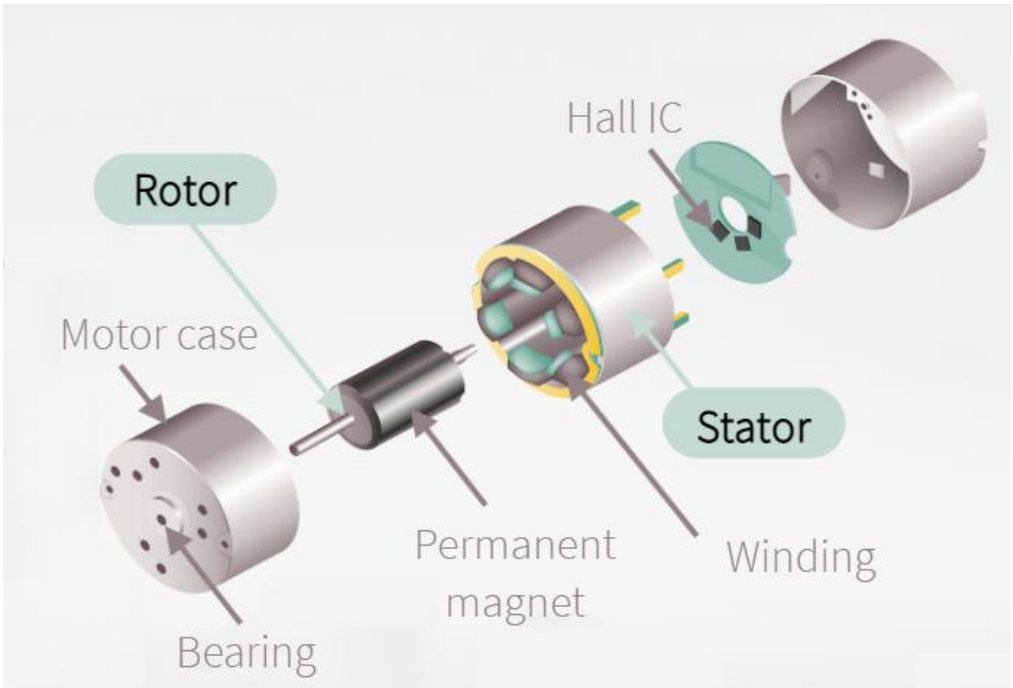


Figure 1 Three-phase BLDC motor exploded diagram

The stator windings may be connected in wye or delta configuration:

- The wye (Y-shaped) configuration, sometimes called a star winding, connects all of the windings to a central point, and power is applied to the remaining end of each winding. Wye configuration gives high torque at low speed but a lower top speed.
- The delta configuration connects three windings to each other in a triangle-like circuit, and power is applied at each of the connections. A motor with windings in delta configuration gives low torque at low speed but can give a higher top speed.

The wye winding is normally more efficient because delta-connected windings have a closed loop which allows parasitic currents that create losses. The control method used to drive these different BLDC motor types is basically the same.

Permanent magnet synchronous motors (PMSM) are of similar construction except that they has sinusoidal back-emf, whereas BLDC motors have trapezoidal back-emf.

The electrical behavior of the motor is determined by the phase winding inductance and resistance coupled with the back EMF produced when the motor is rotating. These elements are represented in **Figure 2**.

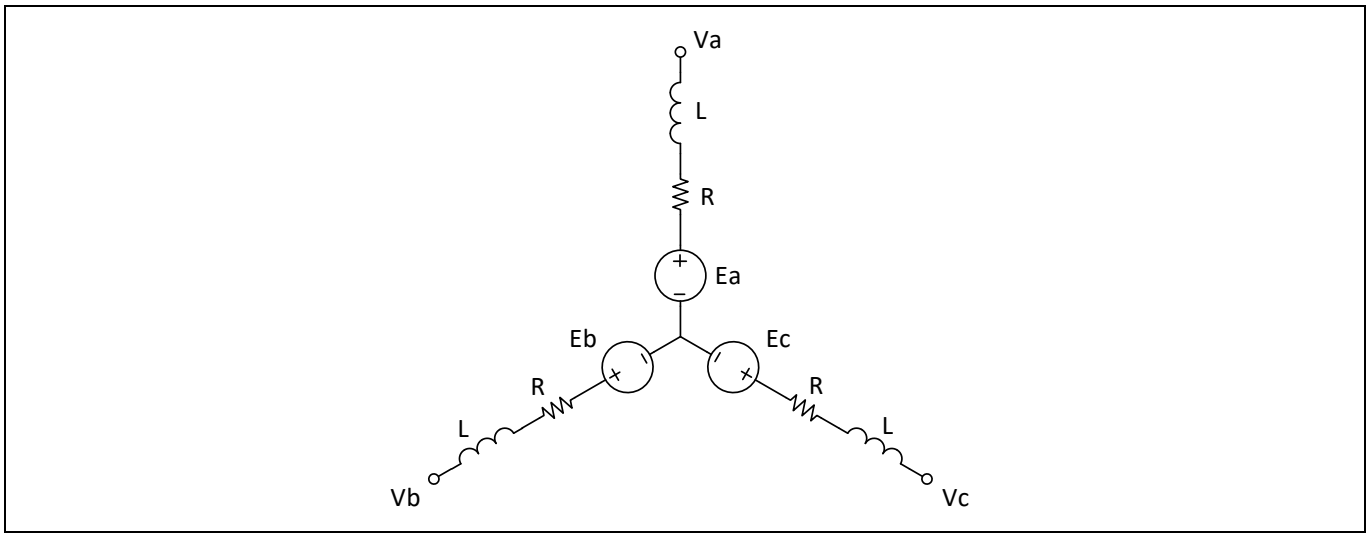


Figure 2 Three-phase BLDC motor electrical model (wye configuration)

The following equation describes the winding voltage and current:

$$V_{a,b,c} = \frac{di_{a,b,c}}{dt} \cdot L + i_{a,b,c} \cdot R + E_{a,b,c} \quad [2]$$

The three-phase motor drive inverter consists of a microcontroller running firmware that executes a control algorithm that produces pulse-width modulated (PWM) signals supplied to the 6EDL71x1 gate driver PWM inputs. The driver outputs are connected to the MOSFETs forming the six switches of the power stage. Additional circuitry is included for battery management, which is not covered in this application note. The inverter may include one, two or three current shunts for sensing the low-side MOSFET source currents.

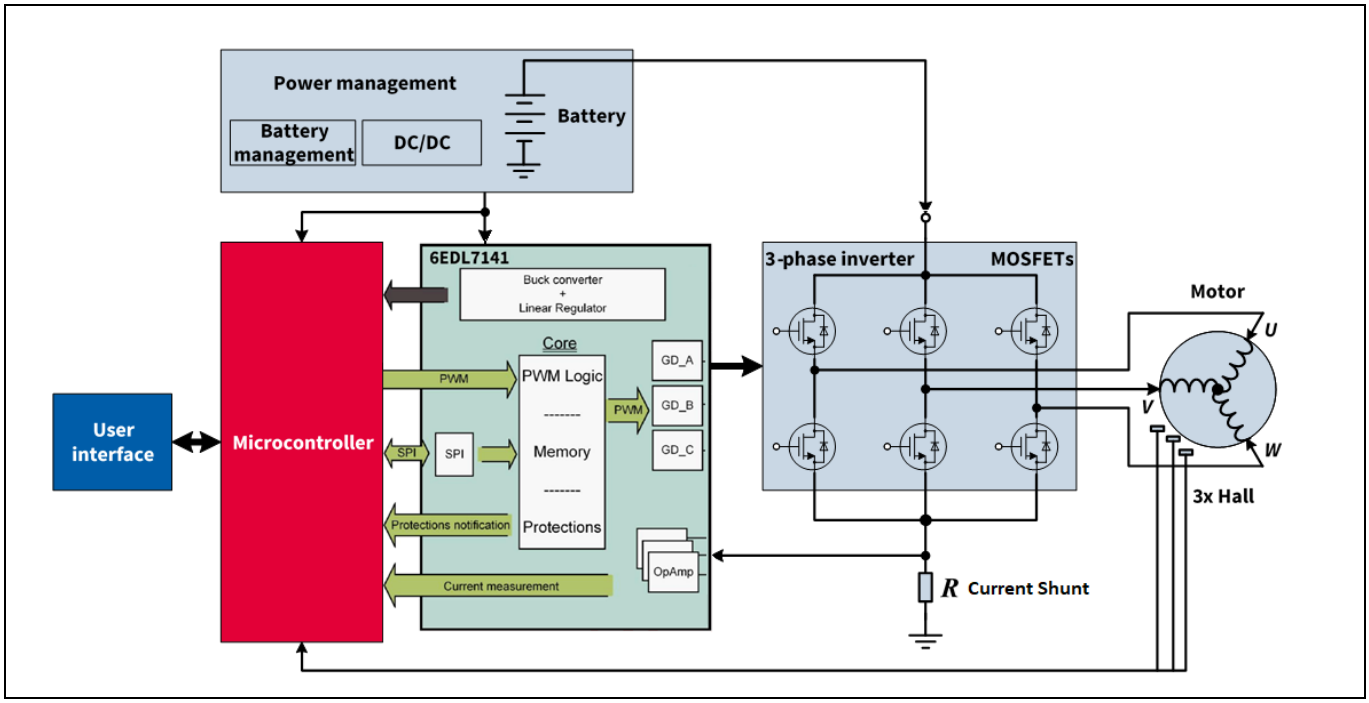


Figure 3 6EDL7141-based BLDC motor drive inverter system block diagram (one shunt example)

1.2 6EDL71x1 series driver functional overview

The 6EDL7141 and 6EDL7151 are three-phase smart gate drivers designed for BLDC or permanent magnet synchronous motor drive systems. They consist of a configurable three-phase half-bridge gate driver able to operate in multiple PWM modes from an input voltage PVDD range of 5.5 V up to 60 V for the 6EDL7141 and 70 V for the 6EDL7151. These smart driver ICs also include an integrated DC-DC synchronous buck converter and low-dropout linear voltage regulator as well as configurable precision current sense (CS) amplifiers. System parameters are stored in a digital core, which includes a serial peripheral interface (SPI) for communication with a microcontroller to allow configuration of a wide range of system parameters. Configuration may also be performed via a PC using Infineon's BLDC motor control workbench graphical user interface (GUI) software tool.[1] This works with the 6EDL_SPI_LINK interface board, which connects to a USB type A port. Configuration settings can be stored in RAM or made permanent by burning to one-time programmable (OTP) memory.

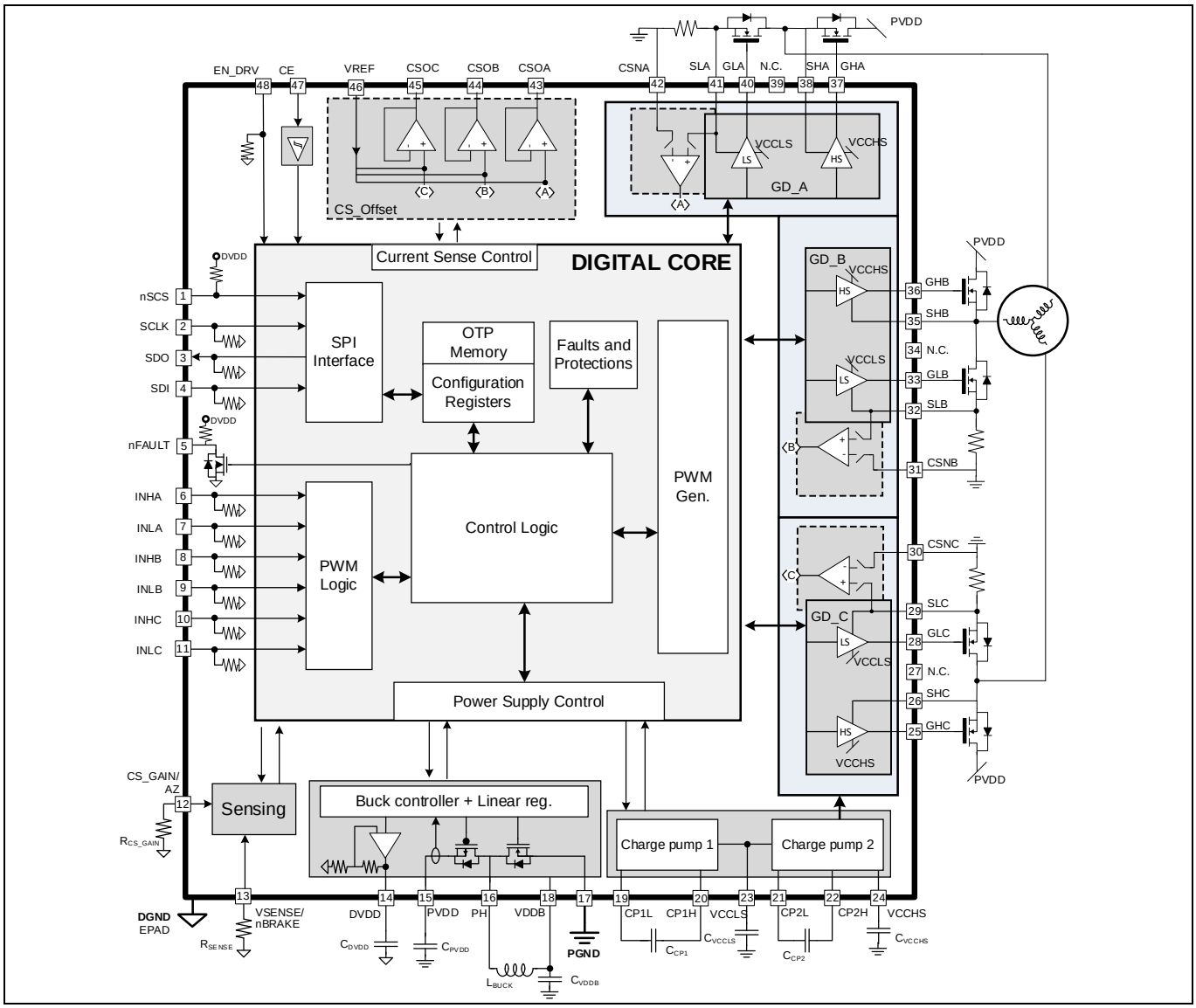


Figure 4 6EDL7141 internal block diagram

[1] The BPA motor control workbench GUI may be downloaded using the Developer Center Launcher: https://www.infineon.com/cms/en/design-support/tools/utilities/infineon-developer-center-idc-launcher/

1.2.1 PWM modes

PWM signals from the microcontroller provide the gate drive control pulses, which can be decoded in several different ways. The 6EDL71x1 provides gate drive pulses to the three-phase inverter low- and high-side MOSFETs. The gate drive output voltages (PVCC) can be selected from several different levels between 7 V and 15 V. Here are some of the PWM modes supported:

- 6PWM
- 3PWM with Hall or optical position sensing
- 1PWM with Hall sensors

This allows the designer flexibility in terms of microcontroller selection to cover a variety of different applications. In 1PWM and 3PWM modes the dead time is configurable in the 6EDL71x1.

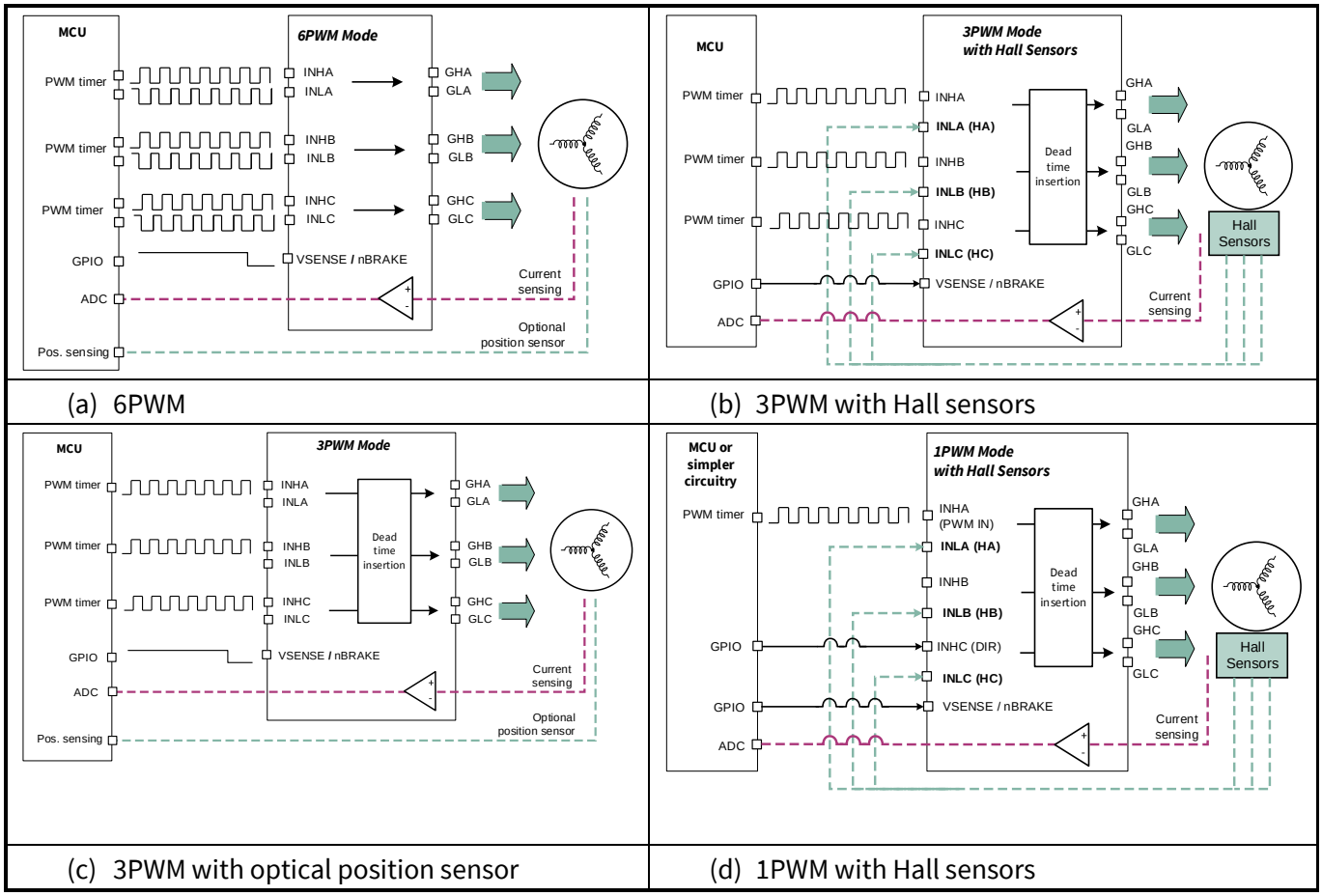


Figure 5 PWM switching modes supported by the 6EDL71x1

Note: ***It should be noted that in 6PWM mode the dead time is set by the microcontroller PWM outputs. In 3PWM and 1PWM modes the dead time is set by the 6EDL71x1.***

A key feature of the 6EDL71x1 driver is the ability to control the slew rate of the phase node voltages at each of the half-bridge nodes connecting to the motor phases shown in **Figure 3**. This is achieved by digital configuration of the gate drive sink and source currents and timing. The 6EDL71x1 series gate driver outputs can be connected directly to each MOSFET gate without any external resistors or other components. Switch-on and switch-off profiles can be optimized to determine the slew rate and thereby minimize EMI and switch-off transients by configuration of the gate drive current during the switching process.

Note: ***The PWM drive pulses produced by the microcontroller that connect to the 6EDL71x1 inputs should not be less than a defined minimum pulse width! The microcontroller firmware must define a minimum pulse width and ensure that pulses shorter than this are not generated under any condition. This is necessary because the 6EDL71x1 gate drive outputs require a certain amount of time to complete the turn-on and turn-off transitions. A typical value is stated in the 6EDL71x1 datasheet; however, this time period will vary depending on the gate drive configuration settings and the type of MOSFET used in the inverter.***

1.2.2 Current sense amplifiers and comparators

The 6EDL7141 and 6EDL7151 integrate three precision CS amplifiers, which can be used to measure the current in the inverter via shunt resistors. Single-, double- or triple-shunt measurements are supported. Each CS amplifier can be enabled individually. The gain and offset are configured internally and can be set via the user interface. An additional output buffer allows adding a variable offset voltage to the sense amplifier output, which can be set to four different values either by programming the internally generated level or by applying an external voltage at the VREF input pin so that negative current in current shunts can also be measured.

A positive overcurrent comparator detects an overcurrent condition on a motor winding for a positive shunt voltage. This comparator can be used to apply PWM cycle-by-cycle pulse truncation, terminating the gate drive to limit the maximum motor current. An additional negative overcurrent comparator is also used for detecting the overcurrent condition on motor winding for negative shunt currents. A built-in DAC is used for programming the thresholds of the overcurrent comparators.

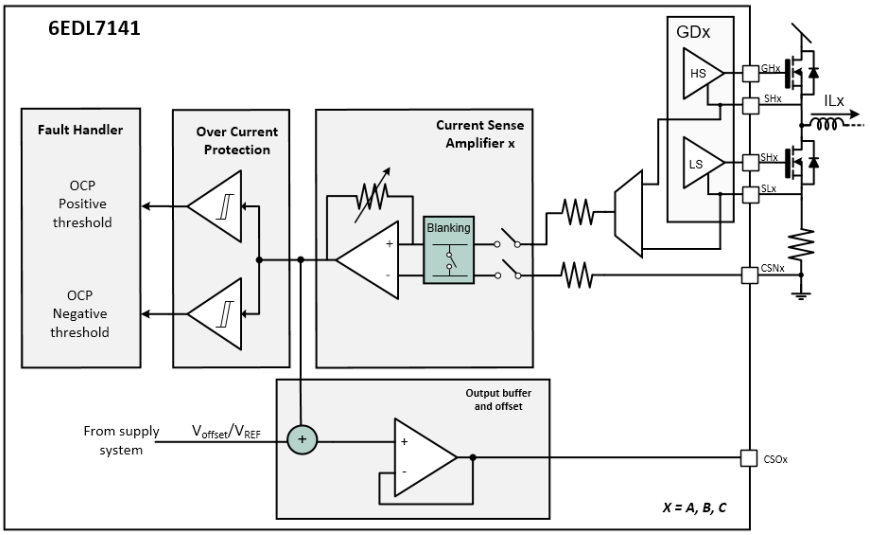


Figure 6 6EDL71x1 CS amplifiers and comparators

1.2.3 Integrated buck, linear regulators, and charge pumps

The 6EDL7141 and 6EDL7151 also include an integrated power system infrastructure based on a synchronous buck regulator and linear regulator (LDO). This converts the battery voltage to an internal voltage (VDDB), which is set to 6.5 V, 7 V, or 8 V depending on the gate drive voltage setting, able to supply up to 300 mA. The only external components required are the inductor and capacitor. The buck regulator output (VDDB) supplies the linear regulator, which can provide a noise-free 3.3 V or 5 V supply (DVDD) for the internal digital circuitry and external microcontroller.

Integrated low- and high-side charge pumps supplied from the buck regulator provide the gate driver supply voltages, which enable duty cycles up to 100 percent. Each charge pump uses an external switched capacitor (CP1 for the low-side and CP2 for the high-side) to transfer charge from the buck converter output to the gate driver bias supplies: VCCLS and VCCHS. VCCLS is referenced to the system zero-volt rail and VCCHS is referenced to the system positive supply rail. The voltage level is referred to as PVCC, which is equal to VCCLS and VCCHS-PVDD. Unlike conventional half-bridge drivers, the 6EDL71x1 includes an advanced high-side driver scheme that enables VCCHS to able to supply the switch-on voltage and current to the high-side gate drivers for all three phases without the need for separate floating supplies for each phase. The values of the switched capacitors and bias supply capacitors, CVCCLS and CVCCHS, need to be selected according to the datasheet instructions for the charge pumps to operate correctly. The charge pump clock frequency is selectable from 195.3 kHz, 390.6 kHz, 781.3 kHz, or 1.56 MHz with optional frequency modulation to reduce EMI.

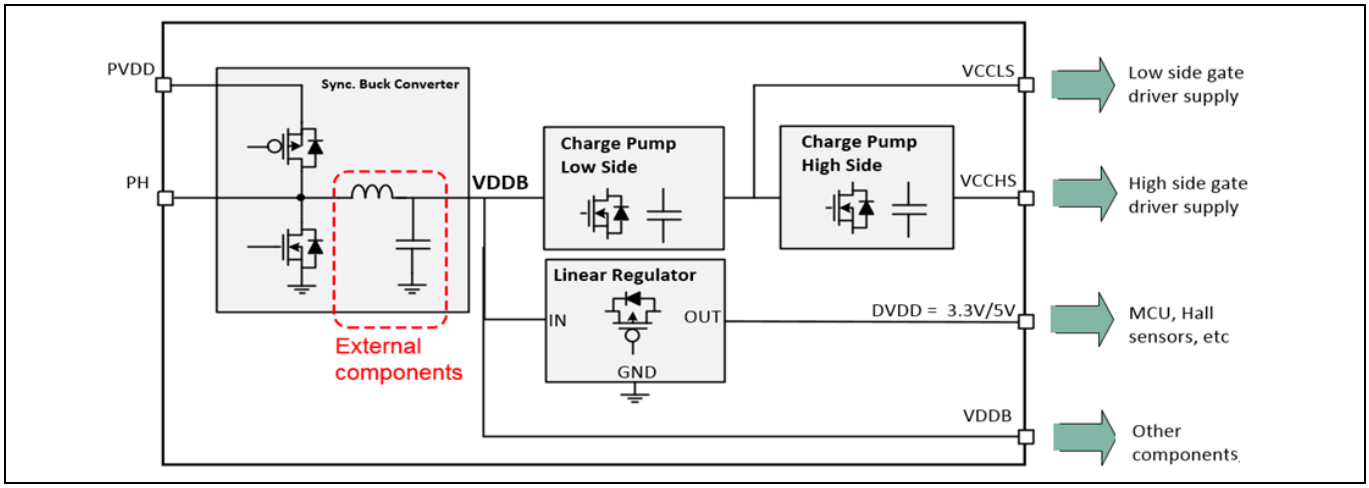


Figure 7 6EDL71x1 integrated power supplies

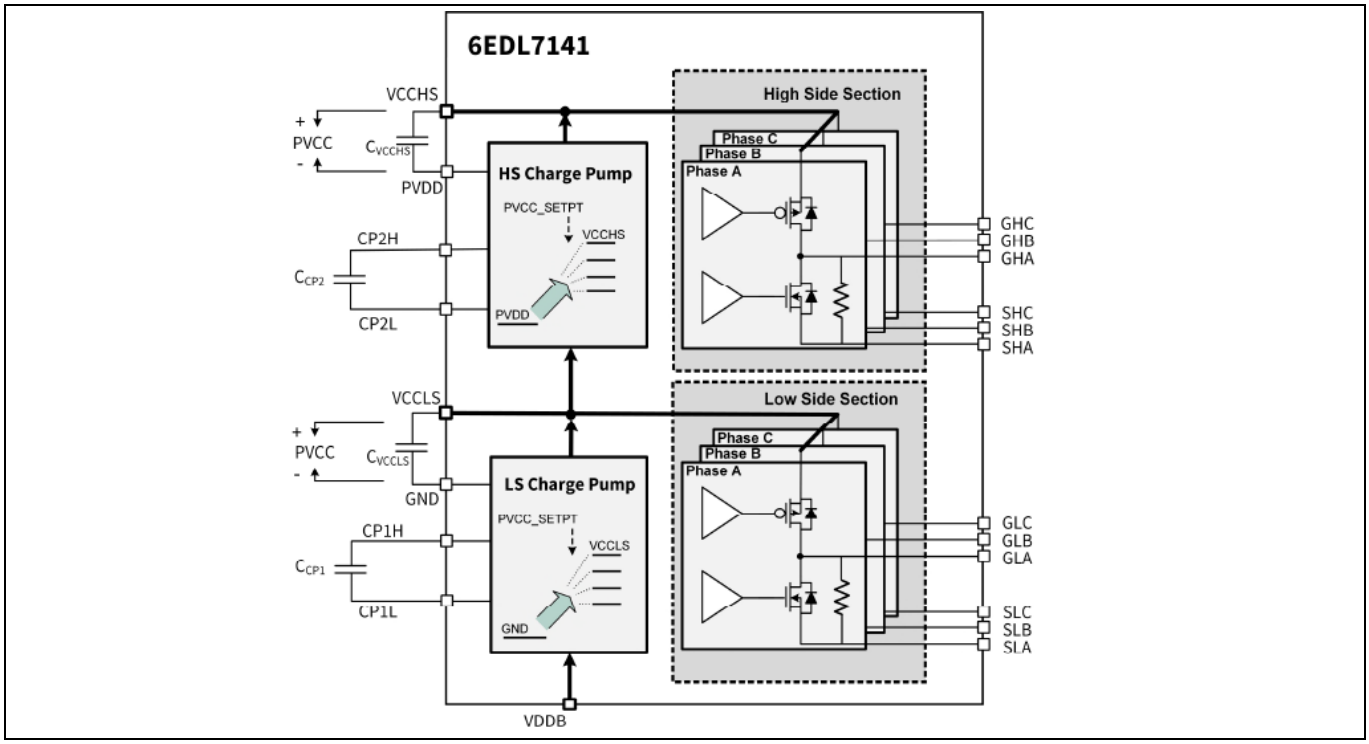


Figure 8 6EDL71x1 integrated charge pumps and gate drivers

The 6EDL71x1 also incorporates the following additional protection functions:

- Overcurrent protection (OCP) for the internal power supplies and inverter phases
- Undervoltage lock-out (UVLO) for the input bus voltage and digital supply voltage
- Overtemperature detection, warning and shutdown
- A configurable watchdog (WD) timer
- Locked rotor detection based on Hall sensor inputs and memory fault detection

2 System functional description

2.1 Commutation methods

The three-phase BLDC motor drive inverter may employ either trapezoidal/six-step commutation (also known as block commutation) or field-oriented control (FOC). Implementations may be sensed using some type of position sensor (e.g., Hall sensors) or may be sensor-less, utilizing more complex control algorithms capable of determining the rotor position from phase current measurements.

In the various different cases different PWM switching modes may be used, which are supported by the 6EDL71x1 as described in **Section 1.2.1**. In each case the PWM operates at a fixed frequency and the duty cycle is adjusted to control the stator winding currents in each phase. The switching frequency is typically around 10 kHz. The winding inductances remove most of the PWM switching frequency component but a certain amount of high-frequency (HF) ripple remains. If used, position sensors may be connected to the microcontroller or directly to the 6EDL71x1, depending on which PWM mode is being used. More complex control algorithms such as sensor-less FOC would require 6PWM mode. 3PWM and 1PWM modes may be used with more basic microcontrollers in cost-sensitive applications.

2.1.1 Trapezoidal/six-step (block) commutation

Th 6EDL71x1 series of gate drivers can support the trapezoidal PWM schemes listed in the table below, which may be selected by firmware.

Table 1 Trapezoidal commutation PWM schemes

Modulation scheme	Description
Low-side modulation	Modulation is applied to the low-side switches
High-side modulation	Modulation is applied to the high-side switches
High-side modulation with synchronous rectification	Modulation is applied to the high-side switches with a complementary pulse to the low-side switches

Basic low- and high-side modulation schemes do not use synchronous rectification (SR) and rely on the MOSFET body diode to conduct during the PWM off periods. This adds to the conduction losses in these devices; therefore, it is preferable to use SR. In this case the complementary MOSFET is switched on during the freewheeling period with a dead time inserted to avoid any overlap and resulting shoot-through current.

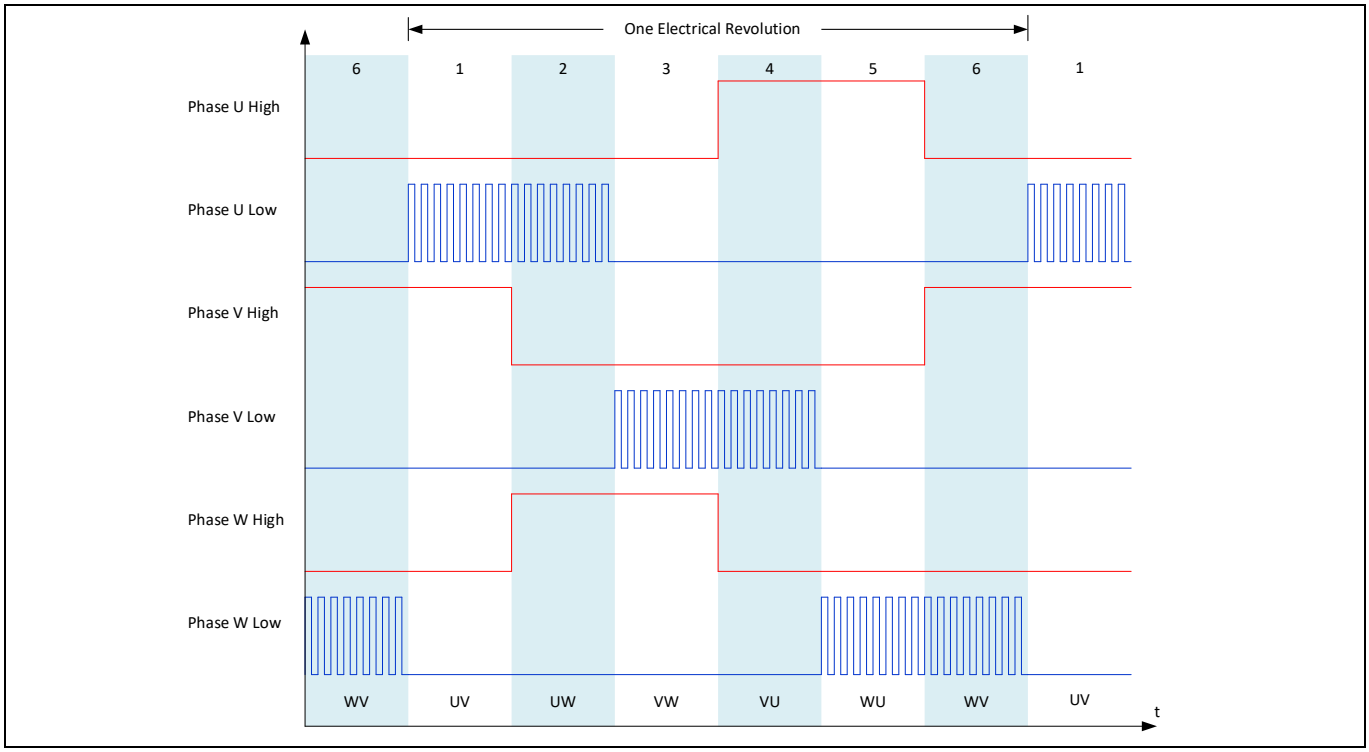


Figure 9 Low-side modulation

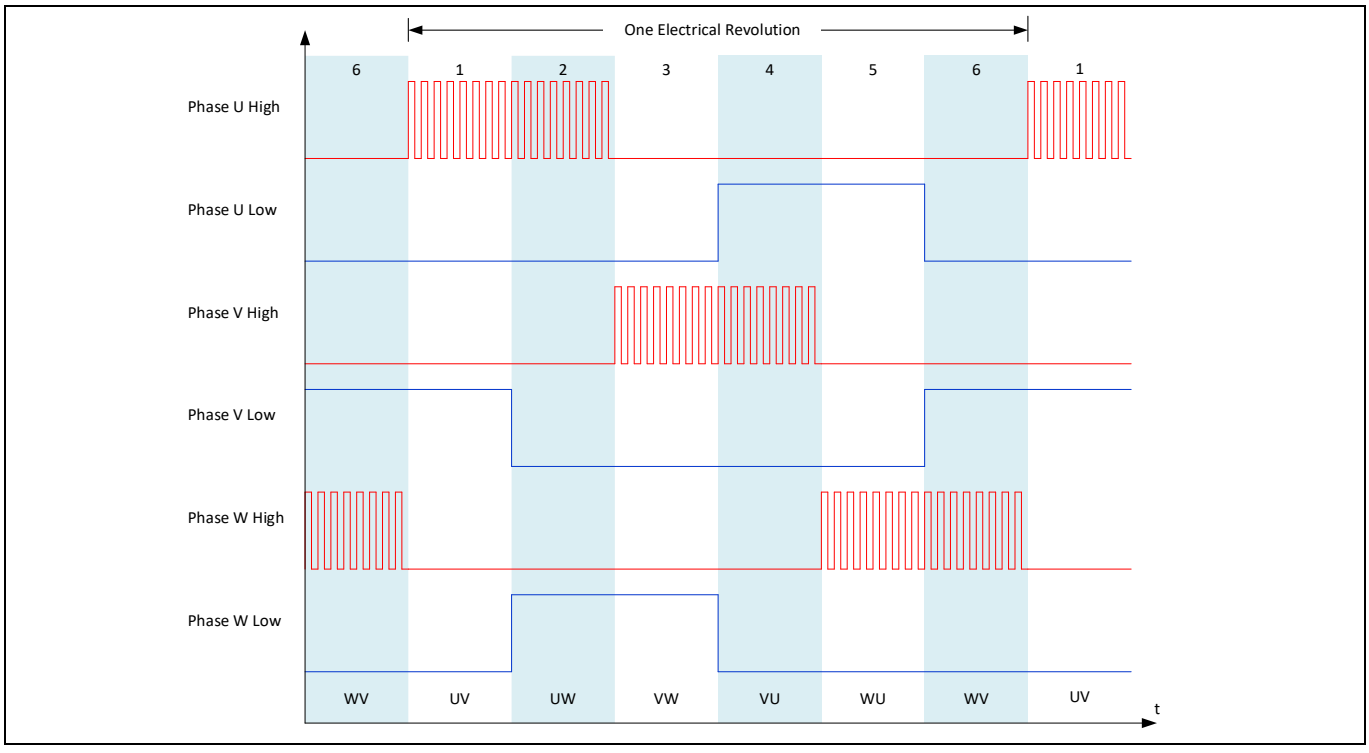


Figure 10 High-side modulation

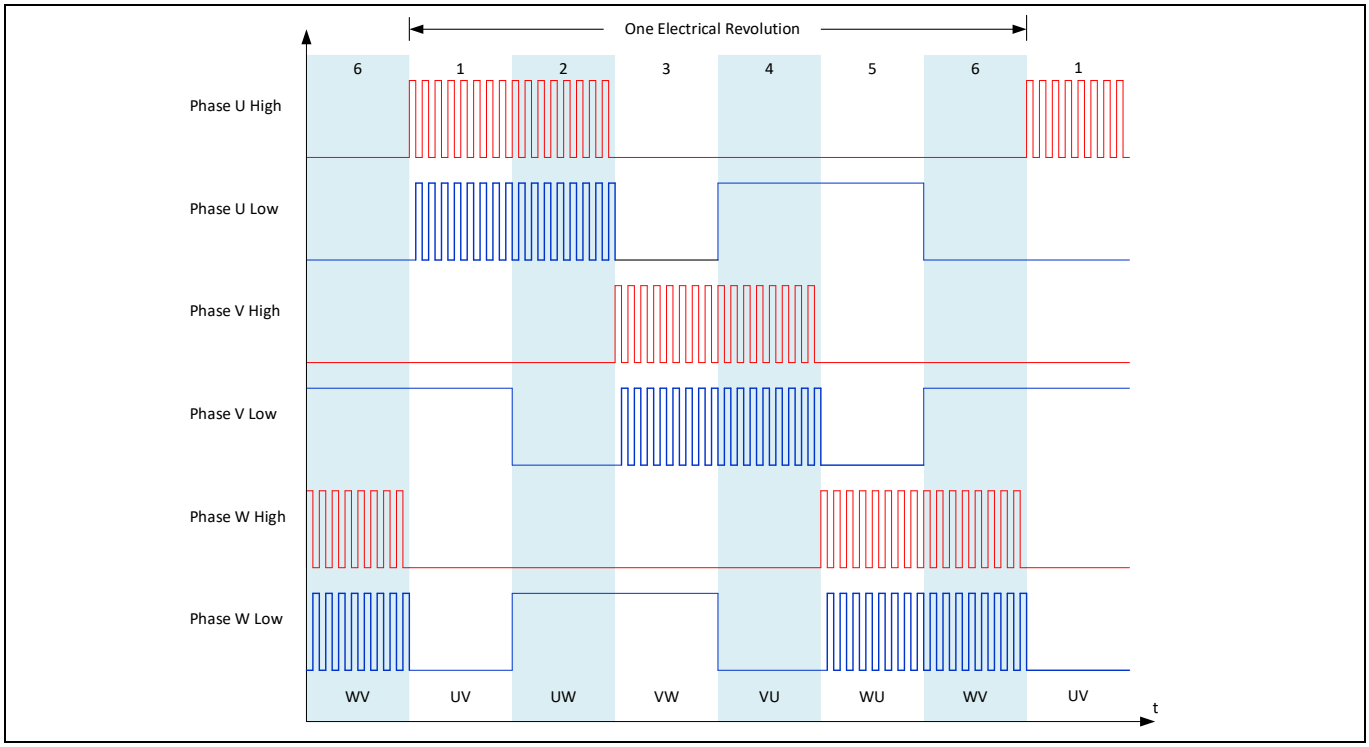


Figure 11 High-side modulation with SR

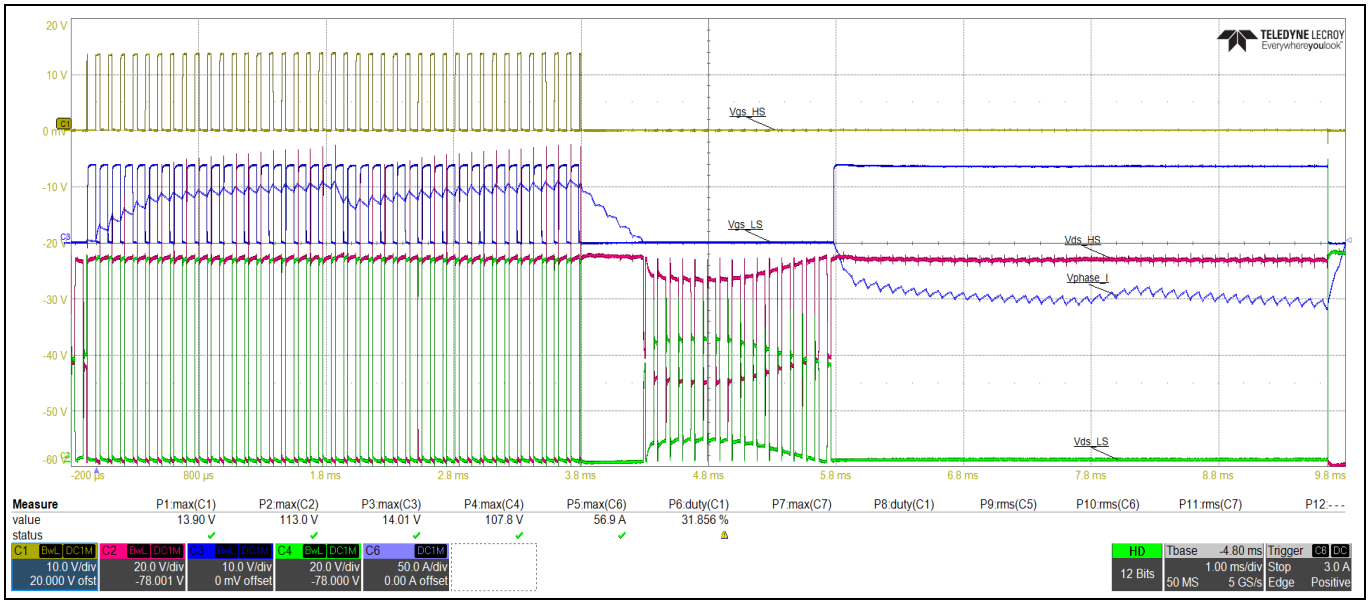


Figure 12 High-side modulation with SR phase waveforms – V_{GS_HS} (yellow), V_{GS_LS} (blue), V_{DS_HS} (red) V_{DS_LS} (green), I_{PHASE} (purple)

During high-side modulation with SR the switching dead time is inserted between the rising and falling edges of the PWM signals to prevent the high- and low-side MOSFETs of each inverter phase from being on at the same time during switching transitions (shoot-through condition). The body diode of each MOSFET conducts current when the MOSFET is off.

2.1.2 Field-oriented control

FOC is a form of sinusoidal phase current control. A simplified representation of the PWM gate drive switching patterns used in FOC is shown in **Figure 13**.

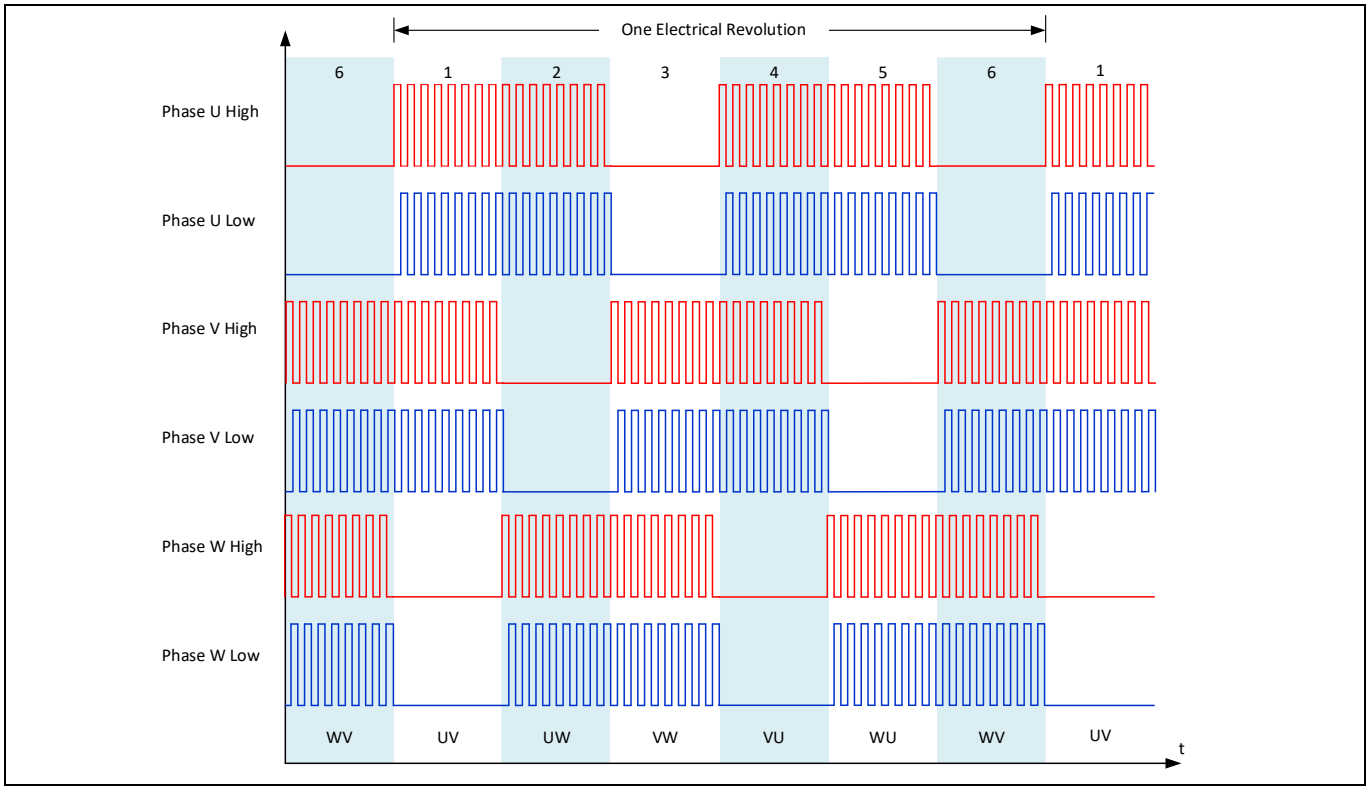


Figure 13 FOC switching pattern (simplified, modulation is not shown)

In the real implementation the pulse widths are modulated to produce sinusoidal phase currents.

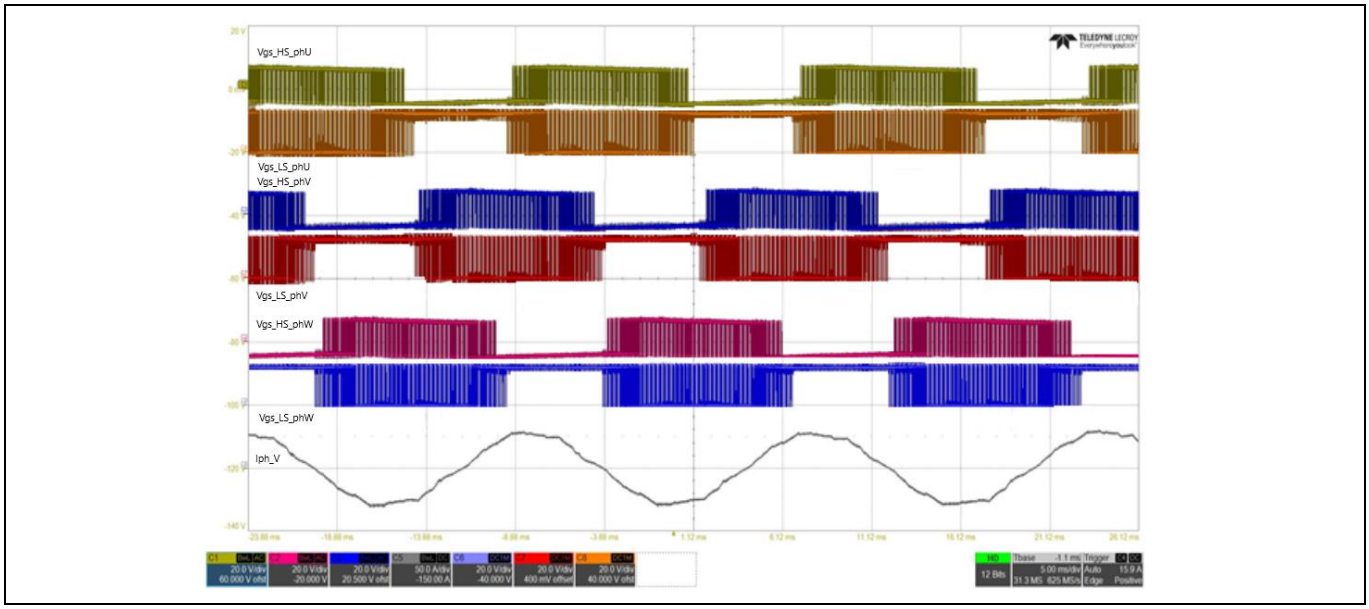


Figure 14 High- and low-side gate drive pulses (5 ms/div) – $V_{GS\_HS\_phU}$ (yellow), $V_{GS\_LS\_phU}$ (orange), $V_{GS\_HS\_phV}$ (blue) $V_{GS\_LS\_phV}$ (red), $V_{GS\_HS\_phW}$ (pink), $V_{GS\_LS\_phW}$ (purple), I_{PHASE_phV} (gray)

FOC is often implemented in sensor-less control schemes, for which 6PWM mode is mostly used. Sensor-less FOC requires a microcontroller with sufficient processing power to support calculations needed to generate the vectors required based on the phase current measurements. Careful selection of the microcontroller is necessary for a successful design, based on the control method used and the required switching frequency. Higher frequencies are sometimes used with FOC to reduce torque ripple, which reduces mechanical power losses in the motor.

2.2 6EDL71x1 smart gate driver features

The high- and low-side gate drivers allow operation over the full duty-cycle range up to 100 percent by virtue of the onboard charge pumps. The gate drive voltages can be selected from the following levels: 7 V, 10 V, 12 V, and 15 V. The charge pumps allow the selected voltage levels to be maintained even if the battery voltage drops to a lower level, which allows standard gate-level MOSFETs to be used in low input voltage conditions.

Unlike typical gate drivers, the 6EDL71x1 gate drive outputs are current driven such that the source and sink currents supplied to the MOSFET gates are constant and digitally configurable. This permits the designer to eliminate diode-resistor networks commonly used with standard voltage-driven gate driver ICs. In most cases, gate resistors can be removed altogether, reducing component count and at the same time simplifying and allowing further optimization of the circuit layout. Where more than one MOSFET is used in parallel a gate resistor is still needed to connect from the gate driver output to each MOSFET gate terminal.

Control of the drain-source rise and fall times is one of the most important system optimization points for drive systems, affecting critical factors such as switching losses, dead time optimization and drain voltage ringing that can lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps to minimize EMI emissions.

2.2.1 Slew rate control

In the three-phase motor drive inverter, the half-bridge switch node voltages transition between 0 V and the DC bus voltage. Depending on the control scheme and switching patterns used in the system design, hard- or soft-switching transitions may occur.

Slew rate control is relevant to hard-switching transitions, where the voltage transition can be defined as $dv_{DS(U,V,W)}/dt$ and the current transition as $di_{D(U,V,W)}/dt$. $dv_{DS(U,V,W)}/dt$ is generally measured during the linear part of the switching transition during the Miller plateau period of the gate drive waveform, between 10 and 90 percent of the bus voltage. Slew rate is the determining factor in reaching the best tradeoff between switching losses and radiated EMI. That is to say a faster slew rate offers lower switching losses but gives rise to higher levels of ringing and HF harmonics that produce EMI. Battery-powered motor drives are required to meet radiated emission limits, defined in standards such as CISPR 14-1, which applies to household appliances, electric tools and similar apparatus.

The 6EDL71x1 series of drivers have the ability to optimize switching by controlling the rise and fall slew rates by means of advanced current-driven gate drive outputs, which control the gate drive sink and source currents during different time segments during the MOSFET switch-on and switch-off processes. This process is described in detail in the following sections.

2.2.1 Switch-on transient

Switch-on transients typically occur across the drain and source of the low-side MOSFET when the high-side MOSFET switches on. These are the result of fast-changing current interacting with MOSFET package and PCB trace inductances ($L_{package}$ and L_{PCB}). The ringing shown in the blue waveform below is a result of the low-side MOSFET body diode recovery, which occurs when the high-side MOSFET is switching on and the current is being diverted from the low-side body diode to the high-side channel.

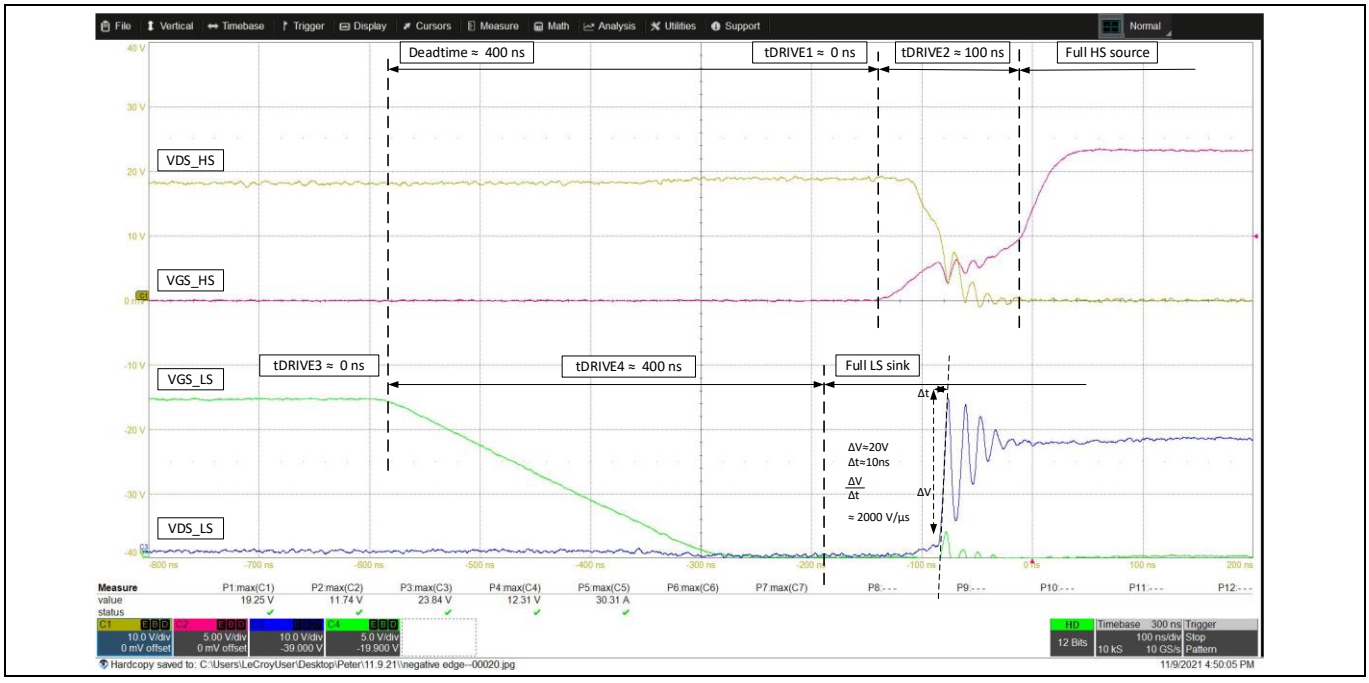


Figure 15 Example $V_{DS(LS)}$ switch-on transient shown in blue

This will be discussed in more detail.

2.2.2 Switch-off transient

Switch-off voltage transients appear between the drain and source of the high-side MOSFET again due to package and trace inductances ($L_{package}$ and L_{PCB}) when large channel currents (I_D) are interrupted, since this current is commutated to the low-side body diode. The worst-case condition is at the highest current, which would normally occur under a motor stall condition. If the transient is sufficiently high to exceed the MOSFET-rated BV_{DSS}, it is likely to cause the MOSFET to avalanche, which can lead to device damage and premature failure.

The peak amplitude of this transient is determined by these inductances and how rapidly the current in the device is switched off, according to:

$$V_{DS} = (L_{package} + L_{PCB}) \cdot {}^{di_{DS}}/_{dt} \quad [1]$$

Where V_{DS} refers to the voltage seen at the MOSFET die inside the package. This explains why a low-inductance SMD package is preferable to a high-inductance leaded package, since $L_{package}$ will be much lower. Since it is only possible to measure the external drain and source connections of the MOSFET, the designer should allow for package inductance and leave a safety margin of at least 50 percent between the peak transient voltage and the device-rated BV_{DSS}. Measurements should be made using a differential oscilloscope probe with a bandwidth of at least 100 MHz.

The yellow waveform shown in the oscilloscope screen capture in **Figure 16** is a measurement of the high-side MOSFET V_{DS} measured at the device terminals when this device is being switched off. The switch-off transient can be observed, which in this case is due to PCB trace inductances. In this example, a 40 V rated MOSFET is used in a PQFN 5x6 (SuperSO8) package with very low inductance. It can be seen that the peak voltage at switch-off reaches 27 V. However, this was measured at full load not under a stall condition, in which case the peak would be expected to be several volts higher.

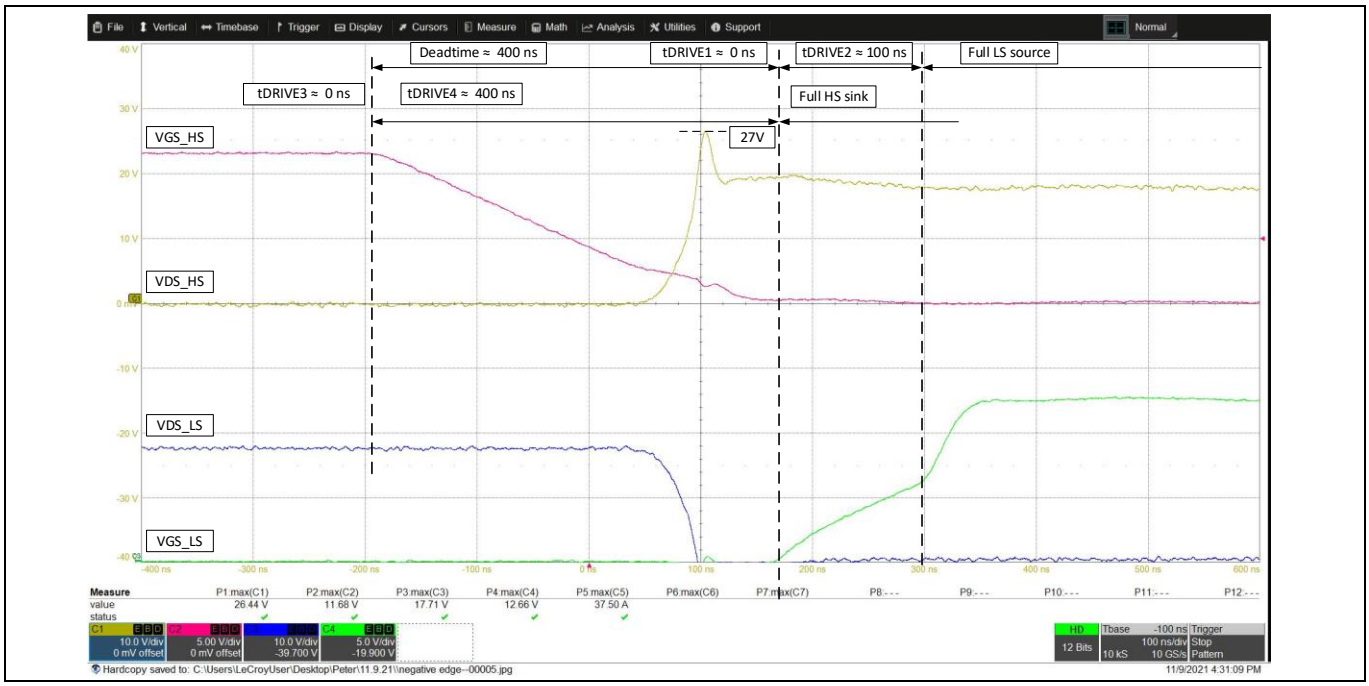


Figure 16 Example $V_{DS(HS)}$ switch-off transient shown in yellow

Since the transient is dependent on di_D/dt, it is possible to reduce it if necessary by slowing down the switch-off transition by reducing the gate drive sink current. This can be done while the inverter is running with 6EDL71x1 series drivers using the motor control GUI. However, care should be taken when making such on-the-fly adjustments to gate driver settings. In some cases it will still be necessary to add series resistor-capacitor snubber networks between the drain and source of each MOSFET; however, this should be avoided if possible since it adds to switching losses.

2.2.3 Configuration of the gate driver

2.2.3.1 Gate drive current and timing

The designer is able to configure the 6EDL71x1 gate driver currents and timing with the following parameters via SPI-accessible registers:

Table 2 Gate drive parameters[1]

Parameter	Description	Minimum	Maximum
I_{HS_SRC}	Source current value for switching on high-side MOSFETs	10 mA	1.5 A
I_{HS_SINK}	Sink current value for switching off high-side MOSFETs	10 mA	1.5 A
I_{LS_SRC}	Current value for switching on low-side MOSFETs	10 mA	1.5 A
I_{LS_SINK}	Current value for switching off low-side MOSFETs	10 mA	1.5 A
I_{PRE_SRC}	Pre-charge current value for switching on both high- and low-side	10 mA	1.5 A
I_{PRE_SNK}	Pre-(dis)charge current value for switching off both high- and low-side	10 mA	1.5 A
T_{DRIVE1}	Amount of time that I_{PRE_SRC} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE2}	Amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high- and low-side drivers.	0 ns	2.55 µs
T_{DRIVE3}	Amount of time that I_{PRE_SNK} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE4}	Amount of time that I_{HS_SINK} and I_{LS_SINK} and are applied. Shared configuration between high- and low-side drivers.	0 ns	2.55 µs

When the input signal from the microcontroller transitions from low to high, the gate drive output first applies a constant current defined by the user-programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}, at the end of which the MOSFET gate voltage should have reached the threshold voltage $V_{GS(TH)}$. The next period of the gate switch-on sequence is defined by the parameter T_{DRIVE2}, which begins immediately after the completion of T_{DRIVE1}. The current applied during T_{DRIVE2} determines both dI_D/dt and dV_{DS}/dt of the MOSFETs, as it will supply the current to charge the Q_{SW} of the MOSFET being driven.

It is necessary to set the correct values for T_{DRIVE1} and T_{DRIVE2}, which are dependent on the values of I_{PRE_SRC} and I_{H,LS_SRC}, meaning that if the gate drive current settings are changed then T_{DRIVE1} and T_{DRIVE2} must be changed accordingly. Failure to do so will result in misalignment and incorrect switching!
In many cases the pre-charge is not necessary and therefore T_{DRIVE1} can be set to zero. This greatly simplifies the gate drive optimization for switch-on.

In the three-phase motor drive configuration, each half-bridge operates in continuous conduction mode with non-ZVS[2] switch-on of the high-side. ZVS normally occurs at the low-side since the phase current is already passing through the body diode. However, non-ZVS switch-on of the low-side can occur under some conditions. Once the T_{DRIVE2} period has elapsed, the gate driver applies full current (1.5 A) to ensure fastest full turn-on of the MOSFET by supplying the remaining charge required to raise V_{GS} to the programmed PVCC value ($Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)}$).

[1] Available current and time delay values are listed in section 8 “Register Map” of the 6EDL7141 datasheet [1].

[2] ZVS – zero voltage switching. Non-ZVS switch-on is also referred to as a “hard” switch-on.

A similar process takes place during the switch-off of the MOSFET, in which the parameters T_{DRIVE3} and T_{DRIVE4} determine the periods for which the programmed discharge currents are applied.

Note: ***When adjusting the slew rate to a desired value it is necessary to set the dead time to a suitable value greater than the sum of T_{DRIVE1} and T_{DRIVE2} for the low to high transition and T_{DRIVE3} and T_{DRIVE4} for the high to low transition, or whichever is greater if both dead times are equal. Dead time is set by the microcontroller when using 6PWM mode and by the 6EDL71x1 in 3PWM and 1PWM modes.***

Figure 18 shows in detail the V_{GS} charging and discharging transitions for a high-side MOSFET in one of the inverter phases during a typical non-ZVS turn-on and turn-off. The different charging and discharging phases of the MOSFET switch-on and switch-off are illustrated above. Thanks to the flexible timing structure provided by the 6EDL71x1 gate driver with its high $T_{DRIVE(X)}$ resolution and ability to set the current during each interval, the designer is able to configure and optimize the switch-on and switch-off operations without the need for any external gate drive components.

During the critical Miller plateau period in hard-switching transitions, the controlled gate drive currents enable control of the slew rate dV_{DS}/dt. This is accomplished by precise control of the gate drive currents during the periods T_{DRIVE2} (switch-on) and T_{DRIVE4} (switch-off), during which the charge Q_{SW} is injected or extracted from the gate while V_{DS} transitions. Higher currents can be used for fast charging and discharging of $Q_{GS(TH)}$ and Q_{OD}, since neither dI_D/dt nor dV_{DS}/dt are affected during these periods.

It is also an option to set T_{DRIVE3} to zero, which simplifies the gate drive optimization for switch-off.

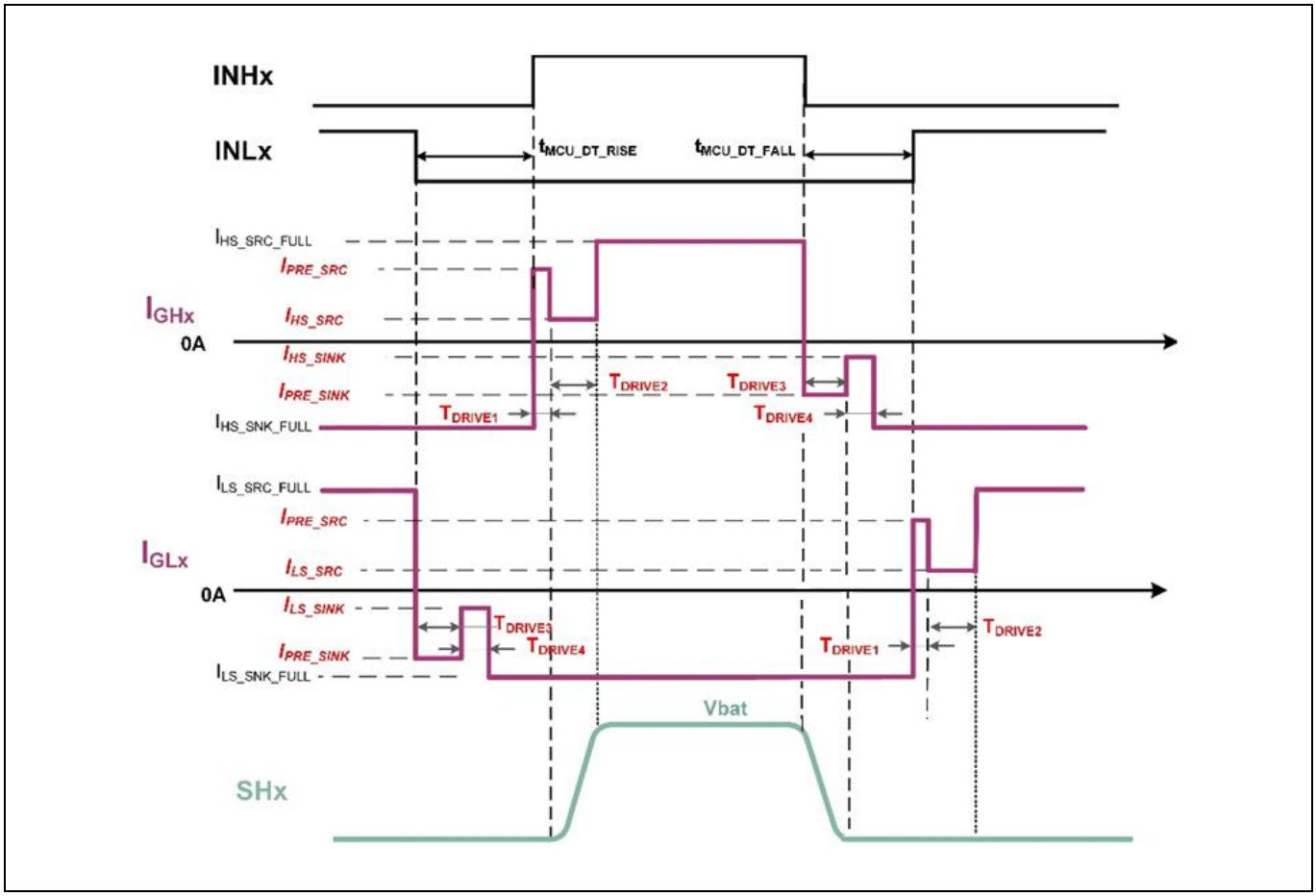


Figure 17 6EDL71x1 slew rate control for half-bridge

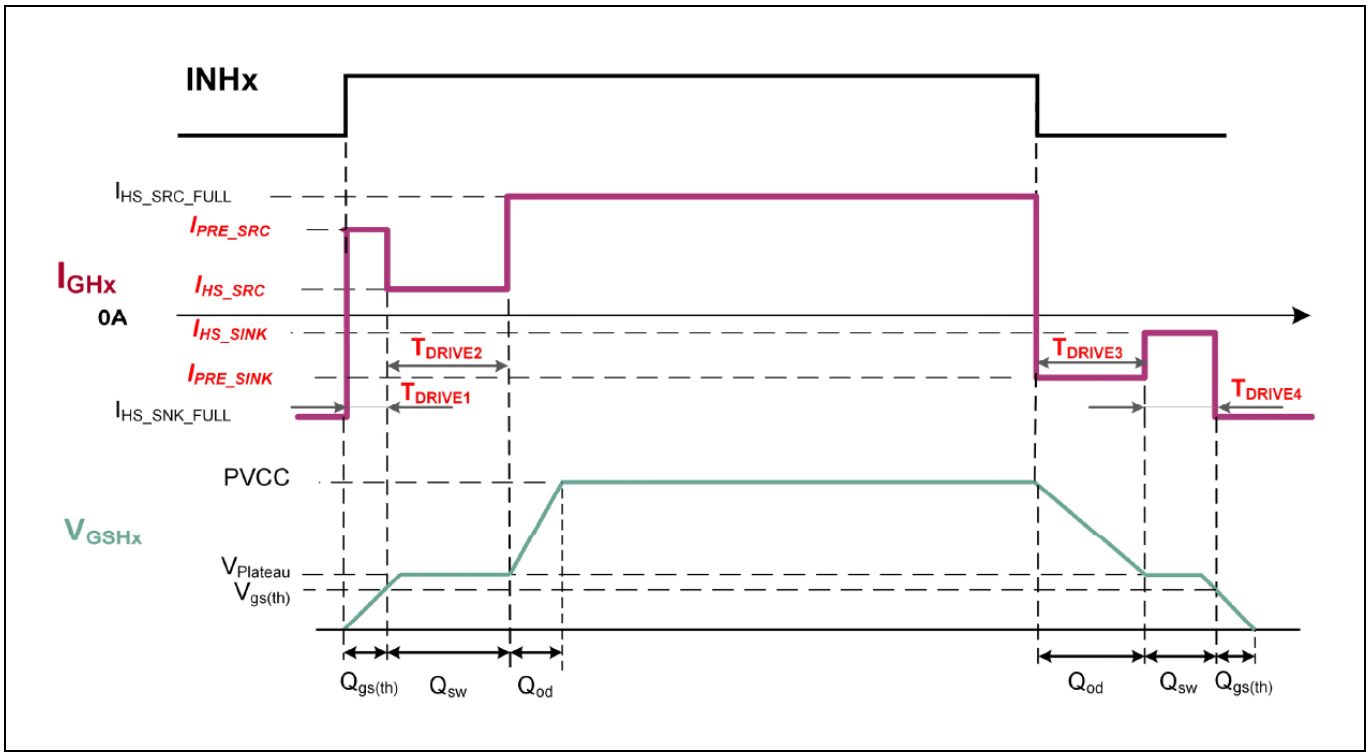


Figure 18 6EDL71x1 high-side gate drive profile

2.2.3.2 Gate pre-charging feature

The pre-charge function enables rapid charging of V_{GS} from zero to $V_{GS(TH)}$ during the initial stage of switch-on. This can be useful when driving MOSFETs with a high gate charge (Q_G) or when driving several MOSFETs in parallel with a large total Q_G. ***However, in most cases where a single MOSFET is used such as an OptiMOS™ device the gate charge is quite low and therefore the pre-charge feature is not necessary and should be disabled to simplify the gate drive optimization process. This is done by setting T_{DRIVE1} to zero.***

When using the pre-charge function, it is important to account for the tolerance of $V_{GS(TH)}$ by designing for the minimum value. The pre-charge current can be selected from seventeen available values. Sixteen of them are defined by $I_{PRE\_SRC/SNK}$ with an additional 1.5 A option, which is the maximum current capability of the gate driver. In cases where larger MOSFETs with relatively high gate charge are used, $Q_{G(TH)}$ during turn-on or Q_{OD} during turn-off may benefit from using the full gate driver capability. Full strength during the pre-charge may be selected via the GUI.

Where pre-charge is not used, T_{DRIVE1} can be set to zero, which results in the gate driver going immediately to the beginning of the T_{DRIVE2} period with its corresponding gate current setting. By doing this I_{HS,LS_SRC} is applied from the start of the switching period to the end of the Miller plateau.

The 6EDL71x1 series gate driver configurability enables optimization for both large and small MOSFETs covering different technologies such as OptiMOS™ or StrongIRFET™. This makes the design process much easier since the source current selected must determine the slew rate during switch-on. The selection of T_{DRIVE2} must allow a long enough period to cover the time from initial switch-on to the end of the Miller plateau. The duration of the plateau depends on the slew rate, which is determined by the source current. Therefore setting the values of T_{DRIVE2} and $I_{HS,LSSRC}$ is an iterative process since these values are interdependent. At the end of T_{DRIVE2} the source current will revert to 1.5 A, therefore it is important to ensure this does not occur prematurely during the Miller plateau period.

During the switch-off phase T_{DRIVE3} can also be set to zero to simplify the configuration of the switch-off. By doing this I_{HS,LS_SINK} is applied from the start of the switching period to the end of the Miller plateau.

If this option is taken, it is important to set T_{DRIVE4} to a period long enough to discharge V_{GS} from its maximum value down to the Miller plateau voltage and then pass through the full duration of the plateau. If T_{DRIVE4} is too short then the full 1.5 A sink current will be applied while the switch-off transition is still occurring. This is very undesirable as it can produce a large V_{DS} switch-off transient that risks MOSFET avalanching under high-current conditions such as a motor stall. As before, the duration of the plateau depends on the slew rate, which is determined by the sink current. Therefore setting the values of T_{DRIVE4} and $I_{HS,LSSNK}$ is an iterative process since these values are interdependent.

For simplicity, T_{DRIVE1} and/or T_{DRIVE3} should be set to zero, resulting in these intervals being skipped unless complex gate drive configuration is absolutely necessary for system optimization. *Alternatively T_{DRIVE2} and/or T_{DRIVE4} could be set to zero and I_{PRE_SRC} and I_{PRE_SINK} could be used as the gate drive currents. However, this approach does not permit different current settings for the high and low-side, though this is not a usual requirement.*

Note: ***When using the 6EDL7141 or IMD700/1A, when transitioning from the pre-charge current setting (at the end of t_{DRIVE1}) to the gate drive source current setting (at the start of t_{DRIVE2}) or from the pre-discharge current setting (t_{DRIVE3}) to the gate drive sink current setting (at the start of t_{DRIVE4}), a short period of reduced gate current can occur for 80 to 100 ns, before the new gate sink or source current value is established. This occurs only for certain current settings.***

To avoid interruptions in the gate drive, the designer may choose not to enable the pre-charge and pre-discharge functions as previously described. However, if these functions are necessary for the design, then current value combinations can be found where the delay does not occur.

Please refer to the 6EDL7141 datasheet section 3.2.2.1 [1]for further details.

This issue is not present in the 6EDL7151.

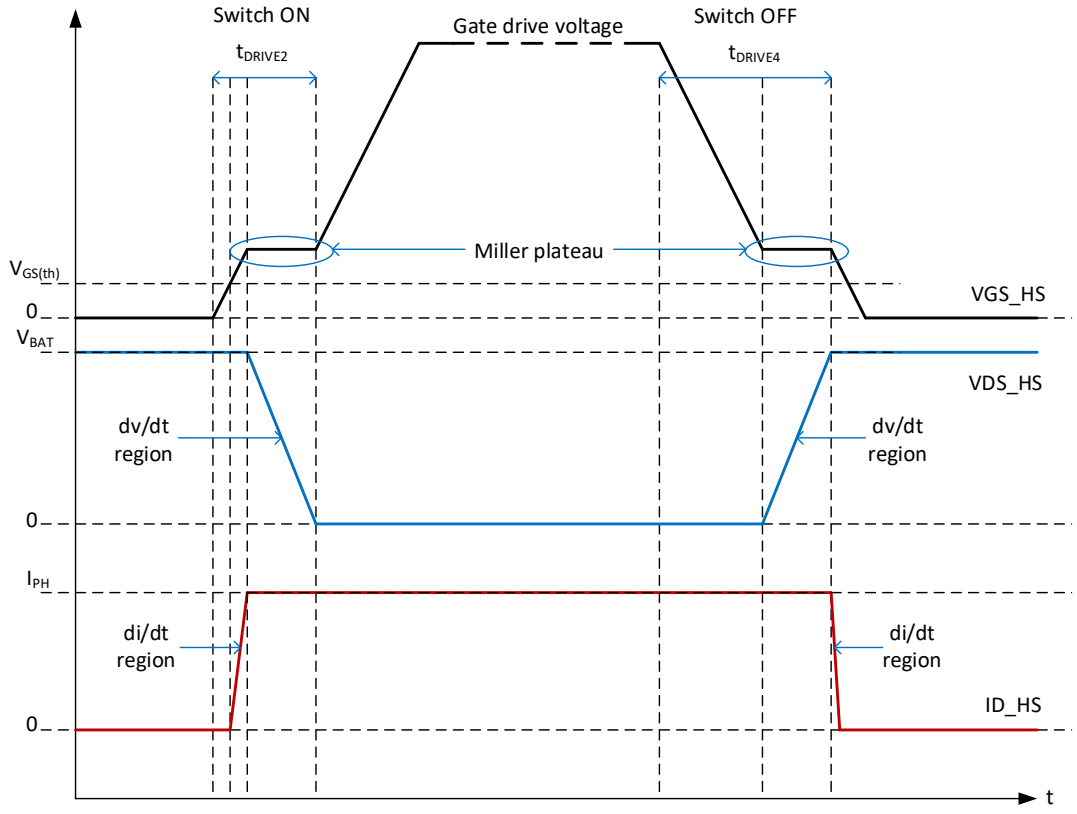
2.2.3.3 Gate drive voltage

The 6EDL71x1 offers the designer several driving voltage options to select from depending on the system requirements, allowing designers to adjust the MOSFET driving voltage (PVCC voltage) via SPI registers. The same-value PVCC applies to both high- and low-side charge pumps from the four possible values: 7 V, 10 V, 12 V, and 15 V. This is done by setting bitfield PVCC_SETPT via the GUI, where the default value is 12 V. Gate drive outputs include UVLO protection.

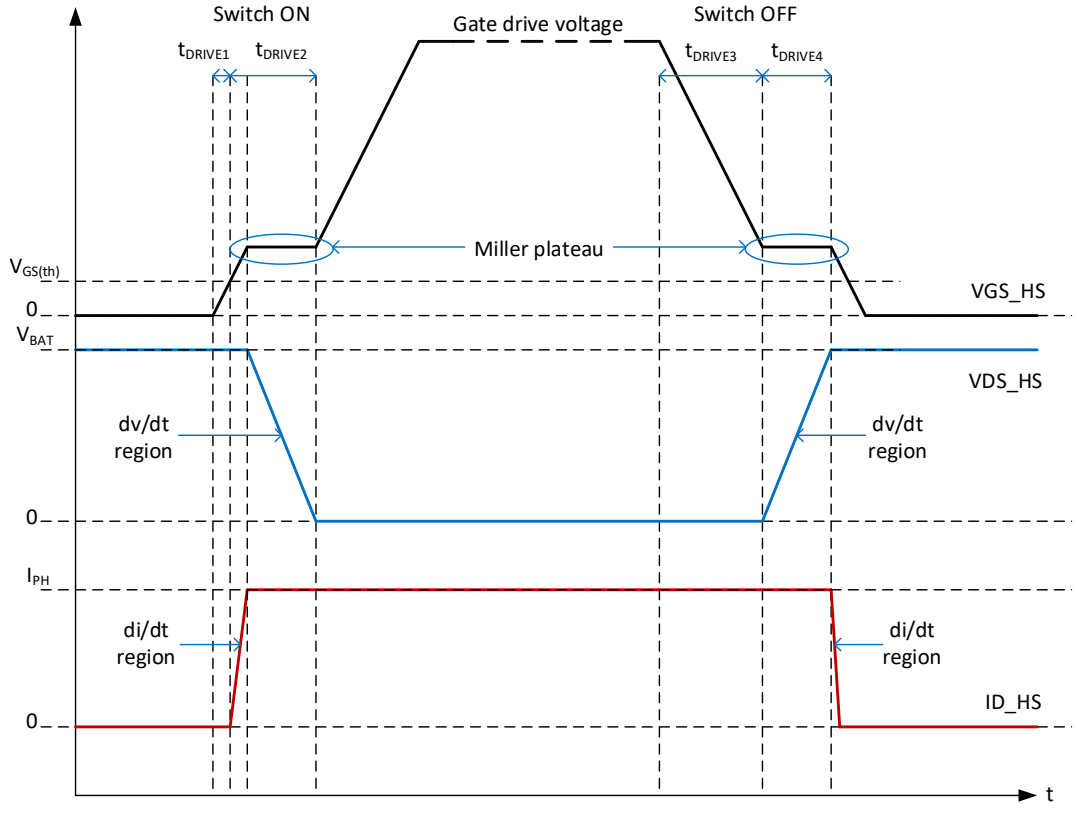
High-impedance MOSFET gate inputs in a motor drive inverter should never be left floating when gate drivers are not activated because electrical noise or static can cause gate voltage buildup. In some cases, such voltages can be high enough to pass the MOSFET gate turn-on threshold, partially switching on the device. If a high- and low-side MOSFET in an inverter phase were to switch on at the same time, the resulting high current could destroy the devices. In order to prevent this, it is common to add weak pull-down resistors between the gates and sources of each MOSFET. The 6EDL71x1 avoids the need for these external resistors by integrating the following functions into its gate driver outputs:

- Weak pull-down: A weak pull-down (RGS_PD_WEAK) is always connected between gate and source of each gate driver output. This ensures a weak pull-down during states where the gate driver is off, either because EN_RV is turned off or because the device is fully off (CE off).
- Strong pull-down: During gate driver off periods, if the external gate-to-source voltage increases for any reason, a strong pull-down (RGD_PD_STRONG) is activated, ensuring a tight pull-down to prevent any partial turn-on.

Figure 19 shows an idealized representation of hard-switching waveforms to illustrate the gate drive operation and to identify the di/dt and dv/dt transitions that occur. These waveforms do not account for MOSFET output capacitances, parasitic inductances or diode recovery that would be present in a practical motor drive inverter; however, they serve to show the timing scheme used in the 6EDL71x1 gate drivers.



(a) Pre-charge and discharge disabled



(b) Pre-charge and discharge disabled

Figure 19 Idealized hard-switching waveforms and 6EDL71x1 gate drive timing

3 Motor drive inverter design

3.1 Defining the system parameters

The inverter power stage design requires careful consideration of the critical parameters listed here, which include:

- Battery voltage (minimum and maximum)
- Battery capacity and impedance
- Maximum continuous and peak power requirements
- Maximum continuous and peak motor phase currents (it is essential to allow for the high current that passes through the MOSFETs during a stall condition for a limited time)
- Control method (this is typically a speed-regulated control loop)
- Commutation method; this could be six-step trapezoidal or sinusoidal
- Switching frequency
- Thermal management, heatsinking
- Form factor
- Motor winding inductance
- Motor winding resistance

$$I_{stall} = \frac{V_{ab}}{2.R} = \frac{V_{bat}}{2.R} \quad [2]$$

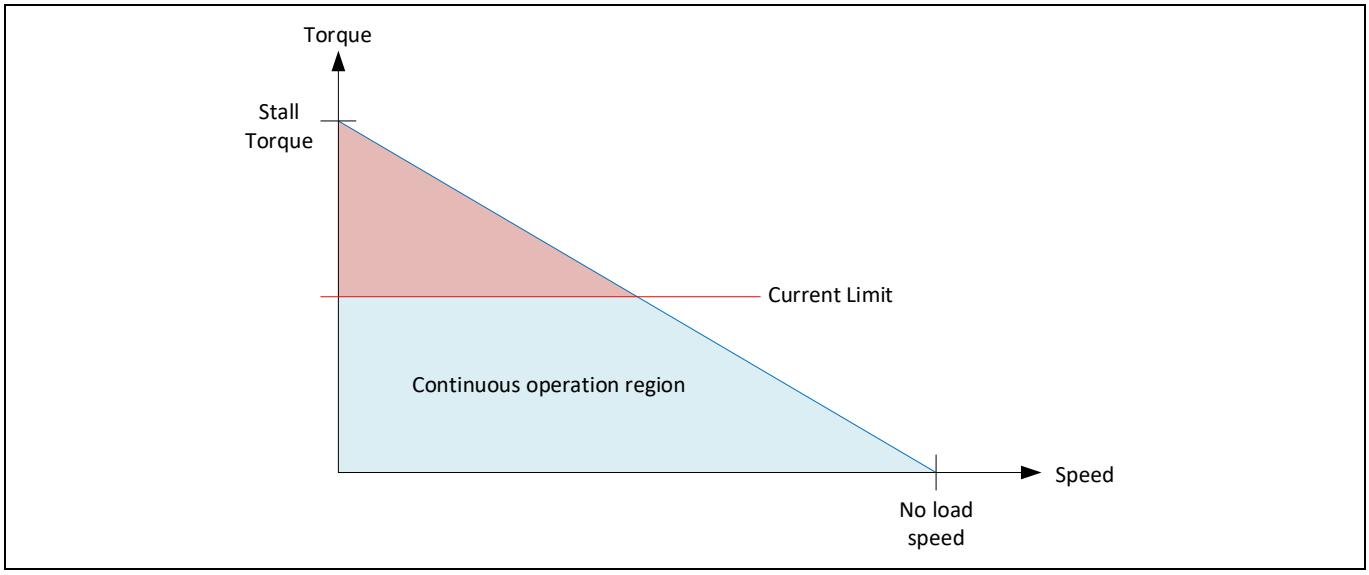


Figure 20 Stall current

3.2 MOSFET selection

The following table lists the MOSFET parameters and design criteria that should be considered when selecting the device to use in a battery-powered BLDC motor drive inverter design.

Table 3 MOSFET parameters for motor drive inverter

Parameters	Quantity	Design criteria
Breakdown voltage	BV_{DSS}	Margin for transients
On-resistance	$R_{DS(on)}$	V_{GS} greater than or equal to 10 V
Maximum continuous current	$I_{D(MAX)}$	Temperature derating
Maximum peak current	$I_{D(PK)}$	Stall current
Gate charges	Q_G	Q_{GD}/Q_{GS} = 0.5 to 0.8, $Q_{GD}/Q_{GS(TH)}$ less than 1.0
Gate capacitance	C_{GS}, C_{GD}, C_{DS}	C_{GS}/C_{GD}
Gate resistance (internal)	R_G	High R_G can cause C.dv/dt
Safe operating area		Switching speed
Body diode recovery	t_{rr}	Lower value preferred
Body diode recovery charge	Q_{RR}	Lower value preferred
Body diode softness factor	RRSF	t_S/t_F greater than 0.8 (t_B/t_A)
Package		Parasitic resistances and inductances

3.2.1 Breakdown voltage BV_{DSS}

The first parameter to consider is BV_{DSS}. As a general rule, consider the highest rated input voltage and add at least 50 percent safety margin.

For example, a system is designed for an 18 V battery, which is rated to operate at a maximum input of 24 V. In this case a 40 V rated MOSFET such as the BSC007N04LS6 would be suitable.

3.2.2 On-resistance $R_{DS(on)}$

Next the $R_{DS(on)}$ should be considered. Best-in-class MOSFETs (i.e., the lowest $R_{DS(on)}$ available in a particular voltage and package) are generally used in battery-powered BLDC motor drive inverters. If necessary more than one device may be connected in parallel in each switch location to reduce conduction losses to an acceptable level. Calculation of total MOSFET losses is a moderately complex process, which is dependent on the type of commutation scheme used and the switching frequency. Both conduction and switching losses need to be evaluated. Once an estimate of device losses has been determined, the desired $R_{DS(on)}$ can be found based on the amount of conduction losses and bearing in mind that this should be increased by 30 percent to account for a die temperature operating at 100°C.

3.2.3 Maximum drain current $I_{D(MAX)}$

Next the maximum drain current rating should be chosen to exceed the stall current, which can be calculated from equation [1]. This may be a pulsed value $I_{D(PK)}$ if the inverter is designed to shut down within a certain time period when a stall current is detected. This protection feature is supported with the 6EDL71x1 driver. The continuous drain current rating $I_{D(MAX)}$ must exceed the maximum RMS current carried on the MOSFET with plenty of safety margin. It should be noted that different MOSFET manufacturers use different methods to specify the maximum current ratings of their devices, therefore designers should be wary of datasheets that claim very high current capabilities compared with devices in the similar packages with similar $R_{DS(on)}$ ratings.

3.2.4 Gate charge ratio

The ratio of Q_{GD} to Q_{GS} should be such that Q_{GD}/Q_{GS} falls between 0.5 and 0.8 so that the device will not be sensitive to induced turn-on caused by the C.dV_{DS}/dt effect during switch-on of the complementary device. This effect can produce unwanted losses due to shoot-through currents if both devices are partially switched on at the same time even for a brief period during switching. A lower R_G value is preferred as this also reduces the effect. At the same time devices with high Q_G are not preferred since they require more power to switch on and off and may require use of the 6EDL71x1 gate drive pre-charge function.

3.2.5 Safe operating area

The MOSFET safe operating area (SOA) should also be considered. This depends on the period of switching, which is the same as the Miller plateau period that occurs during the transition or “slew” of the switch node voltage from one bus to the other. The switching time is determined by the gate drive current, which is set by the gate driver and chosen as a tradeoff between fast switching to reduce switching losses and slower switching to reduce EMI and switching L.di/dt transients. Since the device current can be quite high during switching, it is necessary to ensure that the SOA limits are not exceeded.

3.2.6 Body diode recovery

Body diode recovery is also critical to switching losses and EMI. A faster body diode recovery translates to reduced switching losses at switch-on of the complementary device. However, the snappiness or softness of the body diode recovery determines how much EMI is produced. A softer body diode recovery is preferable. Slow body diode recovery MOSFETs are not suited to hard-switching applications such as motor drive inverters. The body diode voltage and current waveforms of the low-side MOSFET during the turn-off transition are shown in **Figure 20**.

During the period of the motor rotation where a positive current is flowing from a phase node to the motor winding after the low-side MOSFET switches off, its body diode is initially forward biased, carrying a positive current I_F. As soon as the gate-source drive pulse (V_{GS}) goes high to turn on the top-side MOSFET, the body diode turn-off process of the low-side MOSFET is initiated. The diode current reduces at a constant slope (di/dt) to zero and then reverses its direction. The negative current, also known as reverse recovery current (I_{rr}), finally reaches the negative peak (I_{RRM}) and then rises back up to zero. The reverse recovery process completes at this point and the body diode reaches its fully blocking state.

The ratio of t_F and t_S is used to quantify the softness of the body diode, RRSF = t_S/t_F.

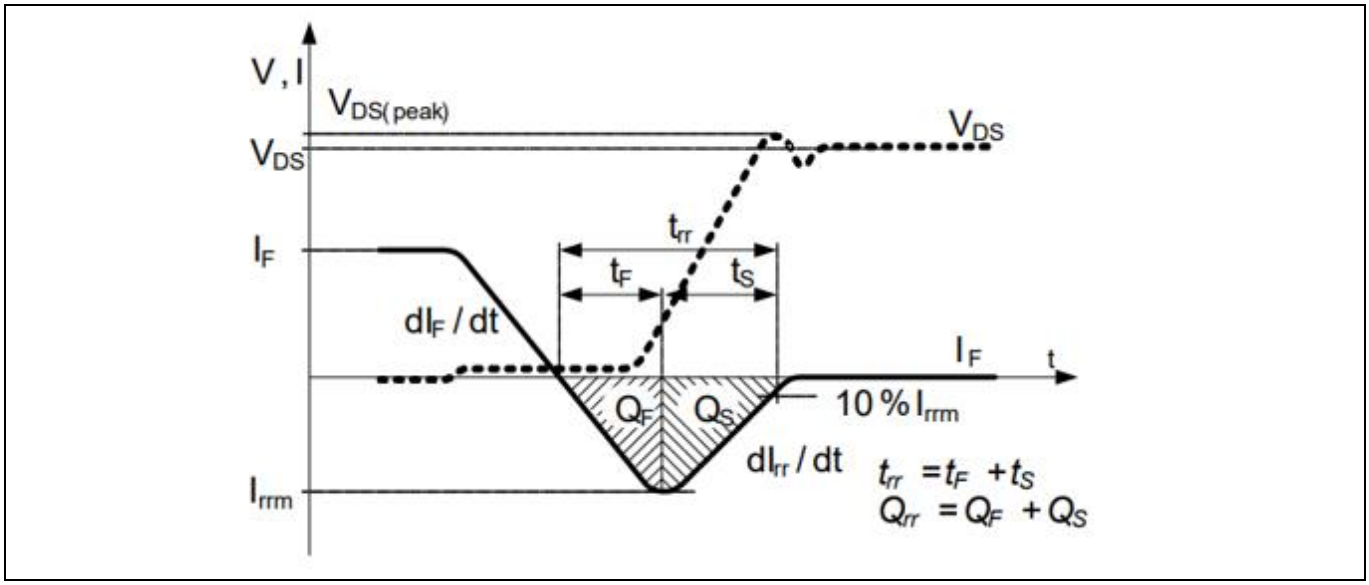


Figure 21 Body diode recovery waveforms

3.2.7 Package selection

Finally, the choice of MOSFET package is critical to the design. Surface-mounted flat packages such as QFN or DirectFET have much lower parasitic inductances compared to leaded packages such as TO-220. Lower inductance reduces losses and ringing, which produces EMI. Flat SMD packages may be used with bottom-side, top-side or dual-side cooling, i.e., with a heatsink mounted under the PCB, on top of the devices or both together. Special packages are available for top-side cooling which have exposed metal on the top. In this case, as with bottom-side cooling, a suitable thermal insulation material (TIM) must be placed between the MOSFETs and the heatsink.

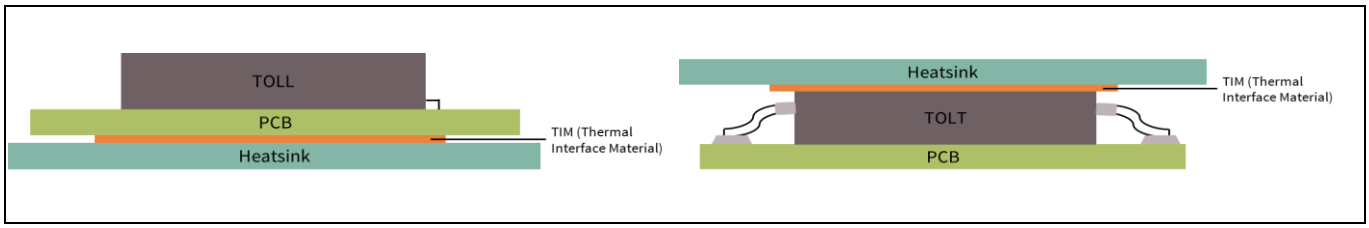


Figure 22 Bottom-side (left) and top-side (right) cooling of SMD power MOSFETs (TOLL and TOLT packages)

Forced air cooling may or may not be used, depending on the application and layout of the design.

3.3 Gate drive optimization

3.3.1 Selecting the gate drive voltage

As mentioned, the 6EDL71x1 gate drivers can be configured for four gate drive voltage options: 7 V, 10 V, 12 V, and 15 V. The choice of gate drive voltage depends on the device $R_{DS(on)}$ vs. V_{GS} characteristics. In **Figure 23**(taken from the BSC007N04LS6 datasheet), $R_{DS(on)}$ vs. I_D curves are shown for several V_{GS} values. It can be seen that at 10 V the $R_{DS(on)}$ is slightly lower than it would be at 7 V. In this case a 10 V gate drive is sufficient to achieve low $R_{DS(on)}$. This would be true for most standard- and logic-level devices, but in some cases 12 V may be necessary for optimization.

MOSFETs may have standard- or logic-level gate thresholds, where $V_{GS(TH)}$ for logic-level devices such as the BSC007N04LS6 is significantly lower than for standard-level parts. As a consequence, for a given gate-to-source voltage, a logic-level MOSFET would produce a lower $R_{DS(on)}$ than a normal-level MOSFET.

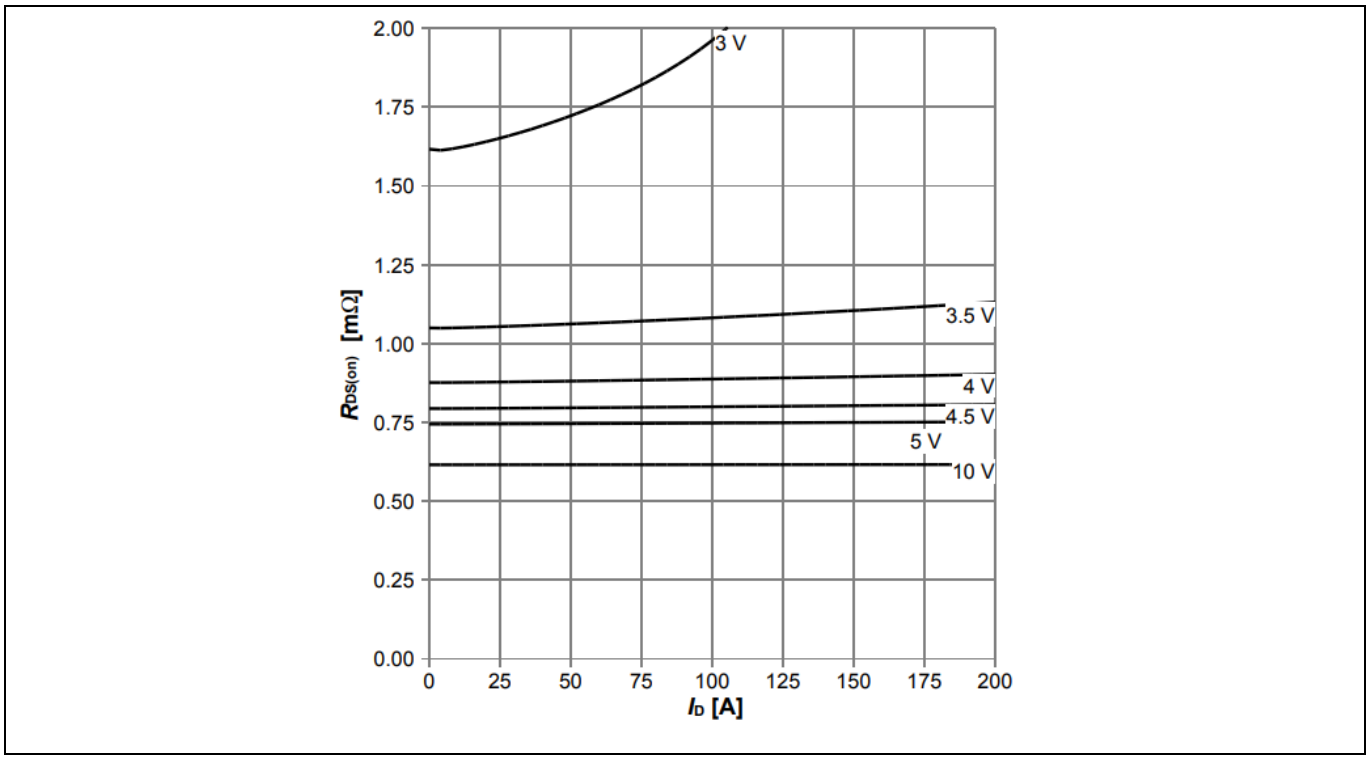


Figure 23 BSC007N04LS6 example $R_{DS(on)}$ vs. V_{GS} characteristic

Note: ***However, it is important to consider that logic-level devices are more prone to induced turn-on caused by C.dv/dt during high-side switch-on due to their lower $V_{GS(TH)}$. It is therefore safer to use standard-level devices in motor drive designs.***

3.3.2 Gate switch-on configuration procedure

The following graph outlines the charging phases of a BSC007N04LS6 device during the non-ZVS switch-on process. This will be used as an example for setting the gate drive parameters of the 6EDL71x1. The BPA motor control GUI tool version 1.3 and above includes a MOSFET tuning function, which is able to calculate the gate drive parameters for a specified device under a given set of conditions. This will be discussed further.

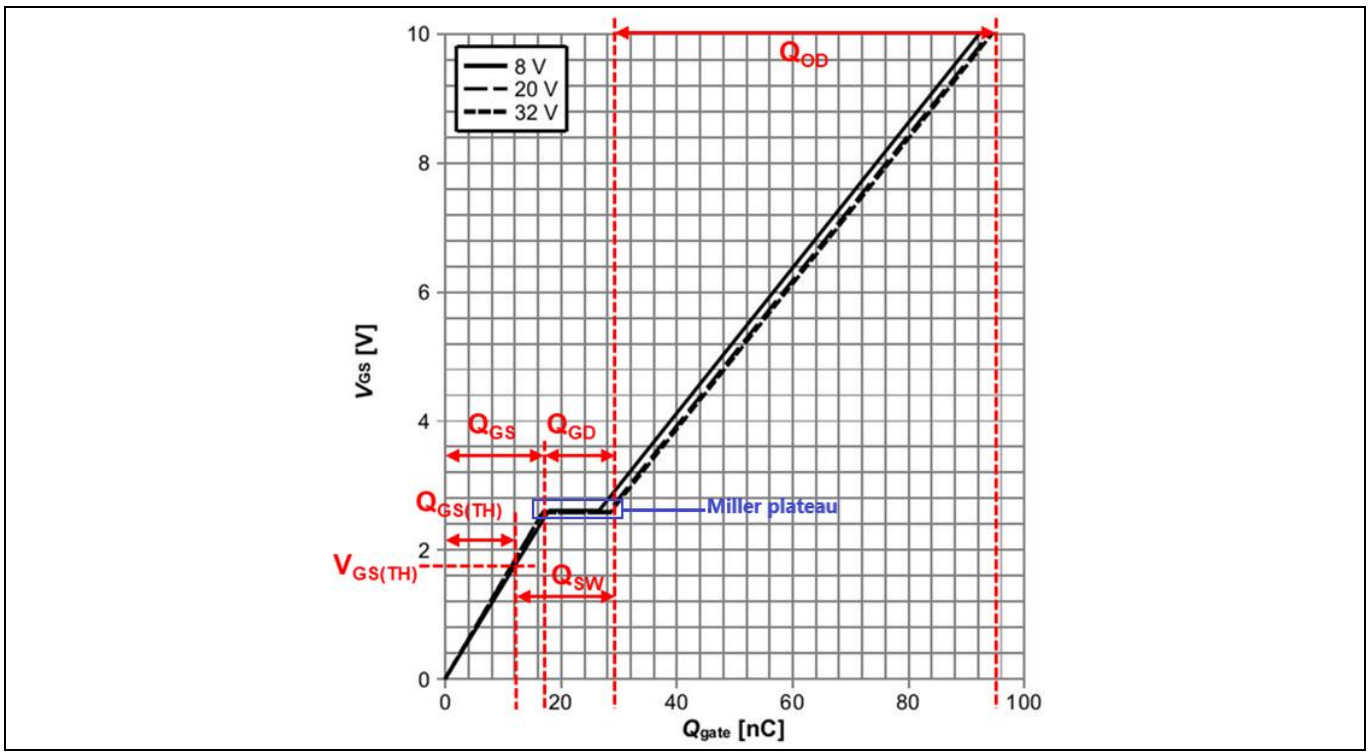


Figure 24 BSC007N04LS6 gate charge graph

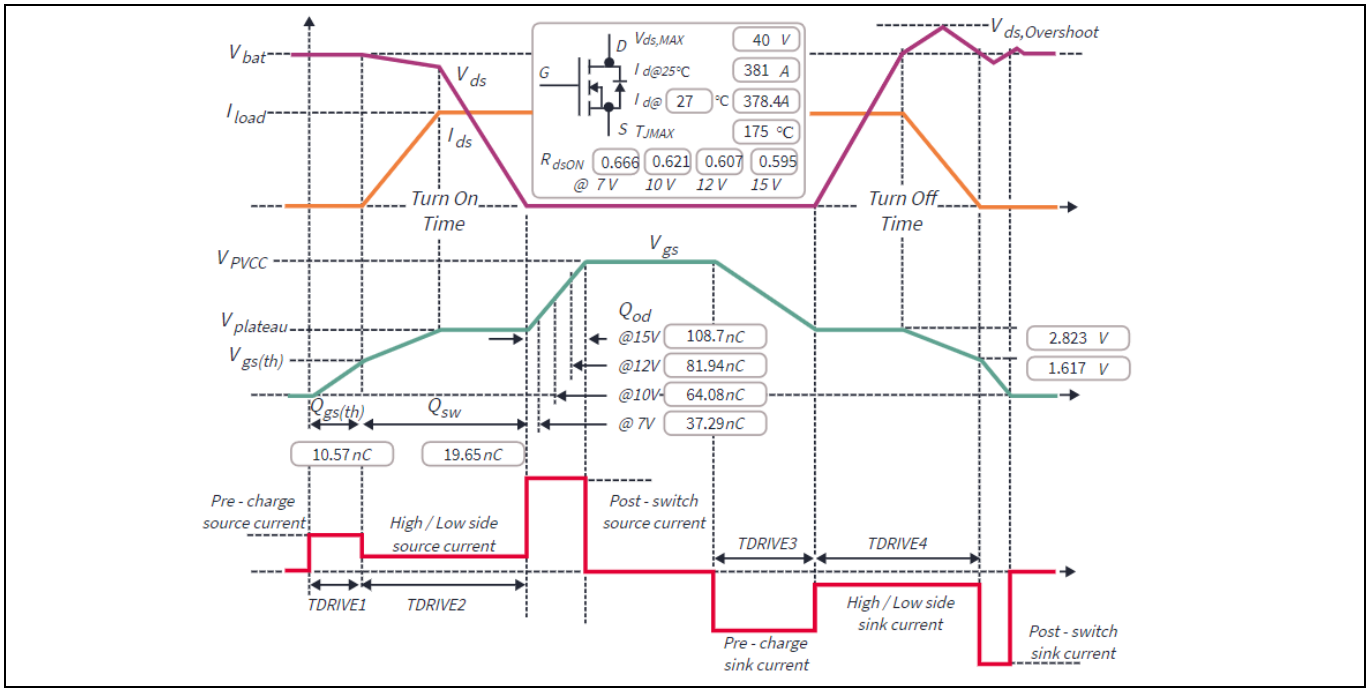


Figure 25 BSC007N04LS6 turn-on and turn-off process

The procedure for setting the gate drive parameters is as follows:

1. Determine the gate drive voltage setting.

   It can be seen from **Figure 23** that the BSC007N04LS6 fully reaches a low $R_{DS(on)}$ value with a with 10 V gate drive voltage. Therefore, in this example, PVCC is set to 10 V.

2. Obtain $Q_{GS(TH)}$ and Q_{GS} from the graph or MOSFET datasheet. For the BSC007N04LS6 $Q_{GS(TH)}$ = 10.3 nC and Q_{GS} = 17 nC, specified at V_{DS} = 20 V and I_D = 50 A. In this example 18 V battery voltage is close to 20 V and the current is in the same range as the application so these values can be used. For a Q_{GS} less than 50 nC the pre-charge function can be omitted, in which caseT_{DRIVE1} should be set to zero. The value of I_{PRE_SRC} can be ignored.

3. For a single MOSFET or two or more parallel MOSFETs with total Q_{GS} greater than 50 nC, determine T_{DRIVE1} from a selected I_{PRE_SRC} value chosen based on a suitable value of T_{DRIVE1}, which can be selected from the options available. Obtain Q_{GS} from the graph or MOSFET datasheet.

   $$I_{PRE\_SRC} \leq \frac{Q_{GS(TH)}}{t_{DRIVE1}} \quad [3]$$

   The value is rounded down to the nearest available value. This is so that during the T_{DRIVE1} period the gate will be charged almost to $V_{GS(TH)}$ (the start of the Q_{SW} period) but should not charge above the threshold. This is so that T_{DRIVE1} ends before the start of the di/dt period shown in **Figure 19**. Another strategy is to use the pre-charge function as a di/dt function instead, which is done by extending t_{DRIVE1} so that I_{PRE_SRC} continues driving the gate during the di/dt period to the start of the Miller plateau, in which case:

   $$t_{DRIVE1} \geq \frac{Q_{GS}}{I_{PRE\_SRC}} \quad [4]$$

   By doing this, di/dt could be controlled independently from dv/dt but the pre-charge function is no longer available.

4. **The next and most important step is to determine T_{DRIVE2} and $I_{\_SRC}$ based on the desired slew rate.** For most cases I_{LS_SRC} can be set to the same value II_{HS_SRC}.

   Obtain Q_{SW} from the graph or MOSFET datasheet. For the BSC007N04LS6 Q_{SW} = 18 nC.

   (Where $Q_{SW} = Q_{GS2} + Q_{GD}$, in this example Q_{GD} = 11.2 nC and $Q_{GS2} = Q_{GS} - Q_{G(TH)}$ = 17 nC – 10.3 nC = 6.7 nC.)

   First consider the desired turn-on time T_{ON} referring to **Figure 25**, where:

   $$T_{ON} = T_{ON(\frac{di}{dt})} + T_{ON(\frac{dv}{dt})} \quad [5]$$

   $T_{ON(dv/dt)}$ can be calculated since the target voltage slew rate dv_{DS}/dt and bus voltage are already known, therefore:

   $$T_{ON(\frac{dv}{dt})} = V_{BAT(MAX)} \Big/ \left(\frac{dV_{DS}}{dt}\right) \quad [6]$$

   and $T_{ON(di/dt)}$ can be calculated as follows:

   $$T_{ON(\frac{di}{dt})} = \frac{Q_{GS2}}{I_{HS\_SRC}} \quad [7]$$

Knowing T_{ON}, t_{DRIVE2} can be calculated by adding a 10 percent margin:

$$t_{DRIVE2} \geq 1.1 \cdot T_{ON} \quad [8]$$

This is to ensure that the t_{DRIVE2} period will extend beyond the end of the turn-on time.

The result is then used to calculate the gate drive source current required to complete the V_{DS} switching transition by reaching the end of the Miller plateau.

5. During the final stage, Q_{OD} is charged, bringing V_{GS} from $V_{PLATEAU}$ to 10 V as quickly as possible.

$$Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)} \quad [9]$$

For the BSC007N04LS6:

$$Q_{OD} = 94\,nC - 18\,nC - 10.3\,nC = 65.7\,nC$$

6. The maximum gate drive source current of 1.5 A is applied during this period. The time required can be estimated by:

$$t_{OD} \approx \frac{Q_{OD}}{I_{GD\_SRC\_PEAK}} \quad [10]$$

$$t_{OD} \approx \frac{65.7\,nC}{1.5\,A} = 43.8\,ns$$

It should be noted that as V_{GS} charges to the full voltage the gate driver will no longer sustain 1.5 A source current though the gate will remain pulled up to the selected drive voltage.

3.3.3 Gate switch-off configuration procedure

1. During the first part of switch-off Q_{OD} is discharged to bring V_{GS} from the gate drive voltage, 10 V in this example, to $V_{PLATEAU}$, which occurs during the period T_{DRIVE3} with the gate sink current I_{PRE_SINK} (I_{PRE_SINK} can be thought of as a pre-discharge current where I_{PRE_SRC} is the pre-charge current).
To select the values, first obtain Q_{OD} from the graph or MOSFET datasheet for the selected gate drive voltage. The discharge of Q_{OD} should happen quite rapidly to minimize the overall switching time, which is desirable for achieving the shortest safe amount of dead time. After choosing a suitable T_{DRIVE3} value, I_{PRE_SINK} can be calculated as:

$$I_{PRE\_SINK} \leq \frac{Q_{OD}}{T_{DRIVE3}} \quad [11]$$

The selected value of I_{PRE_SINK} must be rounded down to the closest available value to ensure that during the T_{DRIVE3} period Q_{OD} will not be fully discharged and the Miller region will not be entered. This is very important to avoid unintended fast switch-off resulting in a large V_{DS} transient. If necessary, a lower value of I_{PRE_SINK} should be chosen to guarantee this. For simplification, it is also possible to omit this stage by setting T_{DRIVE3} to zero, which simplifies optimization. However, this approach would extend the Q_{OD} discharge time and therefore a longer dead time would be required.

The next and most important step is to determine T_{DRIVE4} and I_{HS,LS_SNK} based on the target slew rate.

$$T_{OFF} = T_{OFF(\frac{dv}{dt})} + T_{OFF(\frac{di}{dt})} \quad [12]$$

$T_{OFF(dv/dt)}$ can be calculated as follows based on the same target value used previously (unless a different value is needed):

$$T_{OFF(\frac{dv}{dt})} = {V_{BAT(MAX)}}\Big/{\left(\frac{dV_{DS}}{dt}\right)} \quad [13]$$

$T_{OFF(di/dt)}$ can be calculated as follows based on a selected value of I_{HS_SINK}:

$$T_{di/dt} = \frac{Q_{GS2}}{I_{HS\_SINK}} \quad [14]$$

However, this value is useful only for determining the value of T_{OFF} but not for calculating di/dt. This is because the current is already diverted to the low-side MOSFET before this point.

With the calculated result for T_{OFF}, t_{DRIVE4} can be determined by adding a 10 percent margin:

$$t_{DRIVE4} = 1.1 \cdot T_{OFF} \quad [15]$$

This is to ensure that the t_{DRIVE4} period will extend beyond the end of the turn-off time.

For the sake of simplicity it is common for the same slew rate to be selected for switch-off as for switch-on, $T_{DRIVE4} = T_{DRIVE2}$ and $I_{HS,LS\_SINK} = I_{HS,LS\_SRC}$. However, designers have the option to select different switch-on and switch-off slew rates with the 6EDL71x1, in which case $T_{DRIVE4} \neq T_{DRIVE2}$ and $I_{HS,LS\_SINK} \neq I_{HS,LS\_SRC}$.

2. During the final stage, the remaining gate charge Q_{GS} is discharged, bringing V_{GS} to zero as rapidly as possible. The remaining switch-off time is calculated from the maximum gate drive sink current of 1.5 A applied during this period.

   The time required can be calculated by:

$$t_{TH} = \frac{Q_{GS}}{I_{GD\_SINK\_PEAK}} \quad [16]$$

As V_{GS} falls to zero the sink current will drop to zero, but the strong pull-down will remain while the MOSFET is off, which helps to prevent induced turn-on caused by $C_{GD}.dv_{GS}/dt$.

3.3.4 Setting the dead time

Calculate the total switch-on and switch-off times based on the previously derived values as follows:

$$T_{DRIVE(ON)} = T_{DRIVE1} + T_{DRIVE2} + T_{OD} \quad [17]$$

$$T_{DRIVE(OFF)} = T_{DRIVE3} + T_{DRIVE4} + T_{TH} \quad [18]$$

To allow for tolerances and avoid any possibility of shoot-through, it is recommended to add at least 20 percent to the calculated value:

The dead times T_{DT-} and T_{DT+} should be set to be greater than $T_{DRIVE(ON)}$ and $T_{DRIVE(OFF)}$ + 20 percent:

$$T_{DT-} \geq T_{DRIVE(ON)} \times 1.2 \quad [19]$$

$$T_{DT+} \geq T_{DRIVE(OFF)} \times 1.2 \quad [20]$$

Dead time values are rounded up to the next highest available value. The rising and falling dead times (T_{DT+} and T_{DT-}) are normally both set to this or a higher value. Generally, the highest of the two dead

times (usually T_{DT-}) is chosen for both dead time settings. Keeping the dead time as short as possible reduces the peak current required to deliver a given power to the output; however, the dead time must be long enough to fully cover the switching operations and prevent the possibility of cross-conduction.

In 6PWM mode the dead time is set in the microcontroller instead of in the 6EDL71x1!

In some cases, designers may need to add series RC snubber networks between the drain and source of the MOSFETs to reduce ringing and EMI. This can usually be avoided when using the 6EDL71x1 gate driver with correctly optimized gate drive settings. The addition of a snubber adds to switching losses and should therefore be avoided whenever possible!

In cases where snubbers have been included, it should not be necessary to further increase the dead time since the effect on dV_{DS}/dt is minimal.

3.3.5 Minimum pulse widths

The PWM pulses that control the gate drive outputs produced by the 6EDL71x1 gate driver are generated in the system microcontroller as shown in **Figure 3**. **Section 1.2.1** describes the different PWM encoding options supported and notes the necessity to limit the pulse width to a minimum time value no shorter than $T_{DRIVE(ON)}$. This is required to allow sufficient time for the gate drive pulses to rise from zero to their defined maximum value for V_{GS} as determined by V_{PVCC}, shown in **Figure 25**. It is very important that the system firmware PWM outputs are configured such that generated pulse always exceeds the minimum pulse width $T_{PWM(MIN)}$. The result of a shorter pulse would be that V_{GS} pulses would not reach the full MOSFET turn-on voltage and the MOSFETs would then only partially switch on, either remaining in the saturation region or with high on-resistance. In either case this would lead to unwanted power losses. The $T_{PWM(MIN)}$ value can be determined from the time periods defined in the previous section using the following formula:

$$T_{DRIVE(MIN)} \geq T_{DRIVE1} + T_{DRIVE2} + T_{OD} \quad [21]$$

3.3.6 Procedure for tuning the gate drive parameters on the bench

1. Calculate the values using the procedure described in the previous section or use the BPA motor control GUI MOSFET tuning tool to determine the values (this is described later).
2. Set a longer dead time than the one calculated of at least 1 µs for both rising and falling transitions. This will be reduced to the minimum safe value once the T_{DRIVE} and gate drive current settings have been finalized.
3. Download the parameters into the 6EDL71x1 and microcontroller[1] (if applicable) using the BPA motor control GUI tool “write parameters” function. This can be done using an onboard programmer/debugger. If this is not available, an external XMC_LINK may be used.
4. In cases where a different microcontroller is used, which is not compatible with Infineon programmers/debuggers, the 6EDL71x1 driver may be configured by means of the 6EDL_SPI_LINK configuration board.[2]

[1] This can be done only when the board is using a compatible XMC™ series microcontroller.

[2] Please note that values stored in 6EDL71x1 RAM will be lost when the board is powered down.

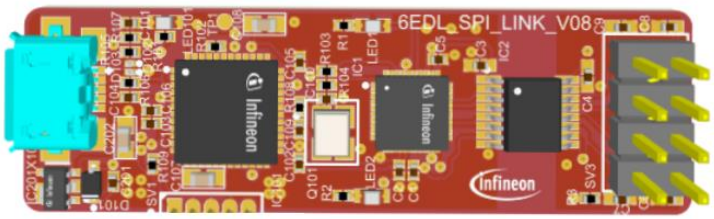


Figure 26 6EDL_SPI_LINK configuration USB adapter

5. Create a suitable project in the GUI for the design being worked on and enter the values of: T_{DRIVE1}, T_{DRIVE2}, T_{DRIVE3}, T_{DRIVE4}, I_{PRE_SRC}, I_{PRE_SINK}, I_{HS,LS_SINK}, I_{HS,LS_SRC}, calculated using the procedure above.
6. Save the project (this is saved as a *.6EDL file).
7. Use the “write device” command to configure the 6EDL71x1 with the values provided in the project.
8. Operate the board at maximum specified battery voltage and monitor the high- and low-side V_{GS} and V_{DS} waveforms using differential probes. If possible, monitor the MOSFET case temperatures and power down the board if they exceed 100°C. If this happens re-evaluate the device selection and gate drive settings and make sure the dead time has been set to a period long enough to avoid cross-conduction and shoot-through.
9. Increase to maximum load[1] and observe the V_{DS} transient peak values. Ensure that there is sufficient headroom between the peak voltage and the MOSFET BV_{DSS} rating.
10. If necessary, reduce the values of I_{HS,LS_SINK} to reduce V_{DS} transient peaks.
11. Determine whether the hard-switching dv/dt slew rates are as expected according to the target value. If not, adjust gate drive source and sink currents via the GUI as necessary to ensure correct switching transitions. This can be done while the board is running.
12. If carrying out EMI measurements, to reduce EMI the slew rate may be reduced. However, when doing this keep in mind that switching losses will be increased.
13. Measure the waveforms to determine the minimum acceptable dead time to avoid any possible overlap in switching, allowing some safety margin. Re-calculate the dead time if the slew rates have been altered. This should yield a result close to the experimentally obtained value.
14. Set the dead time values in the GUI and write the values to the device.
15. Observing the waveforms, reduce the dead time in small increments of 50 to 100 ns until an acceptable value is reached where there is 20 percent safety margin.
16. Use the GUI “Flash XMC firmware” function if using an XMC™ microcontroller.
17. Save the project each time a value is changed.
18. When the final values have been decided, the designer can use the GUI “burn OTP” function to ***permanently*** set these values in the 6EDL71x1.

[1] If the load is a BLDC motor, increase the torque and speed to fully load the system.

3.4 Input capacitor selection

To avoid excessive DC bus ripple it is necessary to include a combination of electrolytic and ceramic capacitors at the DC bus input. In cases where the battery is connected to the inverter through very short cables, the input capacitors are sometimes omitted to save space. It is very important to consider the drop in DC bus voltage that occurs when the motor is initially activated from a stationary state because this may cause system problems, which will be further explained in the next section.

The purpose of the capacitors is to provide a low-impedance path for HF current to circulate around the power circuits in each phase. Electrolytic capacitors have higher capacity but include series resistance (ESR) and inductance elements (ESL), whereas ceramic capacitors have lower capacity but do not include significant parasitic elements. Surface-mounted ceramic capacitors are also much smaller and easier to place close to the current loops at each of the phases.

In general, the selection of capacitors is a tradeoff between performance requirements and component cost/space constraints.

3.4.1 Electrolytic capacitors

First, select a suitable voltage rating, which is higher than the absolute maximum input voltage with a safety margin added of at least 30 percent. Then select a part with the lowest possible ESR and ESL values or alternatively with the highest ripple current rating. It is common to use two or three parallel electrolytic capacitors. In the first case one can be placed either side of the board and in the second case one can be placed at each of the phases. The goal is for each phase to have a similar current loop, so the placement of capacitors at each phase should be similar as far as possible.

The main constraint on electrolytic capacitor selection is size (board area) and height. For best performance the largest possible devices are selected within these constraints with the highest ripple current rating and lowest ESR and ESL ratings.

It is important to note that should the electrolytic capacitors be too small for the inverter's power rating the circulating ripple current will exceed the part rating, causing damage and premature failure.

3.4.2 Ceramic capacitors

Surface-mounted ceramic capacitors should be selected based on capacity, voltage rating and package size. One popular approach is to place an identical bank of parallel capacitors at each of the phases such that the connections to the top-side drain and ground are as short as possible. The connection to ground is generally through several vias to the ground plane on the first internal layer of the PCB. Each bank of ceramic capacitors may contain different values such as 1 µF, 2.2 µF or 4.7 µF. This is because different values have different impedance profiles at different frequencies and therefore a combination of values should provide better filtering across the frequency range.

The ceramic capacitor voltage is selected in the same way as for electrolytic capacitors; however, there are typically fewer options available so higher-voltage parts are generally used. For example, 50 V rated ceramic capacitors in a 24 V motor drive inverter.

Finally, the physical size should be based on board space constraints. 0805 and 1206 parts are generally a good tradeoff between size, rating, and cost.

3.5 PVDD connection

Since the inverter DC bus voltage is connected directly to the three-phase half-bridge power stage, it will inevitably contain some degree of HF noise and ripple. This increases under higher load conditions, i.e., for higher motor speed and torque conditions. Even with suitable electrolytic and ceramic input capacitors significant ripple can exist and it is essential to optimize the board layout in order to mitigate this. Such ripple contains components at different frequencies and may include high-voltage transient voltage spikes if there is too much inductance in the HF current path.

In order to supply a noise-free voltage to supply the PVDD input of the 6EDL71x1 driver, a diode (D1 in the example below) may be placed between the bus voltage and PVDD. This is often done and has been implemented on several Infineon evaluation boards.

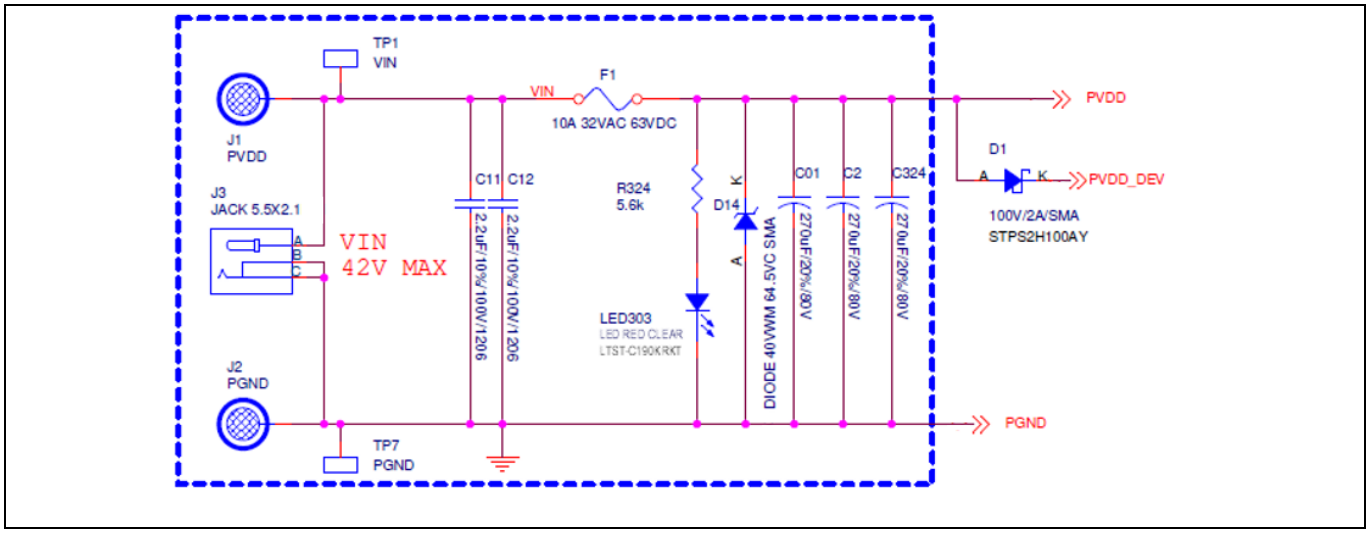


Figure 27 DC bus voltage containing HF ripple and noise

Where PVDD_DEV is connected to the 6EDL71x1 PVDD pin, with several capacitors connected to the 0 V bus (C36, 37, and 38 in this example):

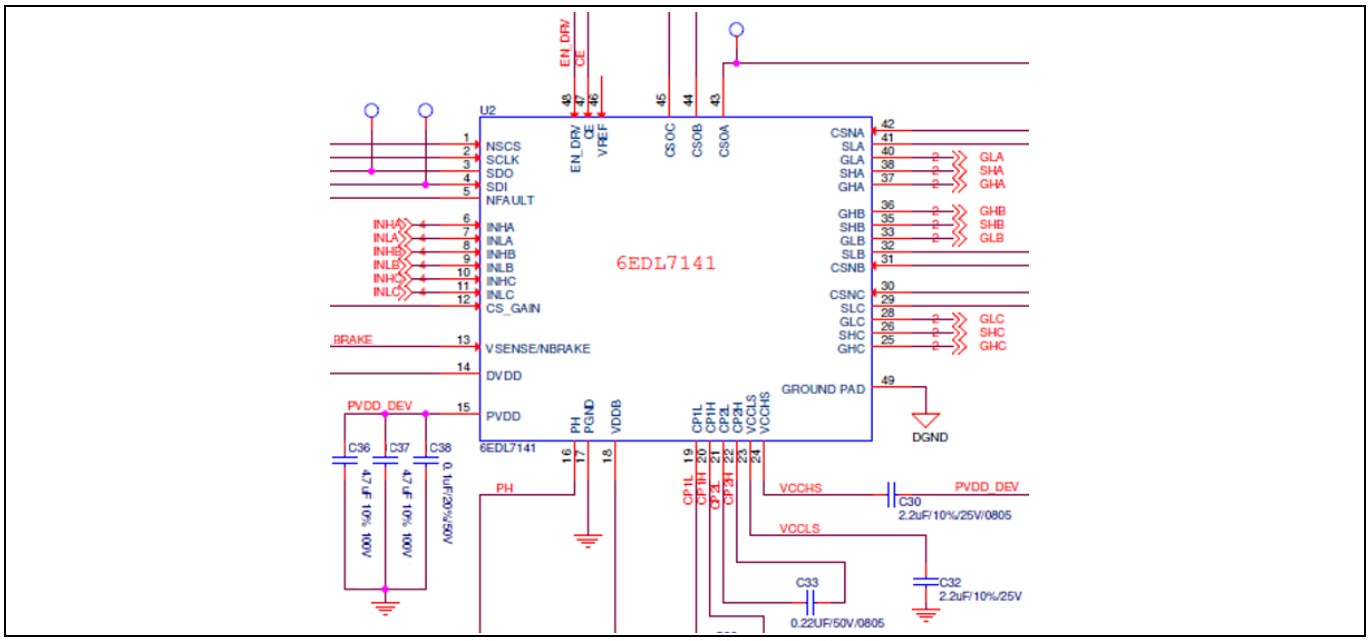


Figure 28 DC bus voltage containing HF ripple and noise

The problem with this approach is that peak rectification of the noise transients occurs so that the voltage at PVDD_DEV can become significantly higher than V_{IN} (PVDD) under certain conditions!

In some cases this peak rectification of the noise transients can create voltages high enough to damage the 6EDL71x1 driver IC. However, a more commonly encountered problem associated with this effect is that the high-side gate drive peak voltage with respect to the switch node is increased. This happens because the gate drive voltages for the three high-sides are derived from VCCHS, which is referenced to the device PVDD (PVDD_DEV). The switch node however transitions between 0 V and the bus voltage V_{IN}.

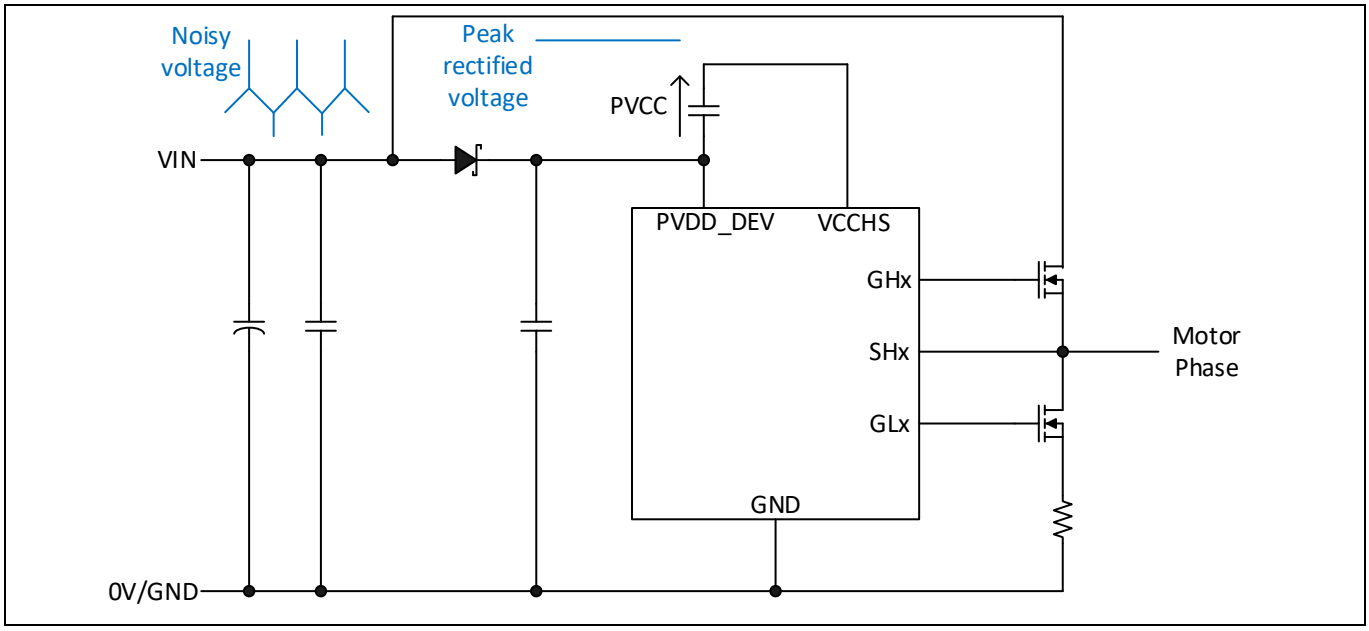


Figure 29 DC bus voltage containing HF ripple and noise

Consider a scenario where PVCC is set to 12 V generated from the charge pump to supply VCCHS but PVDD_DEV is actually 10 V higher than V_{IN} due to peak rectification through the diode. This means that when the high-side MOSFET is switched on the switch node (SHx) is equal to V_{IN} while the gate drive voltage (GHx) is equal to PVDD_DEV + PVCC, which is actually 22 V with respect to the source. This exceeds the MOSFET absolute maximum gate-to-source voltage rating and is likely to damage the gate oxide, causing the device to fail. This is also likely to cause failure of the 6EDL71x1 driver IC.

However, overcharging of PVDD_DEV can be greatly reduced by placing a resistor in the order of 10 Ω in series with the diode. This has the effect of filtering out the transient voltage spikes so that the capacitors connected from PVDD_DEV to ground will now charge only to a voltage level close to the peak of the lower-frequency components of the ripple. This is illustrated in the figure below.

It is therefore strongly recommended to include a series resistor when using a diode between V_{IN} and PVDD_DEV!

Considering a total capacitance of ~10 µF between PVDD_DEV and GND, a 10 Ω resistor would form a low-pass filter with a cutoff frequency of 1.6 kHz, which would filter out fast transients without limiting the current required to supply the 6EDL71x1.

It should be noted that placing Zener diodes between the gates and sources of the high-side MOSFETs to limit the gate drive is not an effective way of limiting the gate-to-source voltage. Not only would it require three additional components, but it would actually cause the high-side charge pump to detect an overload and generate a fault, shutting off all of the gate drive outputs.

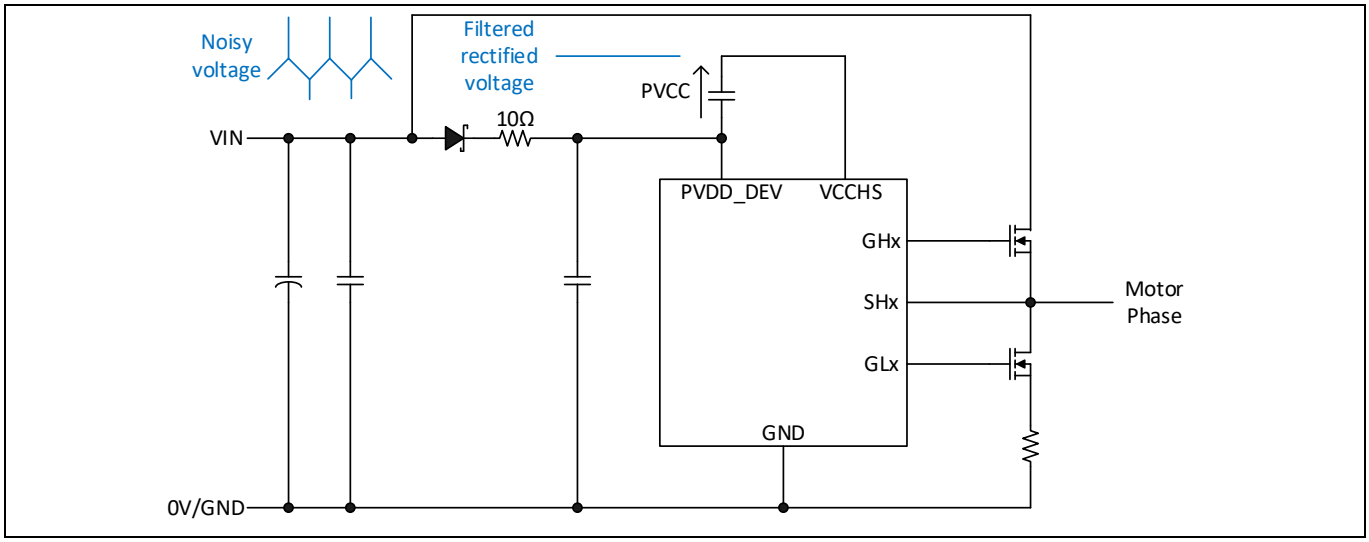


Figure 30 DC bus voltage containing HF ripple and noise

Another possible approach is to connect the VCCHS capacitor to VBAT instead of PVDD_DEV. Having done this, a 12 V or 13 V Zener diode can be placed in parallel with this capacitor to limit the maximum voltage.

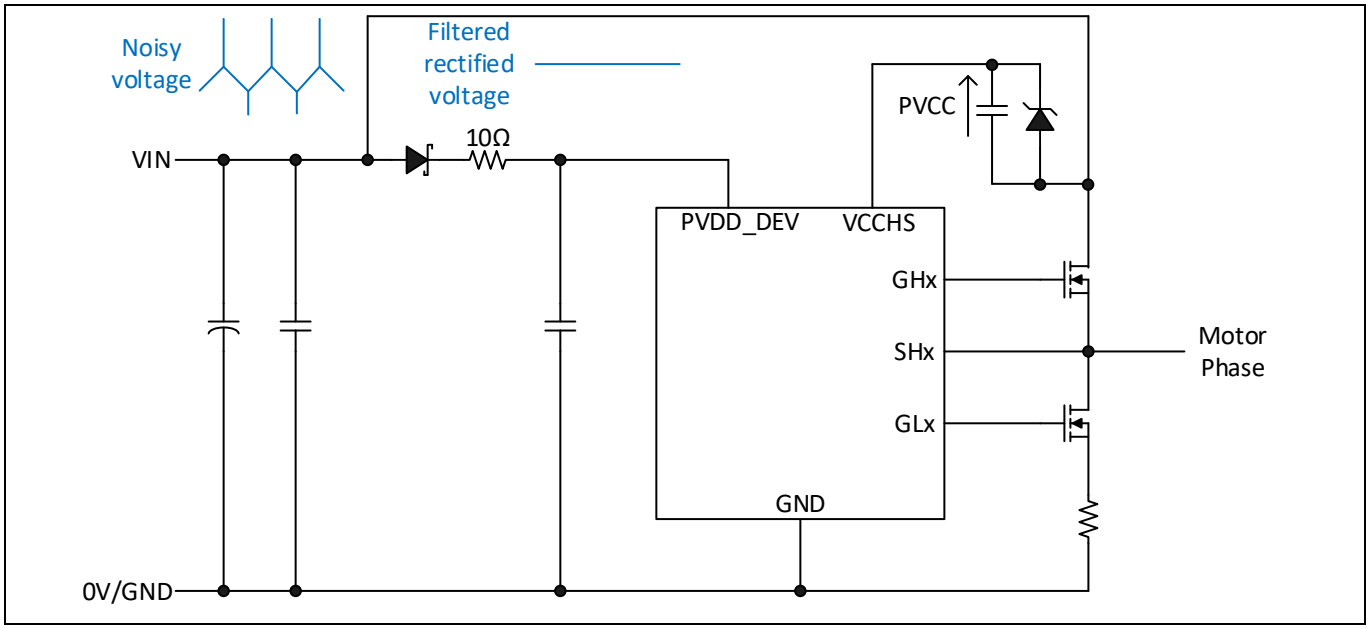


Figure 31 Referencing VCCHS to VBUS and adding a clamping Zener diode

3.6 Configuration of the buck and linear regulators

The VDDB output can be used to supply external components as long as the current limits of the buck converter, charge pumps and linear regulator are not exceeded. The voltage may be set to 6.5 V, 7 V, or 8 V, depending on the gate drive voltage selection. Intelligent OCPs are also implemented for both the buck converter and the linear regulator to prevent any damage to the device if the VDDB output becomes overloaded. Additional overtemperature protections (OTS, OTW) are integrated to ensure that the device operates within correct thermal limits.

Two different switching frequencies, 500 kHz (default value) or 1 MHz, can be selected via the GUI. The buck inductor L1 value is 22 µH for 500 kHz switching and 10 µH for 1 MHz. The values for the buck output capacitors recommended are 22 µF with an additional 0.22 µF ceramic capacitor added to reduce HF noise. Both the synchronous buck converter and linear voltage regulator circuits are shown in **Figure 32**.

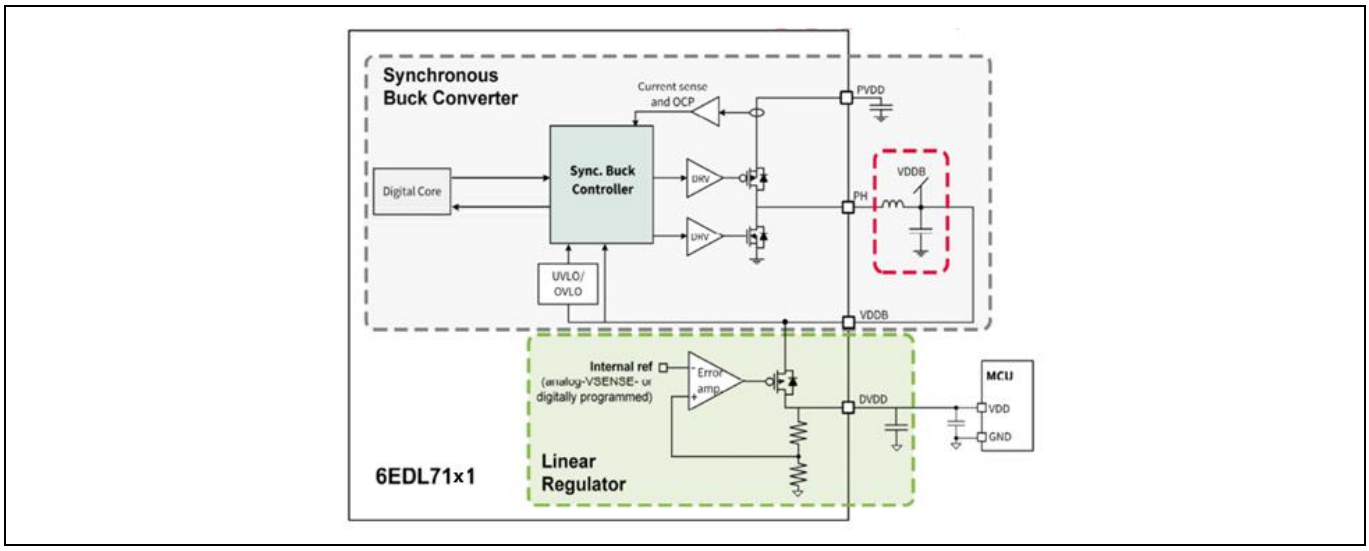


Figure 32 Detail of integrated synchronous buck converter and linear regulator

The following protections are implemented to ensure correct operation of the buck converter:

- Output UVLO
- Output overvoltage lockout (OVLO)
- OCP, cycle by cycle

In a situation in which the current exceeds the OCP level, the buck converter controller terminates the high-side gate drive pulse until the start of the next PWM period. The low-side operates accordingly after insertion of the dead time.
Once the OCP event takes place, a counter increments each consecutive period that the peak current is reached. After 16 switching cycles, the buck OCP fault is triggered and the nFAULT pin is set low to signal the MCU. The buck converter will continue operation in current limitation to ensure the MCU remains powered. If the OCP is not triggered for three consecutive PWM periods, the counter resets.

The integrated linear regulator output DVDD can be set to either 3.3 V or 5 V by means of an external resistor R44, which is set to 10 kΩ on this evaluation board to set DVDD to 5 V. It is possible to override this hardware setting through the GUI, which can also read back the value set by the hardware. The linear regulator can also be used to provide an offset to the CS amplifiers to allow negative current measurements.

DVDD OCP can be configured between four different levels – 50 mA, 150 mA, 300 mA or 450 mA, with 450 mA being the default value. If the OCP level is reached a fault is reported through the nFAULT pin. The DVDD OCP works in two different stages:

1. Pre-warning mode at 66 percent of selected OCP level:
   The nFAULT pin is pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching the 100 percent level, the operation will continue normally, releasing the nFAULT pin. The pre-warning allows some extra time for the microcontroller to make a decision on how to react to the possible OCP event.

2. Current limiting mode at 100 percent of selected OCP level:
   If current increases beyond the configured OCP level, the DVDD regulator limits its output current. This causes the DVDD voltage to drop, eventually resulting in a DVDD UVLO fault if the UVLO threshold is crossed. This protects DVDD against a short-circuit condition.
   Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated only under recommended operating conditions as specified in the datasheet.

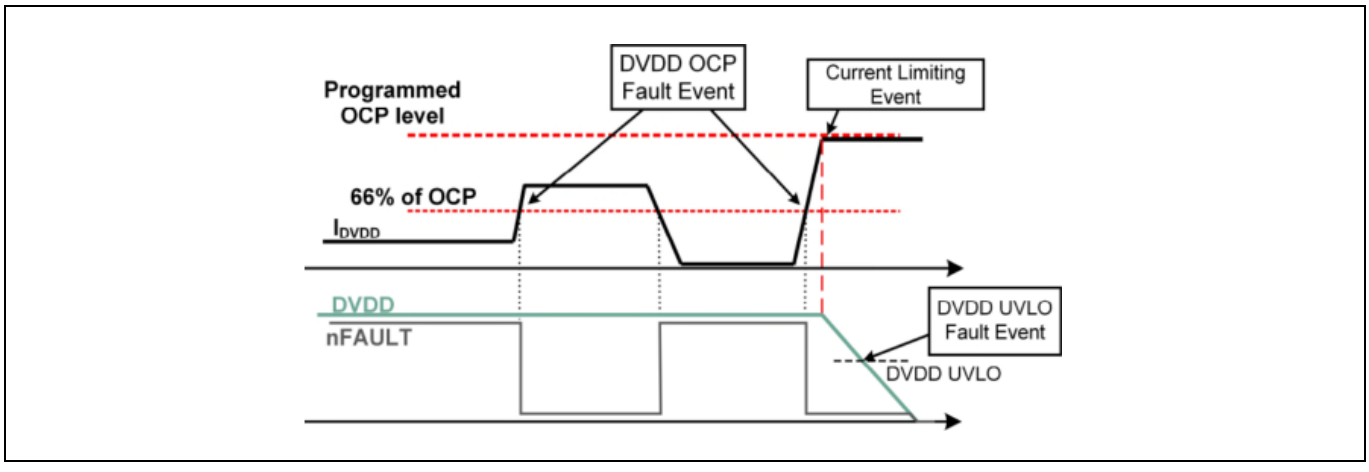


Figure 33 DVDD OCP behavior including pre-warning and current limiting modes

3.7 Configuration of the charge pumps

The high- and low-side gate driver charge pumps are based on switched capacitor circuits that operate at a determined switching frequency. Selection from one of four frequencies, 781.3 kHz, 390.6 kHz, 195.3 kHz, and 1.56 MHz, allows flexibility for EMC optimization, with 781.3 kHz being the default setting. Another useful feature in reducing the EMI impact of the charge pump is the spread spectrum feature, which can also be enabled and disabled via the GUI. This function is enabled by default to provide a frequency variation into the charge pump clock signal in order to distribute emissions over a wider frequency range, thereby reducing peaks.

The selection of charge pump flying capacitors is specified as 0.22 µF and the tank capacitors should be 2.2 µF. The 6EDL71x1 provides pre-charging of the charge pump output capacitors to a voltage just below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. In this way, the charge pump start-up time and therefore the system start-up time are reduced. In this case, when EN_DRV is activated by the microcontroller to enable the gate driver stage, the charge pumps need only to ramp up the voltage from the existing pre-charge voltage to the selected target value. Pre-charge is disabled by default and can be enabled via the GUI.

The start-up time for the charge pumps, defined as the time that the gate drive supply voltages require to get to the target programmed voltage, depends on several factors:

- Target voltage: The higher it is, the longer the start-up time for the gate drivers.
- Charge pump clock frequency: Higher clock frequency results in faster start-up time.
- Charge pump tank capacitor values: A smaller value results in faster ramp-up time but higher ripple.
- Charge pump flying capacitors: Smaller capacitors lead to slower start-up time.

3.8 Configuration of the current sense amplifiers

The 6EDL7141 and 6EDL7151 integrate three CS amplifiers that can be used to measure the current in the inverter via shunt resistors. Single-, double- or triple-shunt measurements are supported, as shown below. CS amplifiers are not included in the 6EDL7131.

Each CS amplifier can be enabled individually. Gain and offset are generated internally and are programmable.

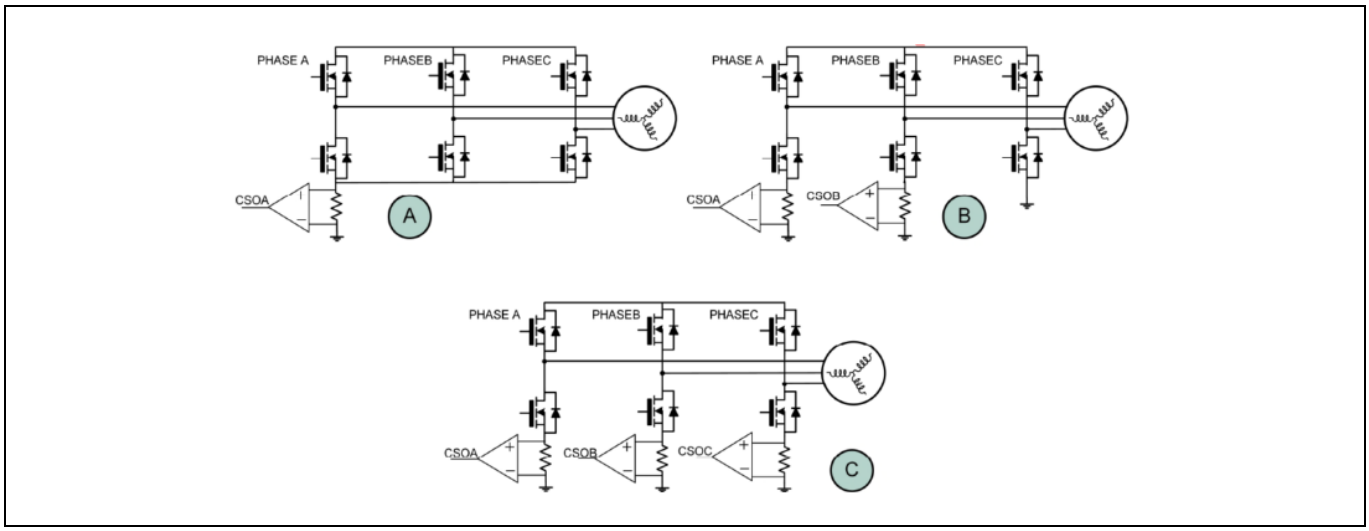


Figure 34 Single- (A), dual- (B) and triple- (C) shunt current sensing configurations

The CS amplifier block contains the following sub-blocks, explained in detail in this section:

- CS amplifier: Connected to external shunt resistor or internally to an SHx pin for $R_{DS(on)}$ sensing. This module amplifies the shunt voltage or $V_{DS(on)}$ voltage to a level suitable for a microcontroller ADC input. It includes leading-edge blanking (LEB) of the signal synchronized to the gate drive, which is active during periods to eliminate noise.
- Output buffer: Allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to one of four different values, either by programming the internally generated level or by applying an external voltage at the VREF input pin. With this implementation, negative shunt currents can also be measured.
- Positive overcurrent comparator: Used for detecting the overcurrent conditions on motor windings for positive shunt voltage. This comparator causes the gate drive pulse to be terminated, thus limiting the motor current.
- Negative overcurrent comparator: Used for detecting the overcurrent condition on motor windings for negative shunt currents.
- OCP DAC: Used for programming the overcurrent comparator thresholds. One sets the positive level and a second sets the negative level, which are shared among the different OCP comparators.

The CS amplifier architecture includes an “auto-zero” function. This takes place during 6EDL71x1 start-up and operation to maintain accuracy of measurements during the lifetime of the device. If no GHx rising edge happens for a given time (tAUTO_ZERO_CYCLE), i.e., if the low-side is fully turned on for a long period in a six-step commutation, then an internal WD timer triggers an auto-zero compensation. Auto-zero is continuous during the standby state. The auto-zero feature can be disabled via the GUI. In addition, the 6EDL7141 and 6EDL7151 include a CS amplifier user calibration mode that can be used to measure and compensate for offset at a time when the shunt current is known to be zero, i.e., when all of the gate drives are low.

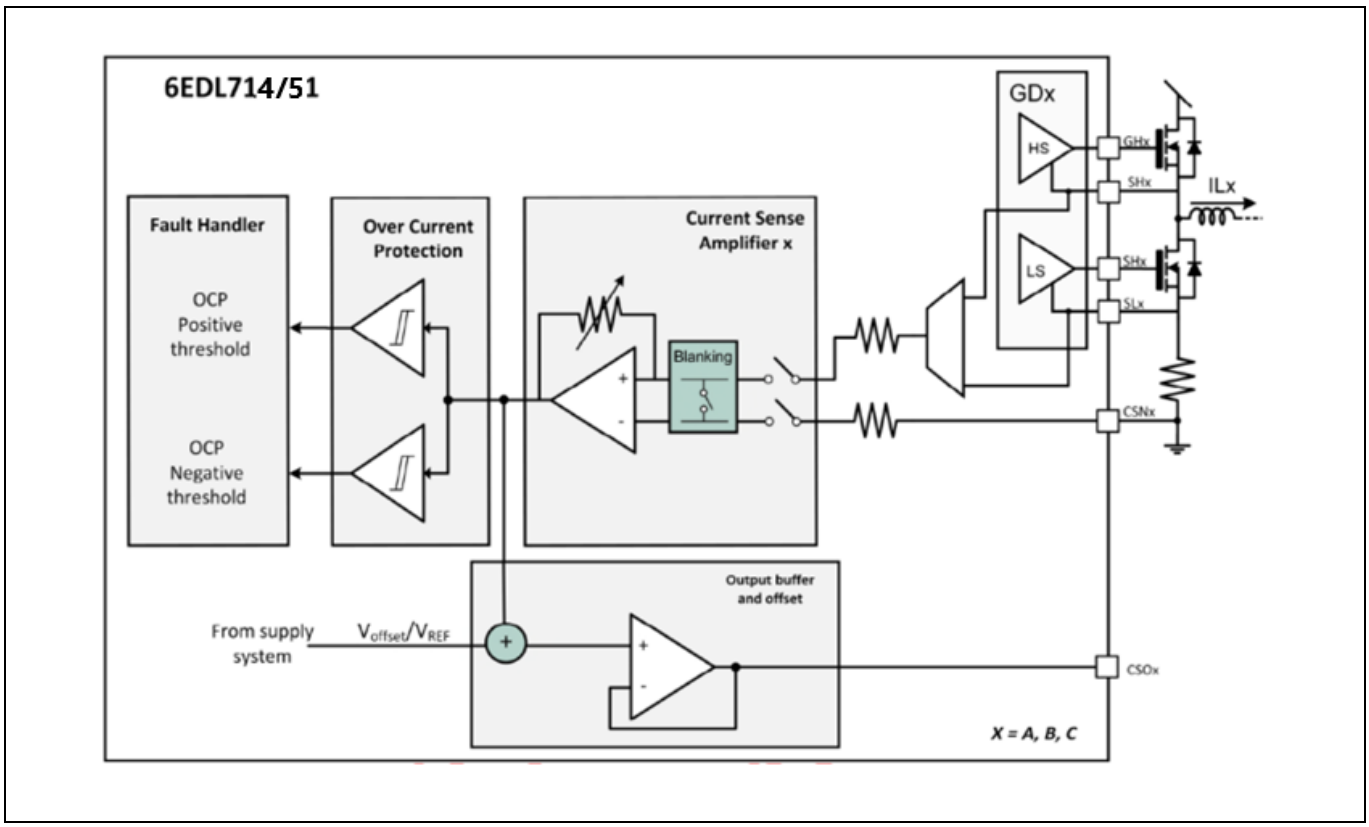


Figure 35 CS amplifier simplified block diagram

The CS amplifiers can be configured for $R_{DS(on)}$ sensing to avoid the use of shunt resistors.
This method is not recommended for FOC designs where accurate current measurements are needed!

However, it may be sufficient for OCP purposes in trapezoidal designs. It should be noted that MOSFET $R_{DS(on)}$ varies significantly with tolerance and temperature!

The CS amplifiers have a default voltage gain of 4. This can be changed via the GUI to any of the following values: 8, 12, 14, 20, 24, 32, or 64. Alternatively, the gain can be selected by connecting an external resistor from pin CS_GAIN to ground. In order to enable analog programming of the CS amplifier via an external resistor, the user must ensure that bitfield CS_GAIN_ANA is set accordingly. The value of RGAIN is read during the start-up sequence of the 6EDL7141 and 6EDL7151. Table 15 in the 6EDL7141 datasheet **[1]**provides the resistor values and register settings for gain selection in both analog and digital modes.

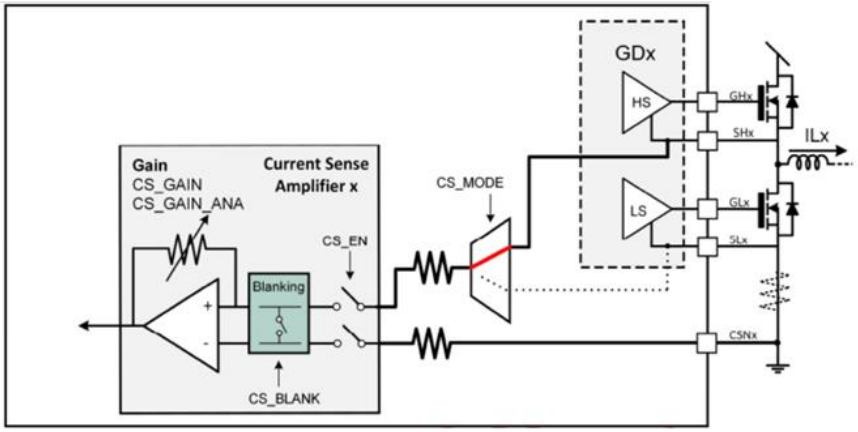


Figure 36 System diagram of a low-side $R_{DS(on)}$ current sensing configuration (not used here)

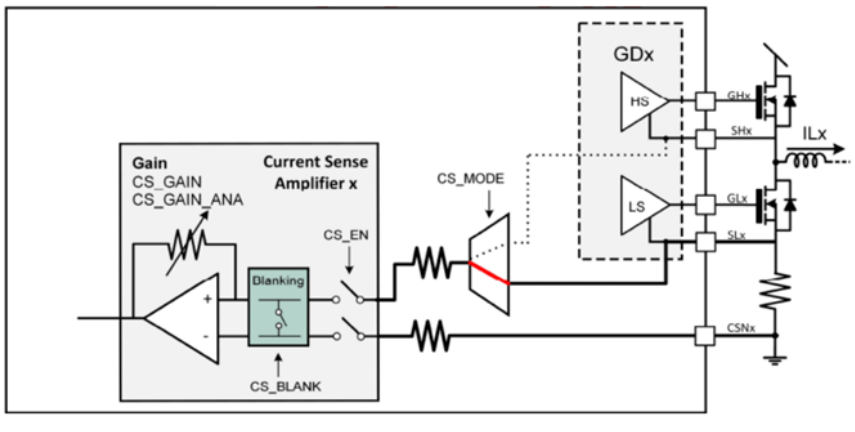


Figure 37 System diagram of an external shunt current sensing configuration

In many motor drive inverters such as this evaluation board, the current is sensed via shunt resistors. In this case, the voltage across the shunt needs to be amplified only when the low-side MOSFET is switched on. In other cases, it might be useful to monitor the signal continuously. The 6EDL7141 and 6EDL7151 support four

different modes of operation of the CS amplifiers regarding when the output is connected to the amplifier, which can be selected through the GUI.

These four modes are:

- Always OFF: CS amplifier output disabled. This is achieved by disabling the amplifier in register CSAMP_CFG via bitfield CS_EN.
- GL ON (default mode): in this mode, the CSOx pin is connected to the amplifier only when the corresponding GLx signal is active. In single-shunt mode CSOx is connected according to the ORing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx come from the corresponding GLx signal. This mode is mandatory if $R_{DS(on)}$ sensing is selected to avoid overvoltage damage to the internal circuitry.
- GH OFF: similarly to GL ON, this mode exposes the output to GL ON period but extends the sensing period to the dead times, both rising and falling.
- Always ON: this mode connects the activated amplifier CSOx signals continuously to the amplifier independently of PWM signals.

The programmable LEB function can be configured in the CS amplifiers. Since both phase node voltage SHx and SLx pins (CSNy) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time (CS_BLANK). The default blanking time is zero, and values between 50 ns and 8 µs can be selected via the GUI. The 6EDL71x1 internal linear voltage regulator (DVDD) can be used for offset generation for CS amplifiers. The default value is 1/2DVDD; values of: 5/12, 1/3 and 1/4DVDD are also available.

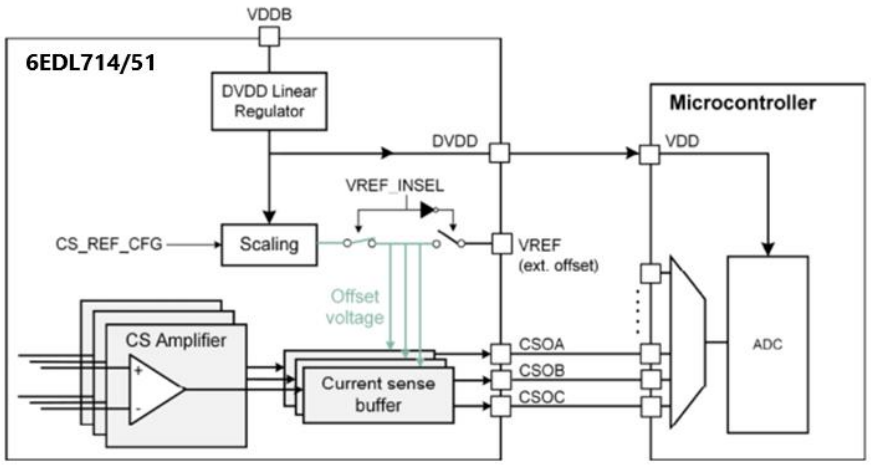


Figure 38 CS amplifier offset generation block diagram

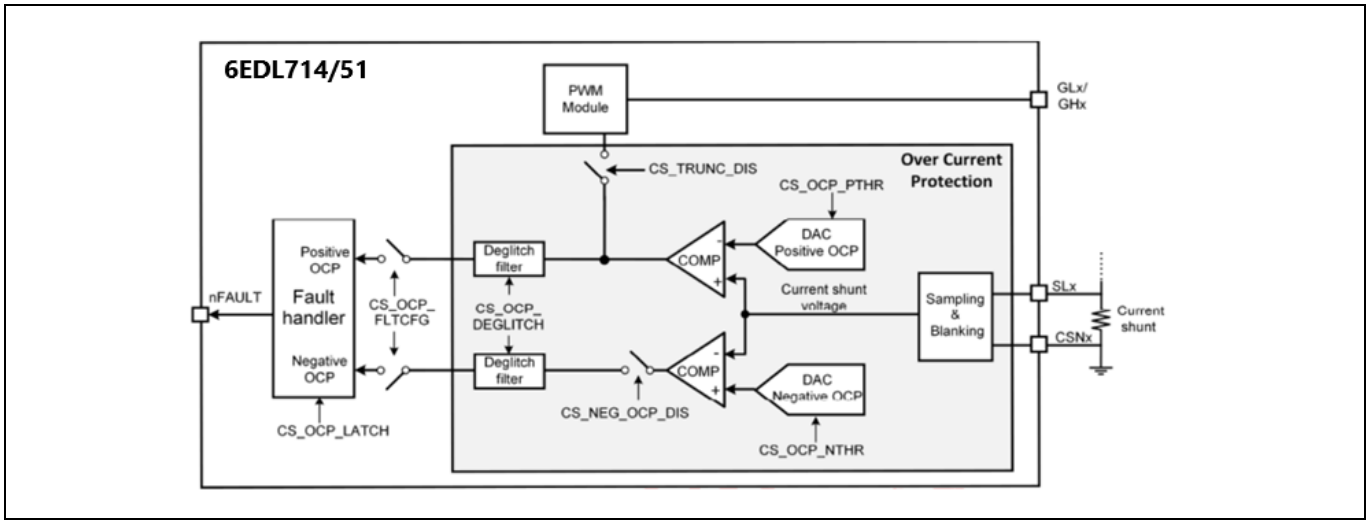


Figure 39 CS amplifier architecture

How the 6EDL71x1 reacts to an OCP event is programmable via the GUI. The following scenarios can be useful for different applications:

- Apply PWM truncation immediately after OCP event and report on nFAULT pin after OCP event – deglitching is disabled if truncation is enabled.
- Disable reporting but keep truncation of PWM.
- Trigger a configurable brake action upon OCP event. If truncation is not desired, a brake event can be configured using one of the available braking modes.
- Disable OCP protection, both nFAULT reporting and truncation of PWM. In this case, OCP is ignored.

It is also possible to select whether the OCP fault is latched or not via the GUI. In a latch configuration, the nFAULT pin is held low until the fault is cleared via an SPI command or after a power cycle. If the OCP fault is configured as non-latched, the nFAULT pin remains low while the fault is being detected but will pull up again when the OCP condition is no longer present. Configuration allows the user to set a target number of consecutive events (PWM cycles) required to activate the nFAULT fault signaling.

If a positive OCP event occurs, the high-side PWM is truncated. The result is that the high-side MOSFETs are all switched off and the current flowing in the motor windings therefore recirculates through the low-side MOSFET body diodes.

4 Using the BPA motor control GUI

The BPA motor control GUI is a tool for installing control firmware into a compatible microcontroller and configuration settings to the 6EDL71x1 gate driver. It includes firmware for motor control boards operating with trapezoidal control or FOC with one or three shunts. Once the options and parameters for a particular project have been selected, the configuration can be saved as a project file with a .6EDL extension.

The BPA motor control GUI is installed from Infineon's Developer Center Launcher, which can be downloaded and installed from the following web page:
https://www.infineon.com/cms/en/design-support/tools/utilities/infineon-developer-center-idc-launcher/

Once installed, click on the "manage tools" tab and search for "BPA". The following should appear:

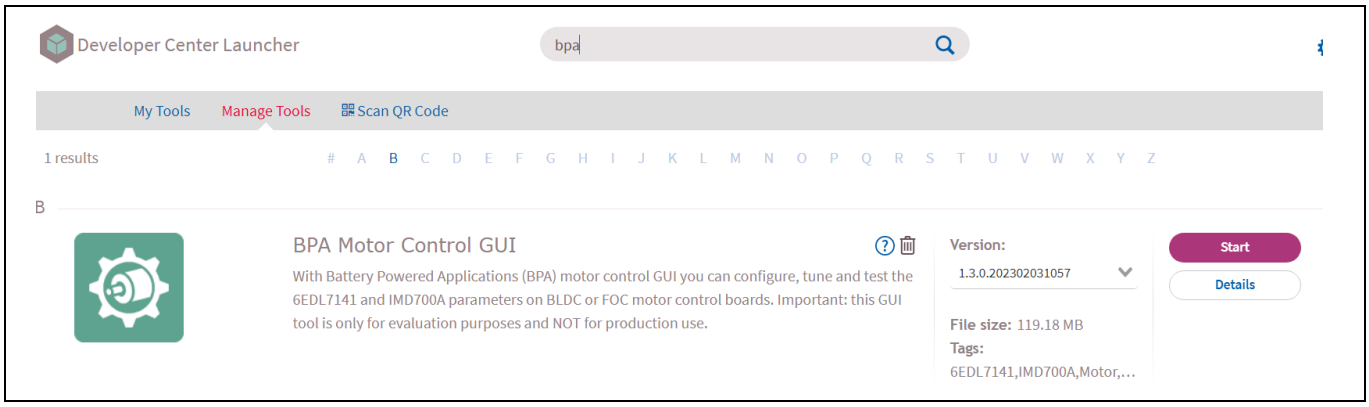


Figure 40 Infineon Developer Center Launcher

Then click on "start" to install the GUI. Once installed and started, the GUI opening screen appears as follows:

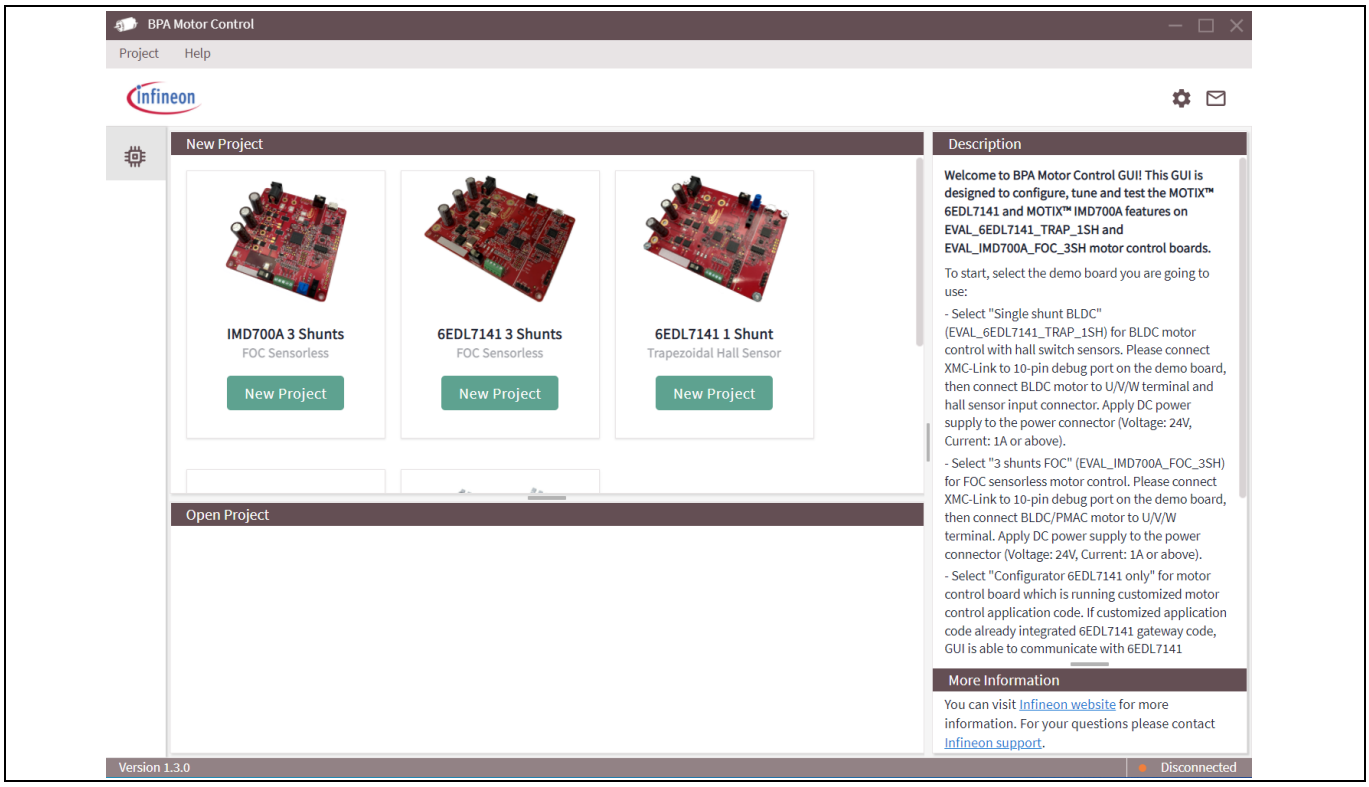


Figure 41 BPA motor control GUI opening screen

4.1 Creating a project in the BPA motor control GUI

To start a new project, first select the required configuration from the available options shown in the opening screen. For example, the EVAL_6EDL7141_TRAP_1SH evaluation board is a single-shunt design for BLDC, which when selected brings the GUI to the next screen. More options are available by scrolling down in the “New Project” window.

Note: ***Note that the GUI is able to recognize whether the correct board has been connected via the USB interface. If the correct board is not connected it will not operate! To connect the GUI to the board go to the “disconnected” button at the bottom right of the screen, click and select the J-Link debugger that should be displayed.***

Having selected a project and with a suitable board connected, the next step is to expand the dropdown menu from the “XMC1400” option in the “Parameter Controls” panel.

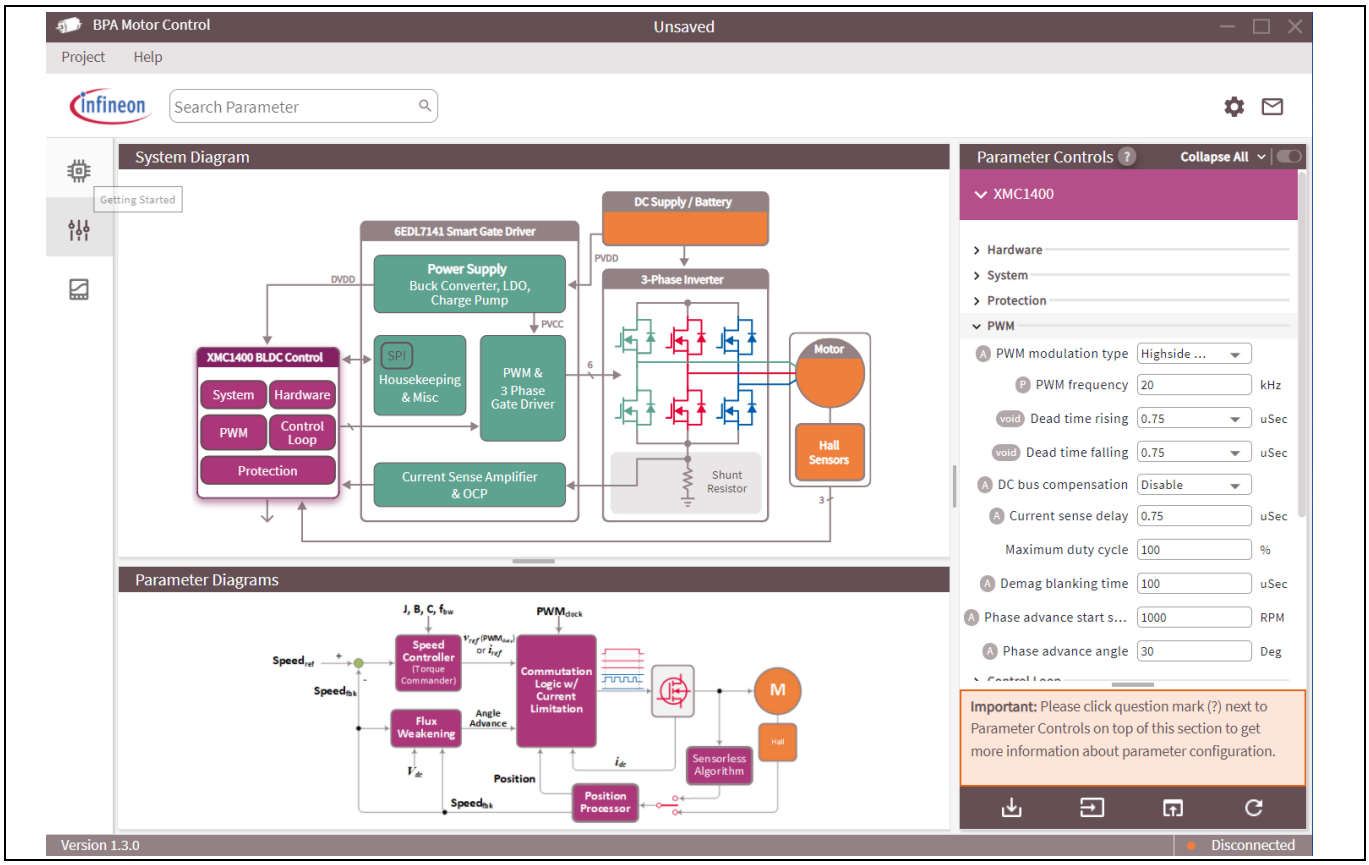


Figure 42 Trapezoidal control with single-shunt firmware configuration menu

4.2 Downloading the motor control firmware from the GUI

The GUI contains firmware code for the XMC1404 microcontroller to support both single-shunt trapezoidal commutation with Hall sensors or three-shunt sensor-less FOC. ***Note that although the user may select firmware parameters, the firmware source code may not be viewed or downloaded from the GUI. The compiled executable file is instead installed into the target board MCU directly.*** Source code for motor drive firmware is available through the Modus Toolbox IDE, which may be downloaded from the following web page: https://www.infineon.com/cms/en/design-support/tools/sdk/modustoolbox-software/

The firmware installed from the GUI contains additional support functionality that allows the GUI to communicate with the microcontroller and 6EDL71x1 driver to both configure the operating parameters and also to control and monitor the motor drive inverter during operation. As mentioned, the GUI includes a suite of firmware options that can be downloaded to any compatible motor drive board, which uses the XMC1400 microcontroller with the 6EDL71x1 or the integrated IMD700/1 A. In **Figure 42**, on the right-hand side the XMC1400 is expanded to show the firmware options available. Some of the firmware options are also shown such as the PWM frequency and dead time.[1]

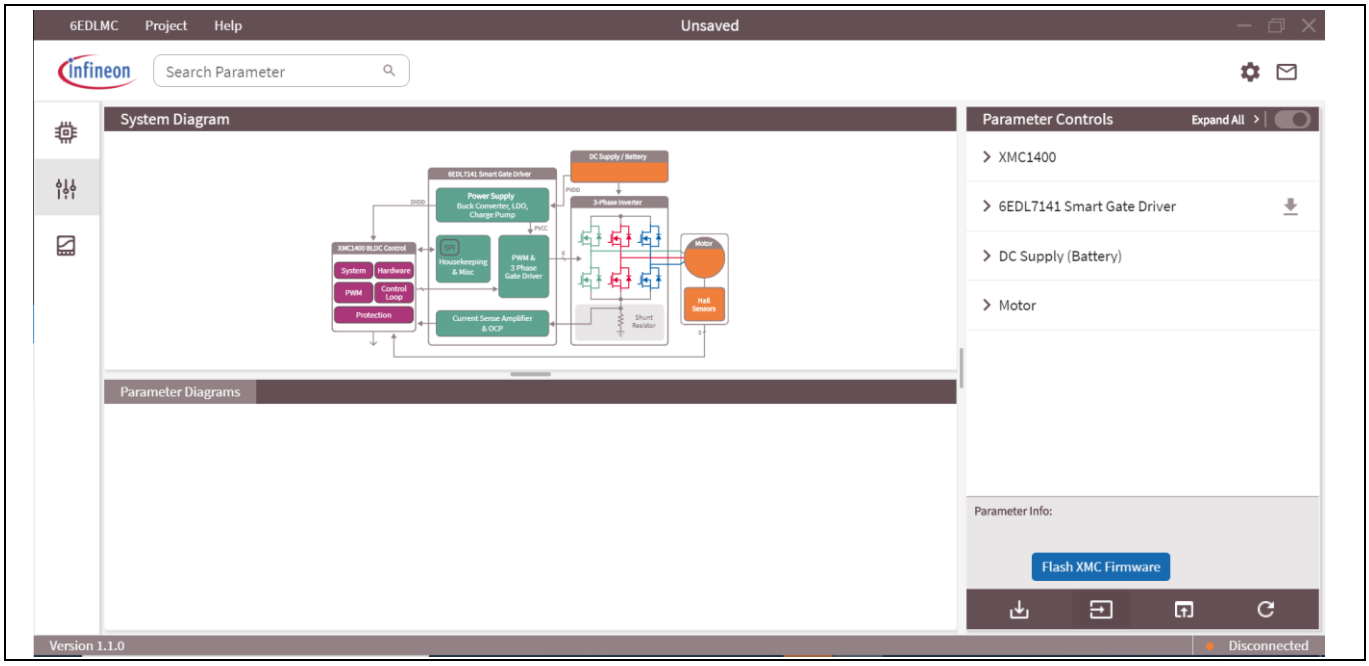


Figure 43 Firmware options and download

There are various important firmware parameters to be selected before downloading. These are listed in the table below with example values. When the firmware parameters have been selected in the GUI, the firmware may be downloaded to the board via the USB cable by clicking the “Flash Firmware” button as shown above. A message will appear to inform the user that the firmware was successfully programmed onto the microcontroller.

Table 4 List of firmware parameters

Parameter	Description	Value	Unit
ADC reference voltage	V_{ADC} reference voltage, same as DVDD	5	V
Shunt resistor	Bill of materials RS1	0.5	mΩ
Potentiometer control	Enable hardware potentiometer	Enable	
Control scheme	Select command parameter	Speed control	
Catch spin start	Catch start a rotating motor	Enable	
PWM modulation type	Select PWM modulation scheme Refer to section 4.1	High-side sync	
Minimum pot. input	Minimum potentiometer input level	5	%
Stall detection time	Delay on stall detection response	1.2	s

[1] In 6PWM mode the dead time is set by the microcontroller or 6EDL7141, whichever is greater. In other modes it is set by the 6EDL7141.

Stall min. amplitude	When amplitude of setpoint is below this value, stall detection is disabled	10%	%
Stall	Enable/disable stall detection	Enable	
Overvoltage threshold	DC-link overvoltage threshold	30	V
DC-link overvoltage	Enable/disable OVP	Enable	
Undervoltage threshold	DC-link undervoltage threshold	16	V
DC-link undervoltage	Enable/disable UVP	Enable	
TRAP	Enable/disable OCP	Enable	
Wrong Hall	Enable/disable incorrect Hall sensor connection detection and shutdown	Enable	
Hall learning	Enable/disable Hall sensor learning	Enable	
SPI timeout error	Enable/disable SPI timeout error	Enable	
PWM frequency	PWM switching frequency	20	kHz
Dead time rising	PWM dead time for rising edge	0.44	µs
Dead time falling	PWM dead time for falling edge	0.44	µs
DC bus compensation	Enable/disable DC bus compensation	Disable	
CS delay	CS ADC trigger delay from center of PWM on-time	0.75	µs
Maximum duty cycle	Maximum PWM output duty cycle	100	%
Demag. blanking time	Demagnetization blanking time for skipping DC-link current measure after PWM commutation	100	µs
Phase advance speed	Phase advance starting speed, advance angle increase linearly above this speed	1000	RPM
Phase advance angle	Maximum phase advance angle (at maximum speed), set 0 to disable phase advance	30	Degrees
Ramp-up time	Ramp-up time from zero to maximum speed	0.5	s
Ramp-down time	Ramp-down time from maximum speed to zero	0.5	s
Ramp-down hold voltage	Maximum DC-link voltage that allows ramp-down; ramp-down will be held if DC-link voltage above the threshold	28	V
Speed control rate	Speed control execution rate in number of PWM cycles	1	
Speed K_P	P-I control parameter: proportional	200	
Speed K_I	P-I control parameter: integral	10	
Speed P-I limit	Speed P-I regulator voltage output limit	100	%

4.3 Configuring the 6EDL71x1 parameters

The PWM configuration and gate driver parameters can be selected by expanding the “PWM and Three Phase Gate Driver” menu and selecting each parameter from the options available. Each parameter has a dropdown menu which allows the user to select from the values available.

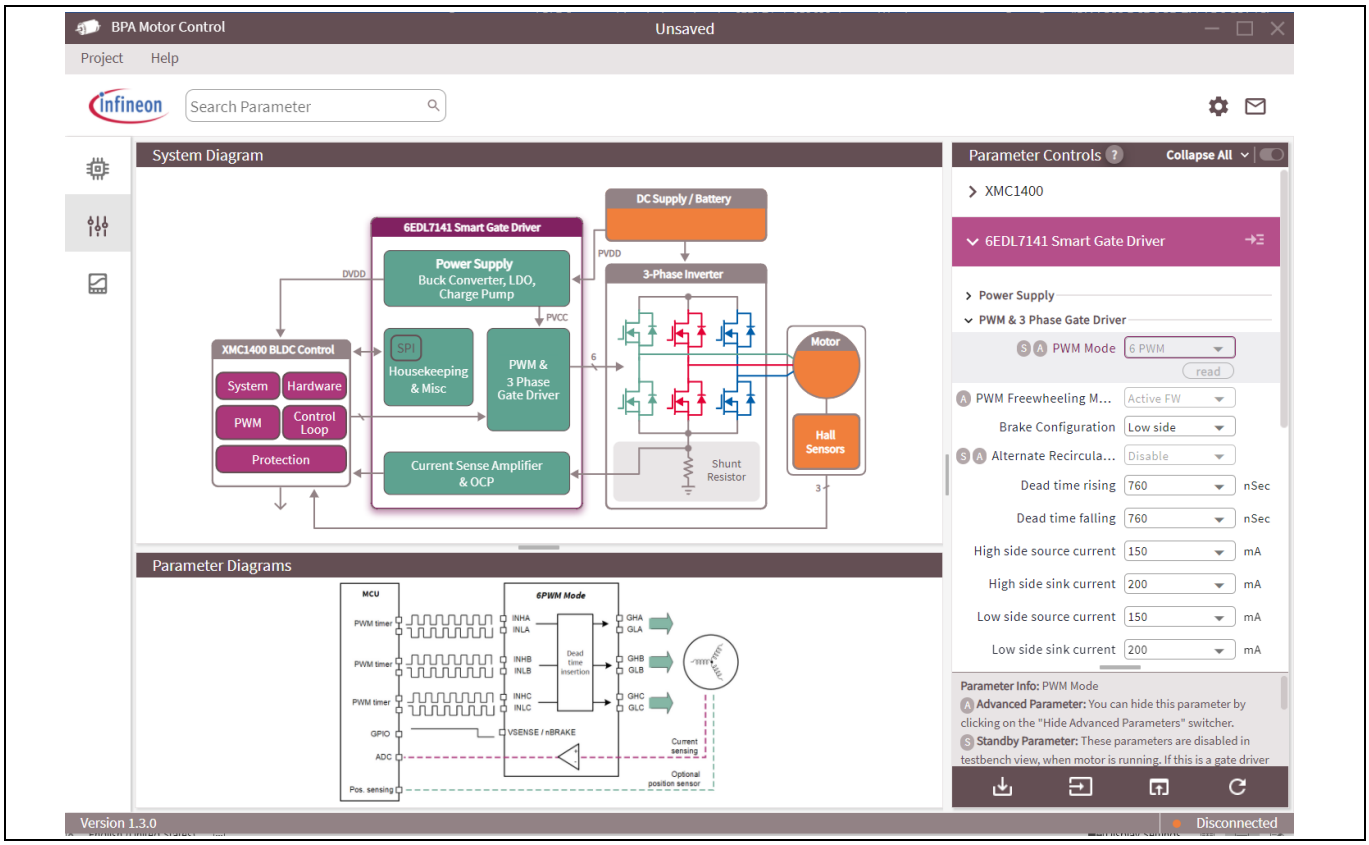


Figure 44 Selecting the PWM mode

The parameters available for adjustment are listed in **Table 5** for the 6EDL7141. The 6EDL7151 includes some additional parameters for configuring the drain-source voltage sensing protection function.

4.3.1 MOSFET tuning tool

MOSFET tuning is a useful design aid included in version 1.3 and above of the GUI. This can be launched from the opening screen.

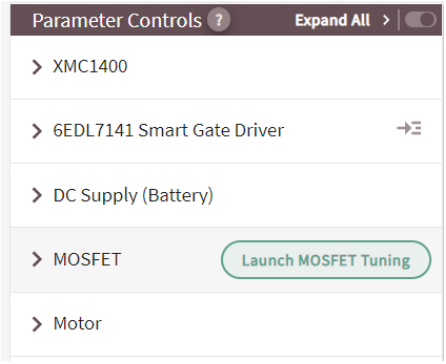


Figure 45 Selecting the gate drive parameters

The MOSFET tuning tool enables the user to select an Infineon MOSFET from the dropdown menu in panel (1). The user then specifies the number of devices that will be paralleled in each of the six switch locations of the three-phase inverter. Next the DC-link (battery) voltage is entered as a parameter along with the maximum operating load (RMS) current per phase and the maximum operating case temperature. The tool retrieves the MOSFET datasheet parameters from Infineon's online database when the user clicks on the "update MOSFET parameters" button. The funnel icon to the right of the MOSFET dropdown menu opens an additional window, which allows the user to filter the available MOSFETs according to BV_{DSS}, $I_{D(MAX)}$ and package.

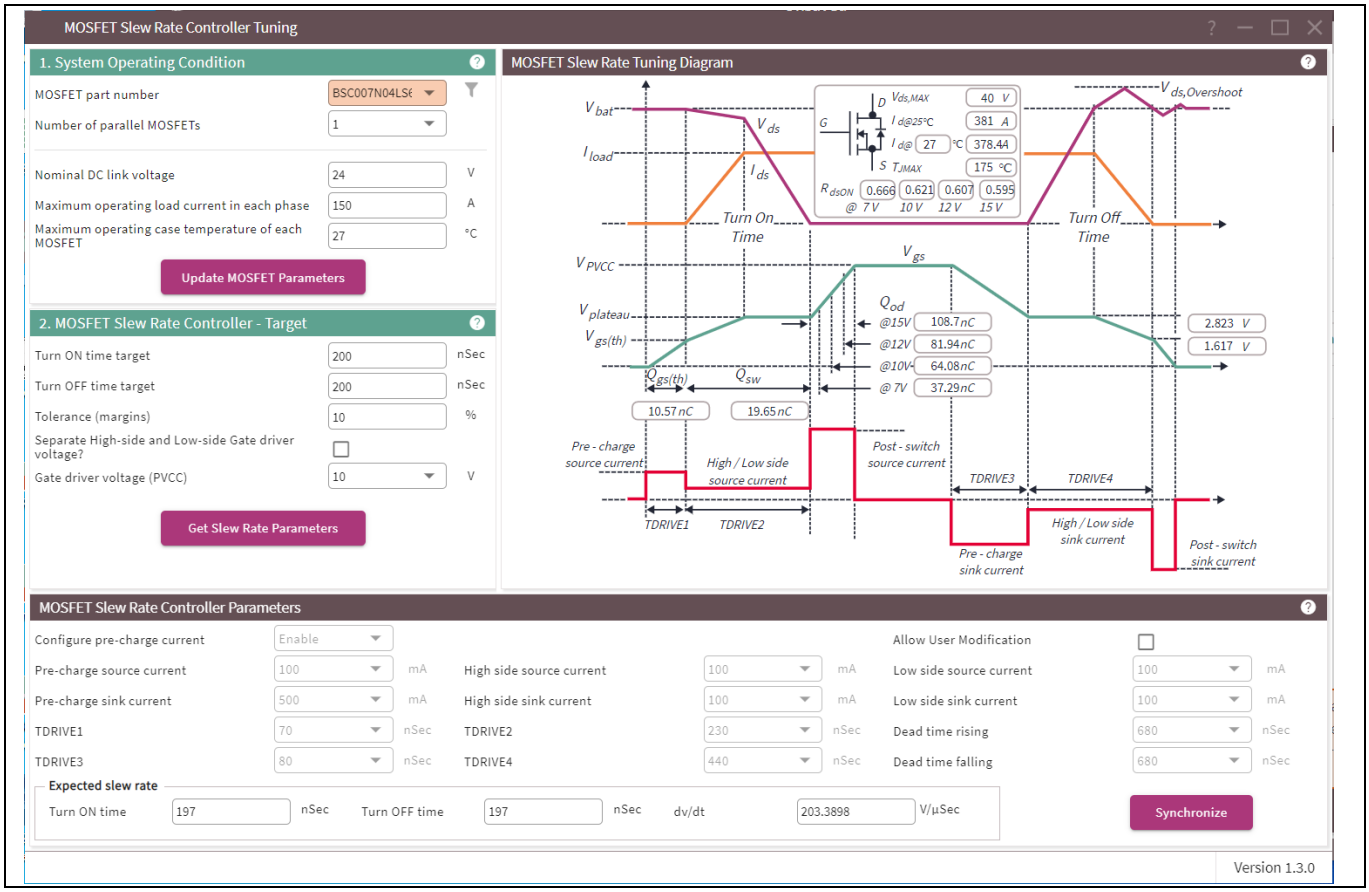


Figure 46 MOSFET tuning screen

Having obtained the parameters for the selected device, the gate drive parameters can be calculated based on target turn-on and turn-off times. These are entered into panel (2) by clicking on the "get slew rate parameters" button.

The calculated values are displayed in the panel at the bottom of the screen and can be loaded into the GUI project's parameter list by clicking the "synchronize" button in the bottom right corner. If required, the user has the option to adjust these values before synchronizing. This design aid allows an initial set of parameters to be determined without the designer needing to carry out any calculations.

Note: ***The designer should verify and fine-tune the calculated parameters during lab evaluation and design verification.***

4.3.2 Adjusting the parameters manually

The GUI enables configuration of all of the 6EDL71x1 selectable parameters, including the onboard power supply and charge pump settings and the CS amplifiers and OCP thresholds as discussed in previous sections.

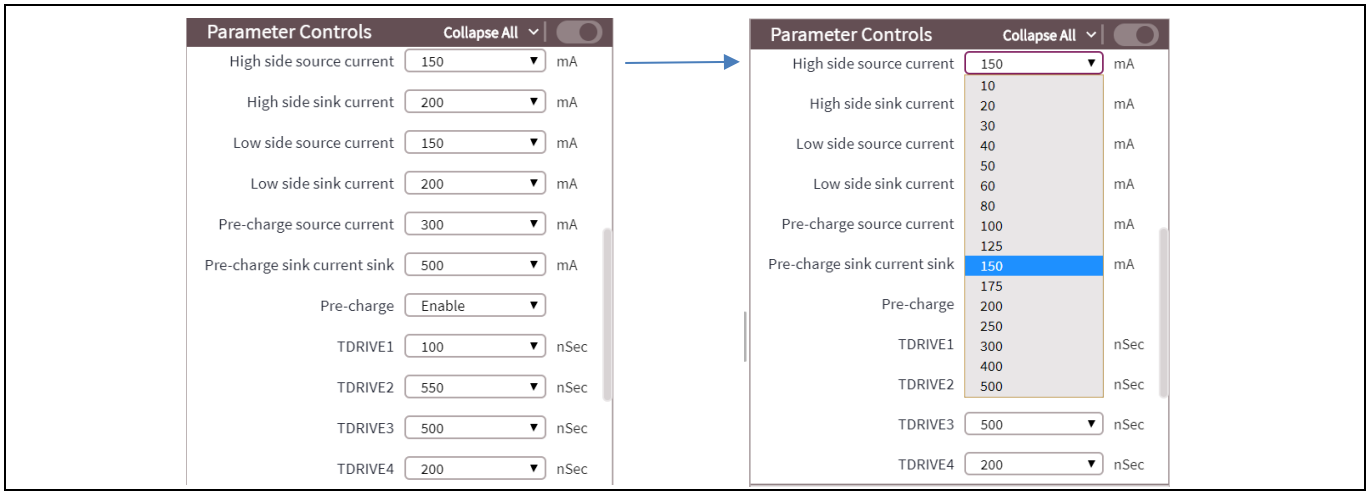


Figure 47 Selecting the gate drive parameters

Once all of the firmware options and 6EDL71x1 parameters have been selected for a design, the project should be saved via the “Project” menu at the top of the screen. The project file has a .6EDL extension. A list of 6EDL71x1 parameters is provided in **Table 5**, which includes some example values. The configurable parameters available vary among different devices in the 6EDL71x1 family. This is also indicated.

The 6EDL71x1 can be programmed with the selected values using the following options:

Figure 48 Transferring the settings to the 6EDL7141

The “Write Parameters” option transfers the configuration to volatile memory, which will remain only while the 6EDL71x1 is powered. This option should be used during bench testing and optimization until the designer is completely satisfied that all of the correct values have been selected. If values are changed during bench evaluation, the project should be saved again. When the designer is sure that the final values have been obtained, the “Burn 6EDL71x1 OTP” option may be used to permanently set the configuration in the OTP memory.

Table 5 List of additional 6EDL71x1 parameters

Parameter	Value	Unit
Power supply		
PVCC setpoint	12	V
Charge pump clock frequency	781.25	kHz
Charge pump spread spectrum	Enable	
Charge pump pre-charge	Disable	
Buck converter frequency	500	kHz
DVDD setpoint	V_SENSE pin	
DVDD soft-start time	100	µs
DVDD turn-on delay	200	µs
DVDD OCP threshold	450	mV
PWM and three-phase gate driver[1]		
PWM mode	6 PWM	
PWM freewheeling mode	Active FW	
Brake configuration	Low-side	
Alternate recirculation	Disable	
Pre-charge	Enable	
CS and OCP (for 6EDL7141 and 6EDL7151)		
Amplifier A	Disable	
Amplifier B	Enable	
Amplifier C	Disable	
Amplifier gain	8x	
Amplifier gain analog select	Disable	
Amplifier mode	Shunt resistor	
Internal offset selection	¼ DVDD	
Use external offset	Disable	
Amplifier timing mode	GLx high	
Amplifier blanking time	1000	ns
Amplifier auto zero	Internal trigger	
OCP positive threshold	300	mV
OCP negative threshold	-300	mV
PWM truncation	Enable	
OCP deglitch time	8	µs
OCP fault trigger	8 events	
OCP fault latching	Disable	
Brake on OCP	Enable	
Negative OCP	Enable	

[1] Refer to **Table 2** for parameters not listed here

Housekeeping		
Hall sensor deglitch time	640	ns
Overtemperature shutdown	Enable	
ADC measurement filter	8	
APC PVDD measurement filter	32	
WD timer	Disable	
WD input selection	EN_DRV	
WD fault report	Status register only	
WD period time	100	µs
Buck converter WD	Enable	
Rotor lock detection time	1	s
Rotor lock detection	Disable	
WD fault latching	Disable	
Brake on WD timer overflow	Disable	
WD DVDD restart delay	0.5	ms
WD DVDD restart attempts	0	
User ID	0	
MOSFET fault detection VDS sensing (for 6EDL7151)		
VDS sensing enable	Enable	
VDS fault configuration	Register and nFAULT	
VDS filter	5.0	µs
VDS blanking	5.0	µs
VDS low side threshold	0.65	V
VDS high side threshold	0.65	V

4.4 Using the GUI to operate the board

The GUI is also able to operate and monitor a 6EDL7141-based motor drive inverter such as the EVAL_6EDL7141_TRAP_1SH through its test bench screen, which is shown in **Figure 49**.

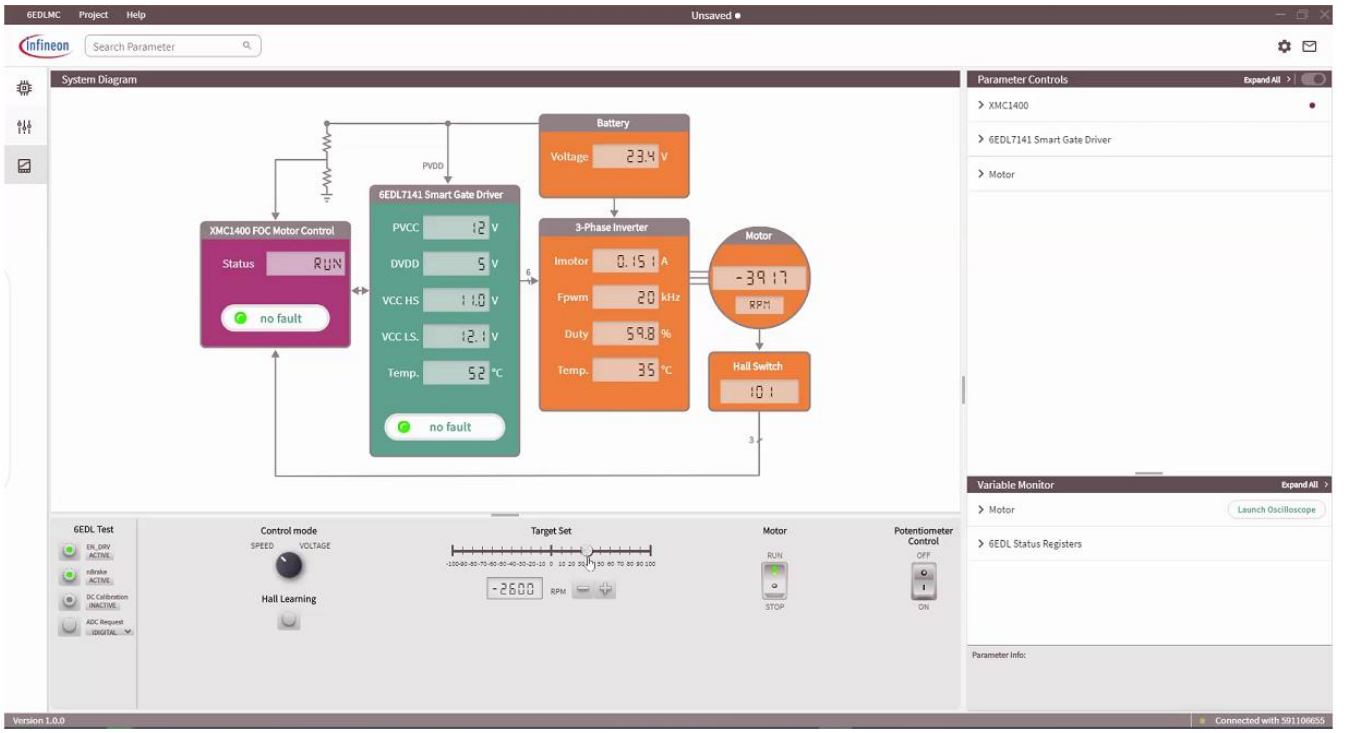


Figure 49 GUI test bench screen

The test bench screen provides a real-time display of the system parameters such as the power supply, internal regulator and charge pump voltages as well as the battery input voltage. It also indicates the rotor revolutions per minute (RPM), the motor current, the PWM switching frequency and duty cycle, and also the 6EDL7141's temperature from its integrated sensor. Fault status is also indicated.

In addition to monitoring, the motor direction and speed can also be commanded from this GUI screen using the "Target Set" slider control in the lower area of the screen. The motor can be started or stopped via the motor switch and the board-mounted speed control potentiometer can also be enabled and disabled. In order to control the speed through the GUI, the potentiometer control switch on the right must be in the off position.

5 PCB layout design guidelines

BLDC motor drive inverters are usually designed on four- or six-layer FR4 boards. To achieve best performance, it is vital to minimize loop inductances and copper losses in the PCB traces. This is done by making the traces as wide as possible and minimizing the HF current loops for the three phases. For each half-bridge, the HF current loop starts at the ceramic HF decoupling capacitors located close to the high-side MOSFET drain. Its path passes through the high-side MOSFET to the switch node and then continues to the drain of the low-side MOSFET and exits from the source, passing through the shunt and then back to the ceramic capacitor ground as shown below:

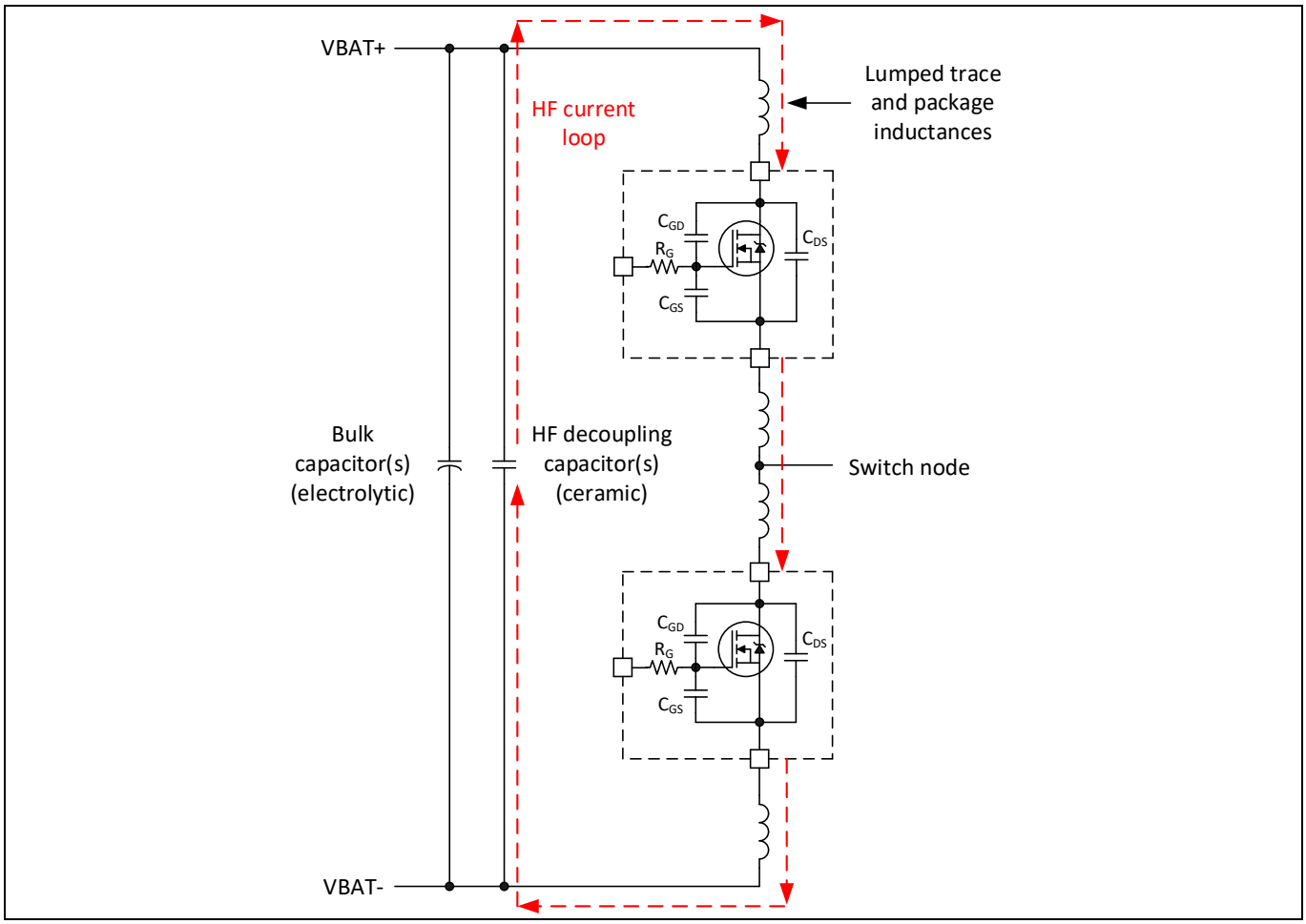


Figure 50 HF switching current path in one phase

Since the majority of the HF component of the current will circulate around this loop, the goal is to make the loop as tight as possible. The recommended strategy for implementing this is to use the top copper layer to connect the DC bus positive (VBAT+) to the high-side MOSFET drains, to connect the high-side sources to the low-side drains and to connect the low-side sources to the shunts. Clearly the high- and low-side MOSFETs need to be placed close together while making provision for the phase connection to the motor at the switch node. The distance between the MOSFETs and HF decoupling capacitors should also be minimized. The power ground return should always be located on the first internal layer, which is closest to the top layer, to minimize the layer separation. The HF decoupling capacitor and shunt ground connections should be connected to the first layer through multiple vias so that the ground return path runs directly beneath the power path on the top layer.

Figure 51 depicts a trace on the top layer, which is viewed by cross-sectional width.

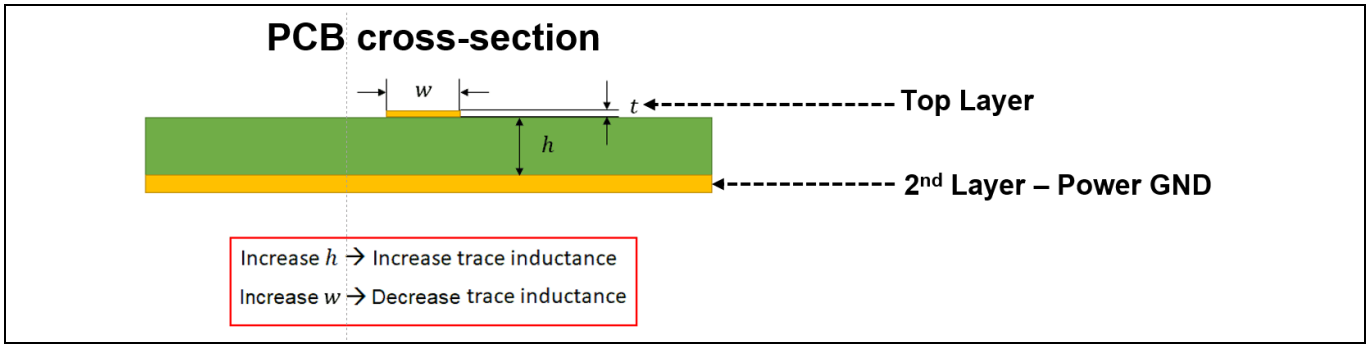


Figure 51 PCB trace inductance between layers

The recommended layout scheme for the top and second layer is as shown in **Figure 52**.

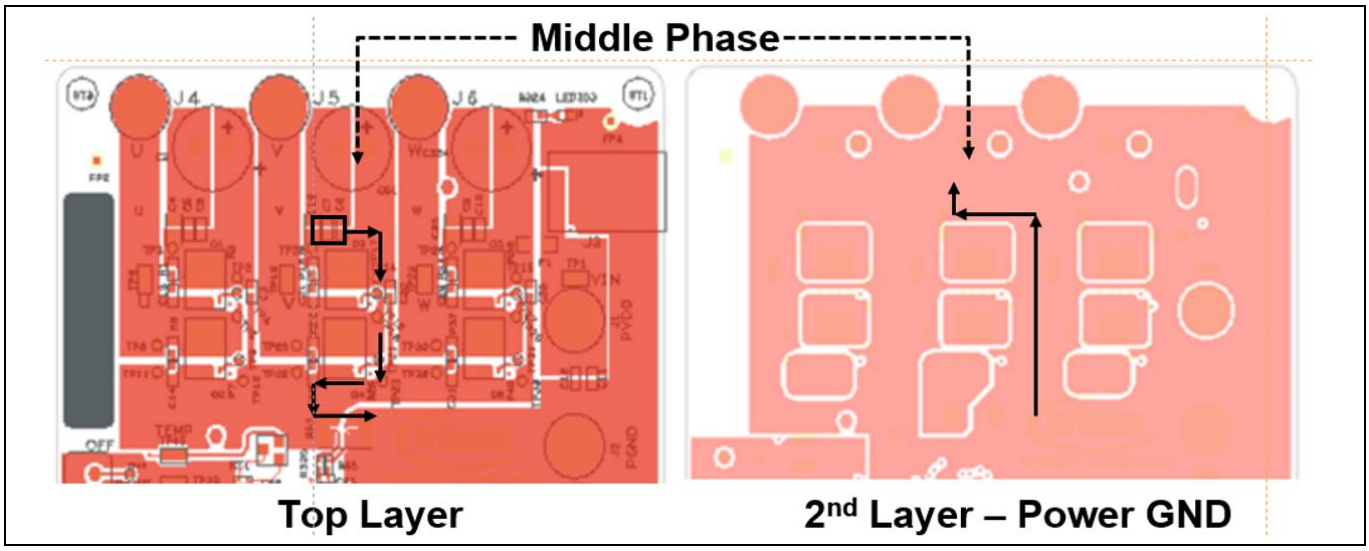


Figure 52 Top and second layer layout optimization

The HF current path for the middle phase (V) is indicated in **Figure 52**, where the black box shows the location of the HF decoupling capacitors.

Layout of the gate drive traces is also critical since incorrect routing of these traces is likely to result in unwanted gate drive oscillations, which prevent the inverter from operating efficiently and produce EMI.

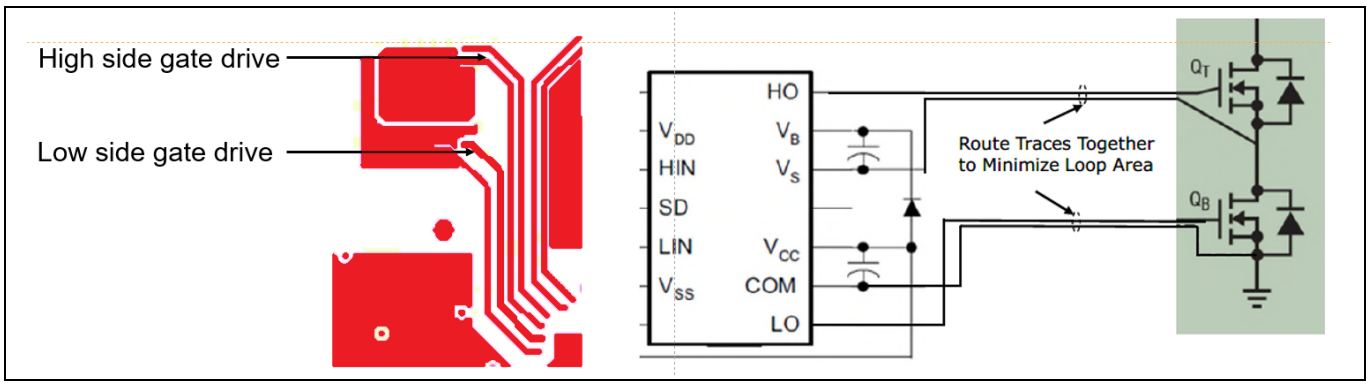


Figure 53 Gate drive trace optimization

To minimize inductance, gate drive traces from the 6EDL71x1 driver outputs to the MOSFET gate connections and return paths should run together as parallel traces on the first layer and be kept as short as possible. This is important when using three-phase gate driver ICs such as the 6EDL71x1 series, since with a single IC package containing all of the gate drivers, it is not possible to locate the driver directly adjacent to each MOSFET.

The PCB layout is optimized to minimize radiated EMI. As mentioned, this is done by keeping the loops carrying the switching currents as small as possible. The HF switching current loops are illustrated in the schematic below. It should be noted that during the switching transition, the high-side gate drive loop current returns to the main ground due to the 6EDL71x1 high-side charge pump. This differs from conventional bootstrap-type high-side drivers, where current returns back to the gate driver. The high-side gate drive loop for the 6EDL71x1 should therefore be kept as tight as possible.

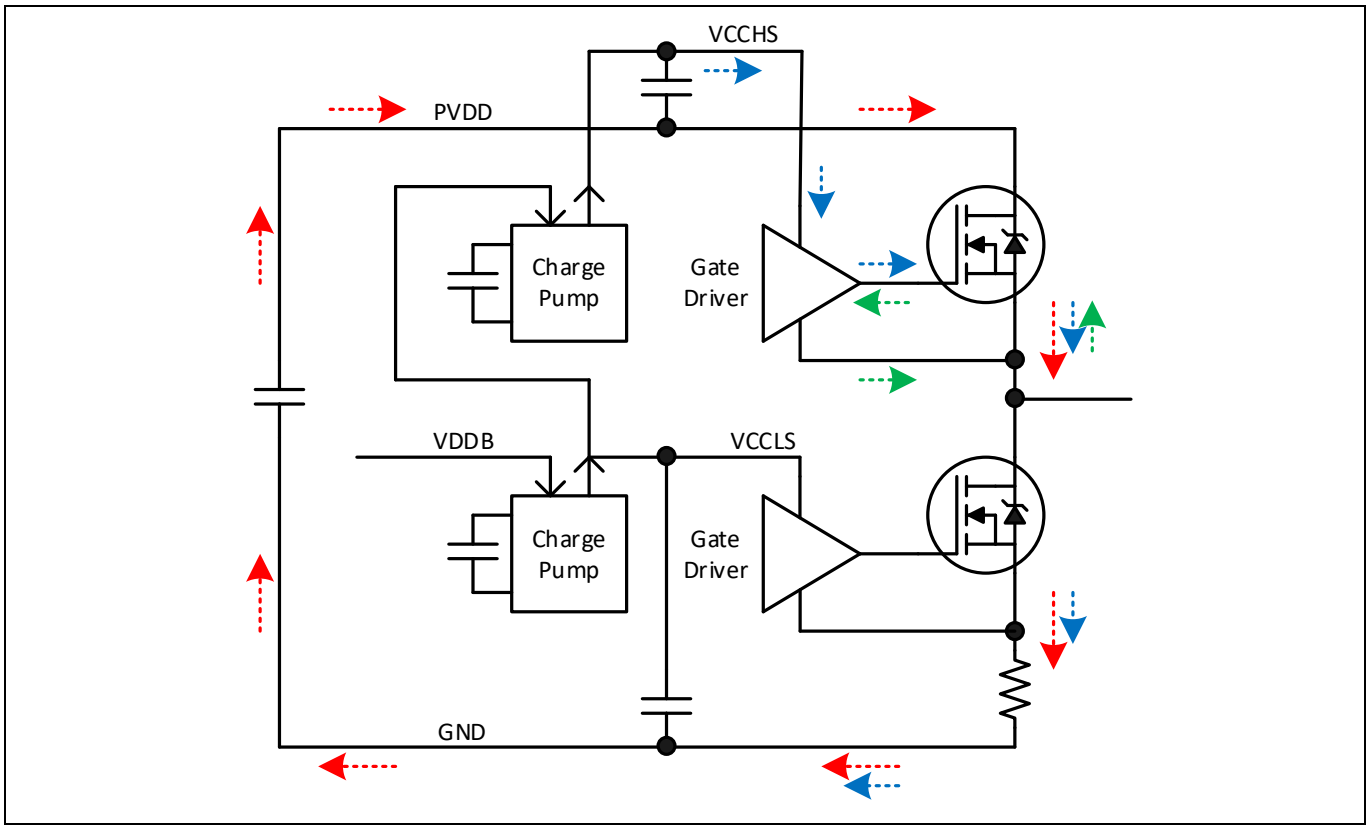


Figure 54 HF current loop for one phase – red: main HF switching loop; blue: high-side gate drive switch on current loop; green: high-side gate drive switch-off current loop

The inverter control circuitry including the microcontroller should have a separate signal ground, which is connected to the power ground only at one point. This should preferably be close to the HF decoupling capacitor ground to minimize noise propagating through the ground which could interfere with digital circuits. The signal ground and traces can be on a different layer. Typically, other available layers are used to provide duplicate high-current paths to reduce DC resistance and heat losses. The bottom layer can be used in a similar way to the top layer for short power traces but should not be used for the HF current loop.

Two-ounce (70 µm) copper layers are recommended to carry high current. These should be used on the top and bottom layers. The inner layers can be 1 or 2 oz. (35 or 70 µm thickness) copper depending on the current carrying requirements.

6 Thermal management

Heatsink design is a critical aspect of motor drive inverter design. It is essential in transferring the heat from the MOSFET die through the package and to the outside. Requirements vary depending on the space available and the form factor and the amount of available airflow. Forced air is sometimes used to transfer heat from the heatsinks, which allows for smaller heatsinks.

When designing a PCB assembly using surface-mount power MOSFET packages mounted on the top side of the PCB, the following heatsinking options are available:

1. Bottom-side cooling (heatsink is mounted the bottom side of the PCB)
2. Top-side cooling (heatsink is mounted on top of the MOSFETs)
3. Dual-side cooling (heatsinks are mounted on both the top and bottom of the PCB)

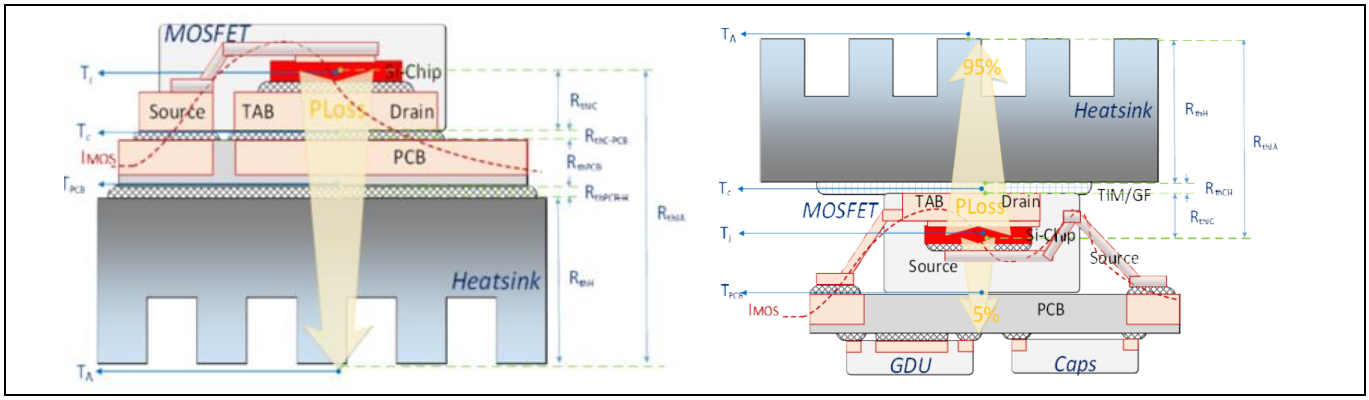


Figure 55 Bottom-side cooling (left), top-side cooling (right)

Bottom-side cooling is the most common scheme used and can be implemented with standard SMD MOSFET packages such as PQFN or D2PAK. Here the heatsink is mounted underneath the MOSFETs on the opposite side of the PCB through a thermal interface material (TIM). Many small vias must be placed under the MOSFETs to allow the transfer of heat through the PCB. The disadvantages are that the thermal resistance of the PCB material produces a temperature difference between the MOSFET packages and the heatsink, and no components can be mounted on the bottom side of the board under the MOSFETs.

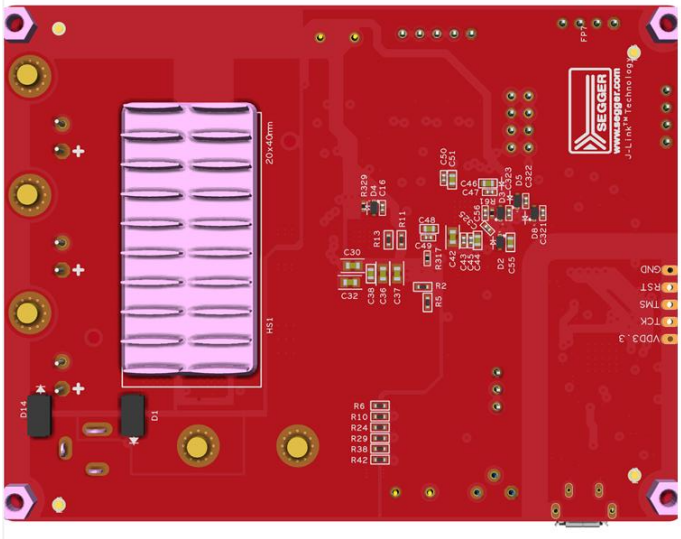


Figure 56 Example board bottom side with heatsink attached

As mentioned previously, thermal vias are added in bottom-side cooled systems to transfer the heat from the die through the bottom of the MOSFET through the PCB to the bottom side. The thermal resistance from the MOSFET junction to the heatsink may be calculated by adding together the different elements of thermal resistance in the path. These elements are analogous to resistors in an electrical circuit. The thermal resistance can be calculated for a single via based on its diameter and length and whether or not it is filled. This value can then be divided by the total number of vias used to obtain the overall thermal resistance of all of the vias RTH_PCB. The size and surface area of the heatsink determines R_{HSK}. With the values of thermal resistance for each element, the temperature rise can be calculated for a specific power loss, which is calculated for the MOSFETs at full load and includes conduction and switching losses.

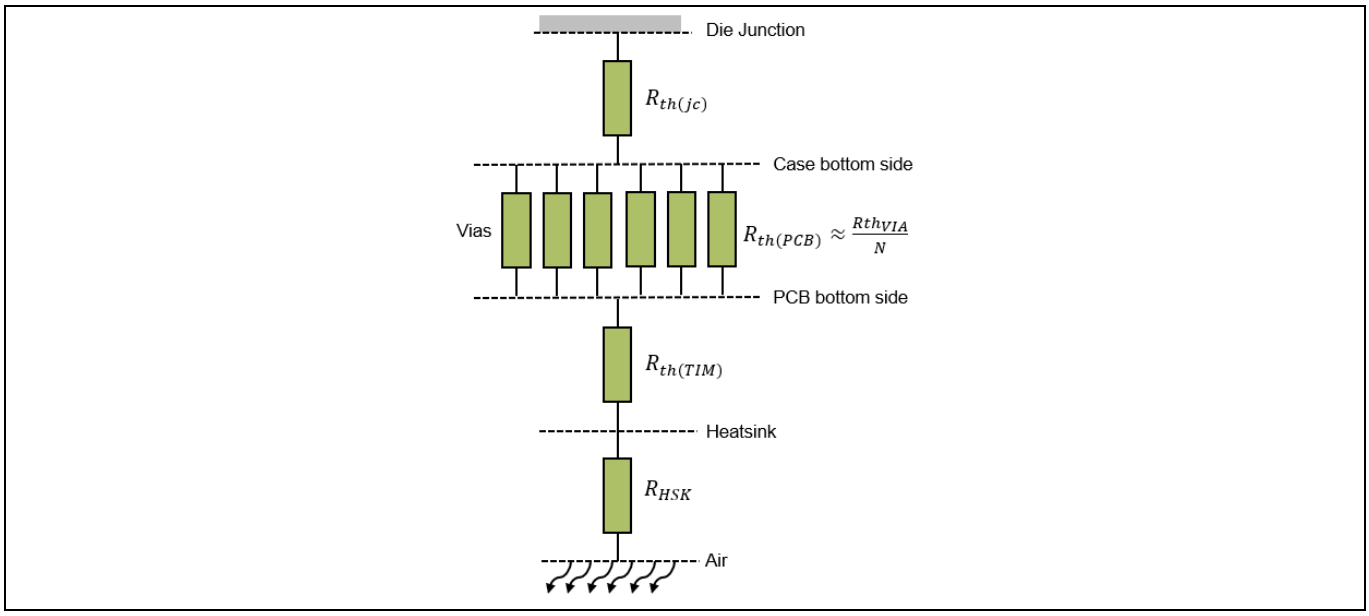


Figure 57 Bottom-side cooling thermal model

The thermal resistance from MOSFET junction to ambient for bottom-side cooling is given by:

$$R_{th(ja)} = R_{th(jc)} + R_{th(PCB)} + R_{th(TIM)} + R_{HSK} \quad [19]$$

Top-side cooling on the other hand, to be most effective, requires packages with top-side exposed metal, such as DirectFET, TOLL-T or top-side cooling versions of PQFN packages. In this scenario, the heatsink is mounted on top of the MOSFETs through the TIM. Since the heat does not have to pass through the PCB material, top-side cooling provides a lower thermal resistance from junction to ambient. This allows more current to be conducted in the MOSFETs, while maintaining the die temperature to acceptable levels.

The thermal resistance from MOSFET junction to ambient for top-side cooling is given by:

$$R_{th(ja)} = R_{th(jc)} + R_{th(TIM)} + R_{HSK} \quad [20]$$

In dual-side cooling configurations, both techniques are combined so that heatsinks are connected on the top and bottom sides. The disadvantage of this scheme is the added cost and mechanical complexity involved in mounting two opposite-facing heatsinks with their associated TIM with the correct amount of torque applied for each side.

Note: ***It should be noted that in all cases where screws are used to attach the heatsinks, the torque applied to tighten each screw should be equal and within the correct range specified for the TIM. Several mounting screws should be placed to achieve even pressure across the various MOSFETs. Overtightening of screws causes PCB material bending and possible TIM damage!***

7 Summary

This application note has provided a detailed guide to battery-powered BLDC design based on the 6EDL71x1 family of smart three-phase gate drivers. It is a general guide, not specific to any one control method or specific 6EDL71x1 gate driver. The configurable gate drive, onboard power supply and protection features have been explained as well as the SPI and associated hardware. Design optimization is made quicker and easier by means of the BPA motor control GUI with its MOSFET tuning design aid, which allows correct tuning of the gate drive parameters to provide the best tradeoff between low switching losses, reduced voltage transients and minimal EMI.

Recommended design practices and tips have also been covered, which include recommendations on component placement, PCB design and layer assignment. An overview of thermal management strategies explains the benefits and disadvantages of bottom- and top-side heatsink mounting.

Designers using the 6EDL71x1 family of drivers are strongly recommended to consult this application note and use it as a guide. We are confident that this will help to save time and avoid issues.

References

[1] Infineon Technologies AG: *MOTIX ™ 6EDL7141*; Datasheet; **Available online**

[2] Infineon Technologies AG: *Evaluation board EVAL_6EDL7141_TRAP_1SH 18 V brushless DC motor drive board*; Application note; **Available online**

[3] Infineon Technologies AG: *MOSFET OptiMOS™ 6 Power-Transistor, 40 V*; Datasheet; **Available online**

[4] Infineon Technologies AG: *Infineon Motor Handbook*; **Available online**

[5] Infineon Technologies AG: *Block commutation vs. FOC in power tool motor control*; Application note; **Available online**

[6] Infineon Technologies AG: *Designing with power MOSFETs (How to avoid common issues and failure modes)*; Application online; **Available online**

[7] Infineon Technologies AG: *Sensored trapezoidal control firmware design in EVAL_6EDL7141_TRAP_1SH*; Application note; **Available online**

[8] Infineon Technologies AG: *BLDC motor control software using XMC™*; Application note; **Available online**

[9] Infineon Technologies AG: *EVAL_IMD700A_FOC_3SH 18 V brushless DC motor drive board*; Application note; **Available online**

[10] Infineon Technologies AG: *PMSM FOC motor control software using XMC™*; Application note; **Available online**

Revision history

Document revision	Date	Description of changes
V 1.0	2023-07-20	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-07-20

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2023 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_2306_PL88_2307_181713

Important notice
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.