

## Using the IRS2982S in a PFC Flyback with opto-isolated feedback

Authors: Peter B. Green

### About this document

#### Scope and purpose

The purpose of this document is to provide a comprehensive guide to using the IRS2982S control IC for LED drivers in a single stage PFC-Flyback converter, which instead of using the transformer auxiliary winding for voltage regulation, uses an opto-isolated secondary feedback circuit for voltage and/or current regulation. The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, with a focus on designing the feedback loop to avoid instability.

#### Intended audience

Power supply design engineers, applications engineers, students.

### Table of Contents

About this document .....	1
Table of Contents .....	1
1 Introduction .....	2
2 IRS2982S functional overview .....	4
3 MOSFET selection .....	6
4 Voltage regulating Flyback converter using the TL431 .....	7
5 Essential design considerations .....	9
6 TL431 example schematic .....	12
7 Dimensioning procedure .....	13
8 Control loop design .....	15
8.1 Plant transfer function .....	15
8.2 Feedback and TL431 error amplifier transfer function .....	20
8.3 Closed loop transfer function .....	22
9 Feedback circuit based on operational amplifiers .....	24
10 Operational amplifier example schematic .....	26
11 PCB layout guidelines for system optimization and EMI reduction .....	30
12 Conclusion .....	31
Revision History .....	31

## Introduction

## 1 Introduction

The IRS2982S is a versatile LED driver IC primarily intended for LED drivers in the 5 to 80 W power ranges, though it may be used up to 150 W. It is suitable for Buck, Buck-Boost and Flyback converters operating in critical conduction mode (CrCM) and discontinuous mode (DCM) at light loads. Flyback converters will be covered in this application note focusing on an isolated voltage regulated design with PFC.

The IRS2982S includes control, protection and gate drive circuitry with a high voltage start-up cell to enable rapid power up over a wide line input voltage range. The IRS2982S is also able to provide power factor correction in a single stage Flyback converter able to meet class C (lighting) line current harmonic limits of the EN61000-3-2 standard.

There are several configurations of Flyback converter that may be used with the IRS2982S depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated.

2. Current or voltage regulation.

In the case of voltage regulation, current limiting is needed for protection against overload or short circuit and in the case of current regulation over-voltage protection is necessary for an open-circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of Flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation feedback may be taken from the auxiliary winding as shown in figure 4 where very accurate voltage regulation is not necessary. An opto-isolator is also necessary for highly accurate voltage regulation.

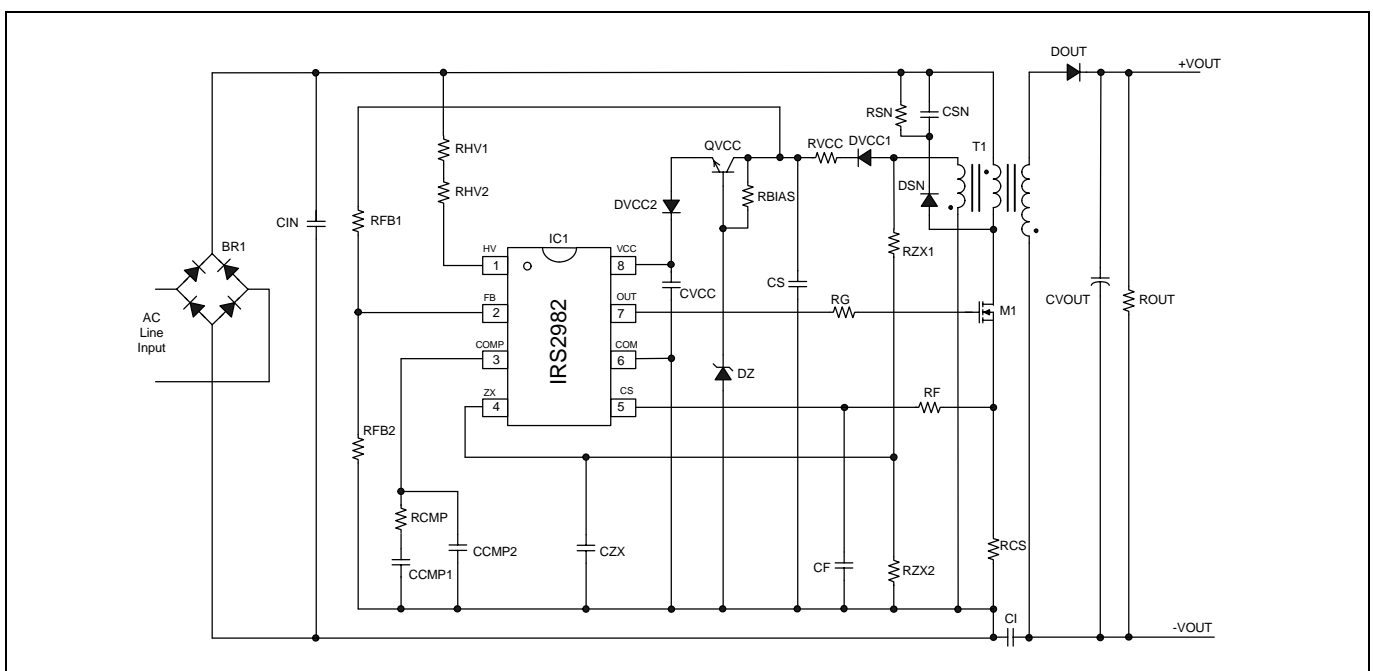


Figure 1 Basic IRS2982S based PFC Flyback converter

## Introduction

The basic circuit in figure 1 shows the main elements of the IRS2982S based PFC Flyback converter. This can be used as a stand-alone power supply or as a front end stage with a current regulating Buck regulator as the back end stage in a dimmable (or non-dimmable) off line LED driver. This front end stage is able to provide a regulated output voltage over a wide range of line and load with sufficient accuracy for the majority of applications. The basic auxiliary winding feedback approach is described in detail in ANEVAL201602 PL16 017, "55 W Flyback converter design using the IRS2982S controller IRXLED04".

This application note will deal with designs where a secondary side regulation circuit is implemented using an opto-isolator for feedback isolation. Such designs are widely used where highly accurate constant current regulation is required.

Some known challenges exist in these types of design such as the tendency for the loop to become unstable and oscillate and the tolerance and variation over time of the opto-isolator current transfer ratio. These topics will be explored and methods for overcoming such limitations will be introduced.

## 2 IRS2982S functional overview

The IRS2982S is comprised of the following functional blocks:

### 1. High voltage start-up cell

The IC internal functional blocks remain disabled in low power mode until VCC first rises above the  $V_{CCUV+}$  under-voltage lock out (UVLO) threshold, continuing to operate while VCC remains above  $V_{CCUV-}$ . VCC is initially supplied through the integrated high-voltage start-up cell, which supplies a controlled current from the HV input provided a voltage greater than  $V_{HVSMIN}$ , is present. The current supplied is limited to  $I_{HV\_CHARGE}$  reducing to less than  $I_{HVS\_OFF}$  when VCC reaches the cut-off threshold  $V_{HVS\_OFF1}$ . The HV start-up cell switches over from *start-up mode* to *support mode* after the feedback input at FB has exceeded  $V_{REG}$  for the first time. In this mode the cut-off threshold becomes  $V_{HVS\_OFF2}$ . During steady state operation under all line-load conditions VCC is supplied through an auxiliary winding on the Flyback transformer with VCC high enough so that the HV start-up in does not supply current. If the auxiliary supply were unable to maintain VCC, the HV start-up cell operating in support mode would supply current to assist.

### 2. PWM controller

The SMPS control section operates in voltage mode where the gate drive output on time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor CCOMP (shown in figure 4) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on time is reached when  $V_{COMP}$  falls to  $V_{COMPOFF}$  below which the gate drive is disabled. Under very light load conditions  $V_{COMP}$  transitions above and below  $V_{COMPOFF}$  to produce burst mode operation. Off time is determined by the demagnetization signal received at the ZX input, which is derived from the auxiliary transformer winding that supplies VCC through a resistor divider. Internal logic limits the minimum off time to  $t_{OFFMIN}$ , therefore the system transitions from CrCM to DCM at light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically after a re-start period of  $t_{WD}$ .

### 3. Protection

The IRS2982S includes cycle by cycle primary over-current protection, which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold  $V_{CSTH}$ . This prevents the possibility of transformer saturation at low line under heavy load but does not protect against output overload or short circuit.

Over-voltage protection is also provided through the ZX input, which provides a voltage proportional to the output voltage. This disables the gate drive output and pulls the COMP voltage below the  $V_{COMPOFF}$  threshold. The error amplifier then starts to charge CCOMP until the gate drive starts up again at minimum on time. Under an open circuit output condition the over voltage protection causes the converter to operate in burst mode preventing the output voltage from rising too high.

The IRS2982S uses an SO-8 package as shown below:

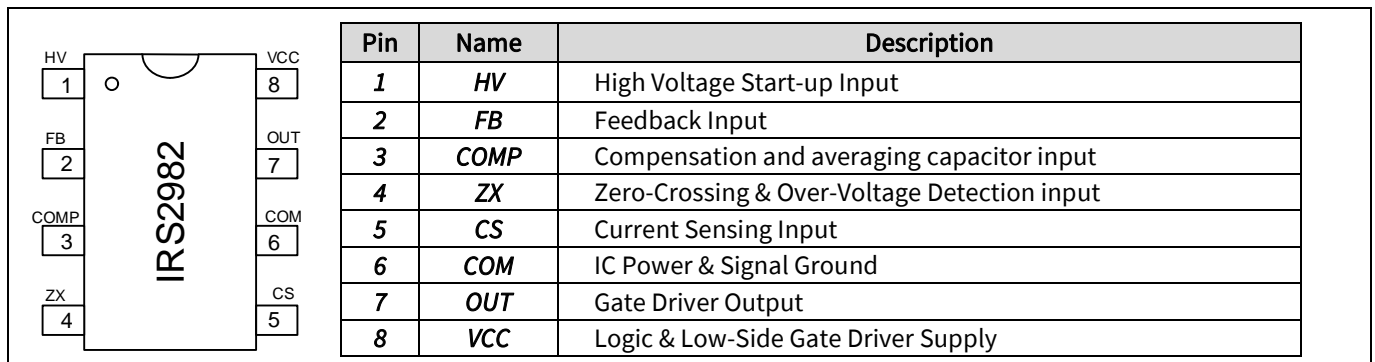


Figure 2 IRS2982S pin assignments

### 3 MOSFET selection

For best efficiency and reliability PFC flyback converter applications designed to operate in the 100 to 265 VAC input voltage range should use MOSFET rated at at least 650 V with  $R_{DS(ON)}$  selected according to the maximum power rating. This accounts for maximum reflected voltage plus switch off transient and allows sufficient margin for ringing. In the case of 277 VAC input converters able to withstand a +10% high line voltage of 305 VAC, a MOSFET rated to at least 700 V is required. The CoolMOS™ P7 series is the latest CoolMOS™ product family and targets customers looking for high performance and at the same time being price sensitive. Though optimizing key parameters ( $C_{oss}$ ,  $E_{oss}$ ,  $Q_g$ ,  $C_{iss}$ , and  $V_{GS(th)}$ ); integrating Zener Diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease-of-use, and price/performance ratio, delivering best-in-class performance with exceptional ease-of-use, while still no compromise in price/performance ratio. The 700V and 800V CoolMOS™ P7 series have been designed for flyback and could also be used in PFC topology; they are not recommended for soft switching topologies where hard commutation could happen due to its body diode ruggedness.

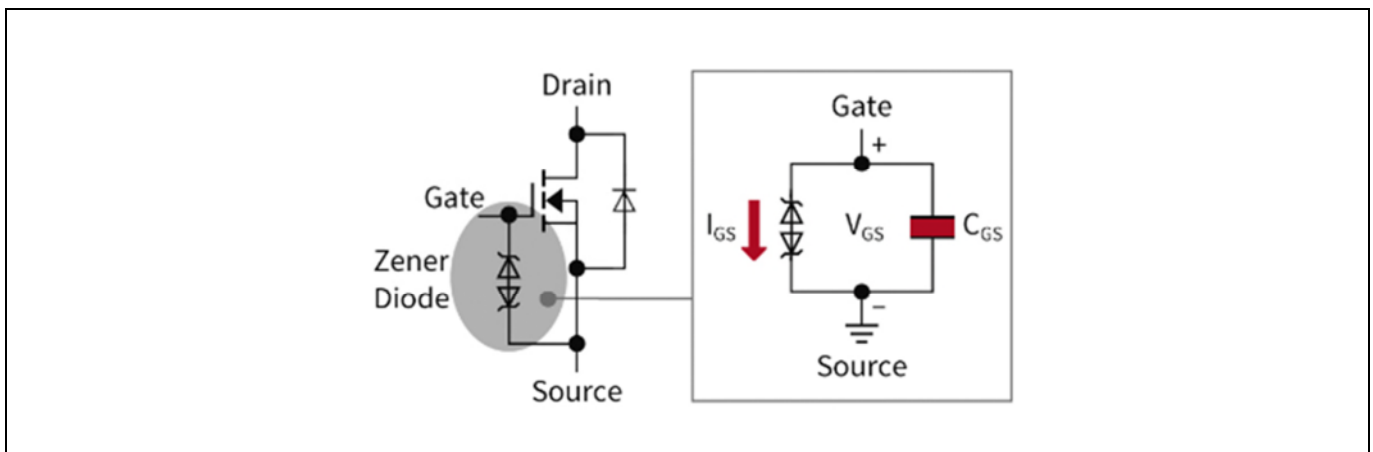


Figure 3 Switching MOSFET gate drive

The 700V and 800V rated CoolMOS™ P7 devices provide excellent performance with additional headroom able to tolerate high drain switch off voltage transients without risk of avalanching. This allows the use of snubber network with minimal power loss to improve converter efficiency.

For applications operating in the 30 to 80 W range the IPP80R450P7 (TO-220) or IPA80R450P7 (FullPAK) is recommended and for applications below 30 W, the IPP80R1K4P7 or IPA80R1K4P7 is recommended. A DPAK version of each of these devices is also available (IPD80R450P7 and IPD80R1K4P7).

For designs in the 80 to 150 W range the IPP80R280P7 or IPA80R280P7 may be used. Heat sinks may be necessary to maintain operating case temperatures below 100°C depending on the power level and choice of device.

## 4 Voltage regulating Flyback converter using the TL431

The well-known and widely used TL431 family of adjustable precision shunt regulators comprises effective, low cost devices available from various semiconductor manufacturers. These three terminal adjustable shunt regulators are available with accuracy options of 0.5%, 1% or 2% over wide operating temperature ranges. They can be thought of as accurate, programmable zener diodes with a very sharp turn on characteristic, whose voltage can be adjusted from 2.5 V to 36 V by means of a resistor divider as shown in figure 3:

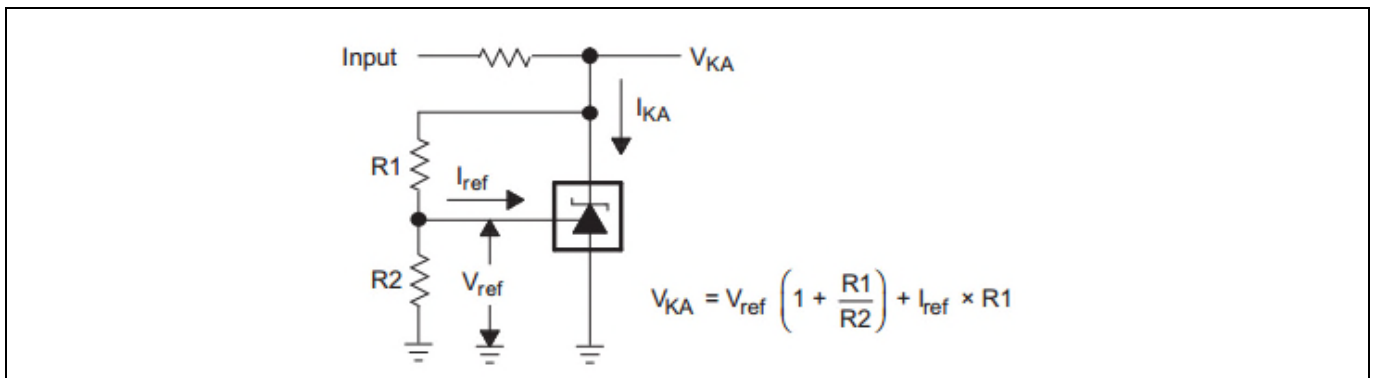


Figure 3 TL431 adjustable shunt regulator

### IMPORTANT:

In order for the device to behave as a shunt regulator, an off-state cathode current  $I_{KA}$  of at least 1 mA is required to provide enough supply to the internal circuitry.

$I_{REF}$  is a small current less than 5  $\mu$ A, which causes some offset in the regulation voltage  $V_{KA}$ . For this reason the value of R1 should not be too large.

When operated with a cathode voltage greater than 2.5 V and bias current  $I_{KA}$  above 1 mA, the TL431 provides a controlled current sink to maintain a cathode voltage, which is then divided down to the fixed reference input of 2.5 V. The TL431 is used like this in place of a voltage reference and operational amplifier to create a secondary side feedback circuit for a power supply.

The reference voltage options of 1.25 V and 2.5 V are normally too high to be suitable for current feedback because the current sensing resistors necessary to generate these voltage levels would dissipate too much power. For example to produce a voltage drop of 2.5 V at 100 mA, a shunt resistor of 25  $\Omega$  would be needed, which would dissipate 0.25 W. There are better solutions available for current regulation, which will be discussed later.

For voltage regulation, the secondary side voltage feedback circuit uses negative feedback to realize an error amplifier with its own reference, which can be set up for type; 1, 2 or 3 loop compensation. An opto-isolator is used to provide isolated feedback to the IRS2982S primary controller. Considerable literature exists to provide detailed theoretical analysis and explanation of these configurations, therefore this application note is limited to providing some practical advice and techniques that can be used in typical LED driver applications.





## 5 Essential design considerations

Please read this section carefully before designing the converter.

### 1. Selection of the opto-isolator

It is of course necessary to select an opto-isolator with sufficiently a high isolation voltage rating to comply with safety standards. A minimum of 4 kV is recommended.

It is also essential to select an opto-isolator with a low current transfer ratio.

The reason for this is that the TL431 used in series with the opto-diode and series resistor  $R_{LED}$ , with an opto isolator has a minimum gain determined by:

$$G_0 > CTR \cdot \frac{R_{PULLUP}}{R_{LED}} \quad [1]$$

2. Where the value  $R_{LED}$  must be low enough to supply sufficient current and therefore  $R_{PULLUP}$  cannot be too high because this would produce too much gain. If the overall feedback gain is too high the system becomes unstable and oscillates due to insufficient phase margin. For this reason an opto-isolator with a CTR of no more than 100% is necessary.

### 3. Selection of critical components

The values of  $R_{LED}$ ,  $R_{BIAS}$ ,  $R_{PULLUP}$  and  $C_{COMP}$  must be selected carefully to ensure stable and reliable operation over the full line-load operating range, while at the same time avoiding significant off time variation during the AC line half-cycle being a necessary condition for high power factor and low iTHD. Designing for stable operation is more challenging in single stage PFC Flyback converters since the cross-over frequency needs to be sufficiently lower than the line frequency to allow “constant” on time operation. It is therefore necessary to model the closed loop transfer characteristics of the system to determine that there will be sufficient phase margin. A MathCAD script has been created to make this task much simpler and less time consuming.

### 4. Ensuring correct start-up operation, **VERY IMPORTANT!**

The presence of  $R_{PULLUP}$  in the circuit adds delay to the IRS2982S initial start-up via its internal high voltage regulator. As previously stated the value of  $R_{PULLUP}$  cannot be too high to achieve a stable system; in a practical system this value may be in the area of 5 k $\Omega$ .

It is very important to account for the fact that during start-up the IRS2982S internal HV start-up cell supplies a limited current of about 3 mA to VCC causing the external VCC capacitor to charge. During under voltage lock out (UVLO), the COMP input is internally connected to ground to ensure that VCOMP will be zero at start-up. This functionality is essential when the IRS2982S is being used in configurations without an opto-isolator, however when an opto-isolator is present with a pull up resistor to VCC there is a potential start-up issue, which needs to be avoided. When the COMP is connected to 0 V, VCC is connected to ground through  $R_{PULLUP}$ . Since  $R_{PULLUP}$  is in the 5 k $\Omega$  range for stable operation in single stage PFC Flyback converters, it diverts some of the available 3 mA of current supplied by the HV start-up cell to ground, delaying charging of the VCC capacitor and at higher ambient temperatures possibly even preventing it from ever reaching the UVLO positive threshold  $V_{CCUV+}$ .

To avoid this problem, it is necessary to place a diode (DVCC2) between the auxiliary supply and VCC and connect  $R_{PULLUP}$  to the anode of this diode so that current from the HV start-up regulator is always blocked from flowing through it. A Schottky diode is recommended to minimize voltage drop. This diode also prevents emitter-base breakdown from occurring during start-up. The following curves show how the HV start-up current is reduced at high temperature:

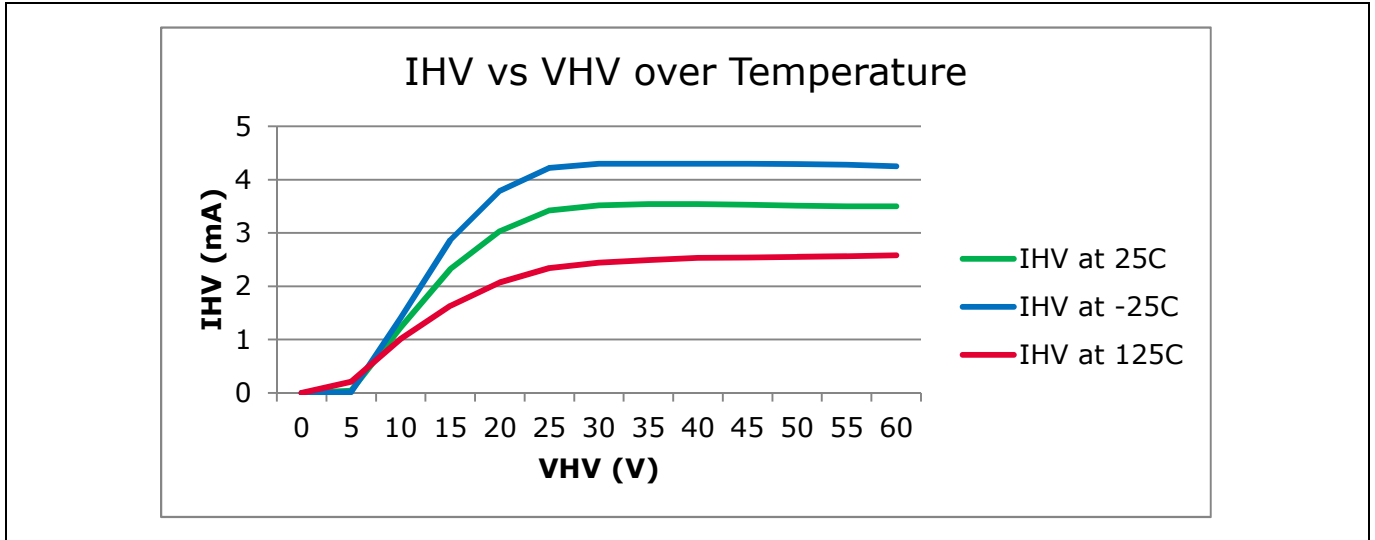


Figure 5 IRS2982S high voltage start-up cell current

The following example shows the start-up behaviour in a typical system comparing performance without DVCC2 present and then with it:

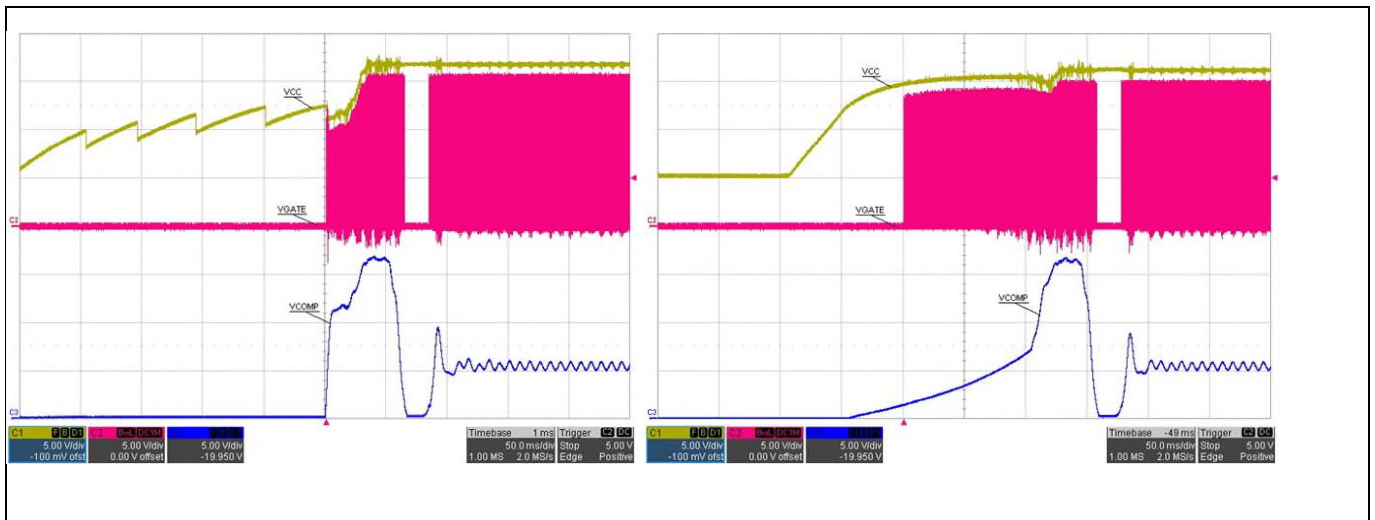


Figure 6 Start-up without DVCC2 (left) and with DVCC2 (right)

In the example where DVCC2 is not included (left), the rise time of VCC is significantly delayed due to the effect of  $R_{PULLUP}$ . In addition there are several sharp drops in VCC caused by emitter-base reverse breakdown occurring in QVCC (Q1). These undesired effects are shown to be overcome by DVCC2 (right).

5. Design of the auxiliary supply and regulator

A simple and reliable auxiliary supply voltage regulator is recommended using an npn transistor emitter follower biased by a zener diode, which provides a voltage limited supply to VCC as a lower cost alternative to an 18 V LDO regulator. Since The IRS2982S has an absolute maximum voltage rating of 20.8 V and a rated maximum of 18 V, an 18 V Zener diode is chosen to set the transistor base voltage providing approximately 17.3 V at the emitter. Where the IRS2982S is used with an opto-isolator, the FB input is connected to ground since the internal trans-conductance error amplifier error is not being used. This being the case, the HV start-up regulator remains in start-up mode at all times and therefore VCC needs to be kept close to 18 V to ensure that its current source is conducting minimal current when the auxiliary supply takes over:

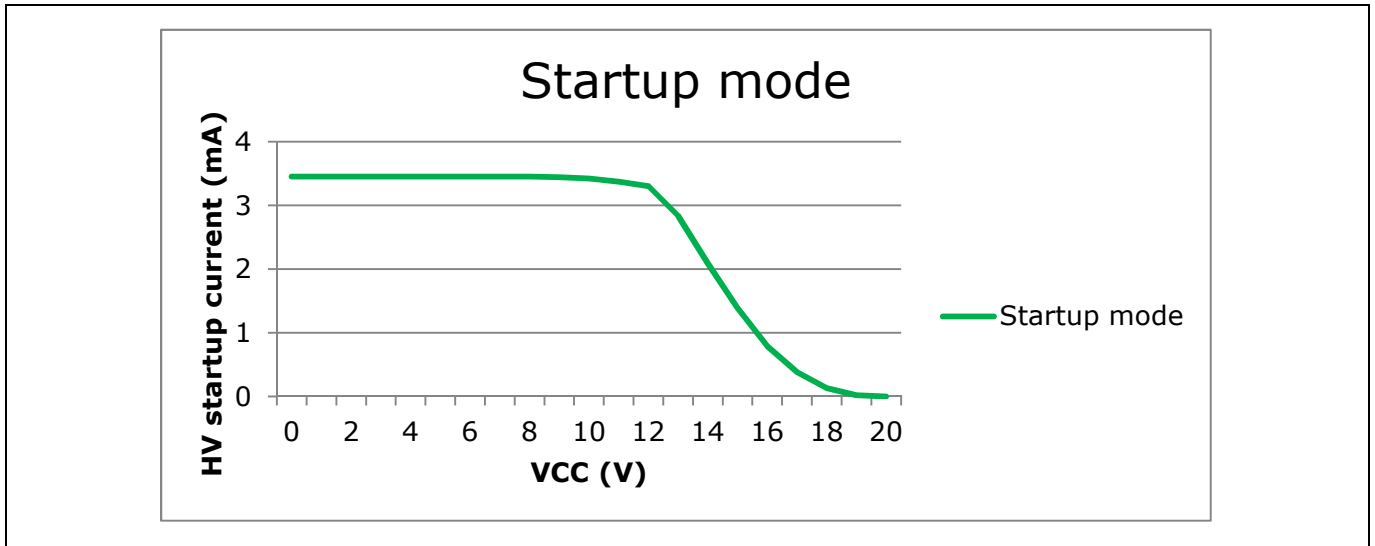


Figure 7 IRS2982S high voltage start-up cell current vs VCC voltage at 25°C

6 TL431 example schematic

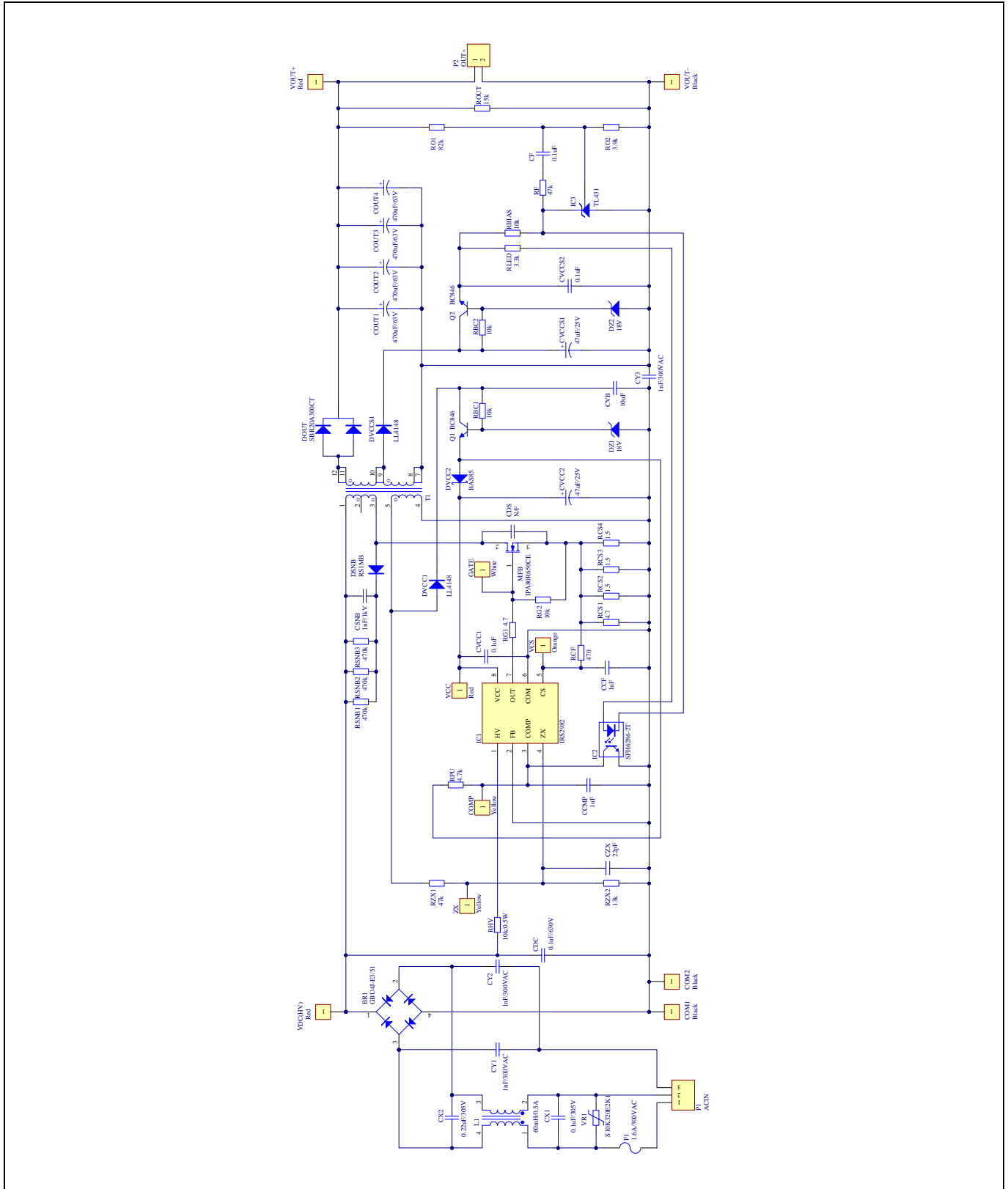


Figure 8 PFC Flyback with opto-isolator and TL431 CV feedback example schematic

## 7 Dimensioning procedure

The Flyback converter is designed for power factor correction with low AC line current total harmonic distortion (iTHD). A typical MOSFET for this type of application is the IPA80R650CE 800 V rated CoolMOS™ device with 650 mΩ on resistance, 45 nC gate charge and low parasitic capacitances in a TO-220 FullPAK. This device is able to withstand high voltage ringing at switch off with minimal added snubber components and has low conduction and switching losses as well low gate drive current.

The output diode has less than 50 ns reverse recovery and a forward voltage drop less than 900 mV at maximum rated current of 10 A at 25 °C temperature, reducing to 700 mV at 150 °C. The blocking voltage is 300 V, necessary to withstand the output voltage under open circuit condition at high line input added to the transformer secondary reflected voltage for a correctly chosen turns ratio.

The Flyback transformer (more accurately described as a coupled inductor) consists of three windings; the primary for energy storage during the on time, the secondary for energy transfer to the output during the off time and the auxiliary, which supplies VCC and provides the required de-magnetization and voltage feedback signals. The IRS2982S (IC1) VCC supply is derived from the transformer auxiliary winding through DVCC1 initially charging CVB then CVCC1 and 2 through RVCC and DVCC2 with DZ to clamp the voltage to protect IC1. Voltage feedback is provided through an opto-isolator from a choice of several secondary feedback circuit options.

The auxiliary winding voltage is proportional to the output voltage so that:

$$V_{AUX} = V_{REF} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = V_{OUT} \cdot \frac{N_A}{N_S} \quad [V] \quad [1]$$

Switching cycle peak current limiting is set by a shunt resistor RCS connected from the MOSFET source to ground to set the peak current according to the threshold VCSTH of 1.2 V. This limits the inrush current during start-up and also protects against damage under over load or short circuit conditions.

The maximum peak current at low line and full load is calculated based on a chosen maximum duty cycle DMAX:

$$I_{P_{MAX}} = \frac{2\sqrt{2} \cdot P_{OUT}}{D_{MAX} \cdot V_{AC_{MIN}} \cdot \eta} \quad [A] \quad [2]$$

The transformer turns-ratio is calculated as follows:

$$N = \frac{N_P}{N_S} = \frac{\sqrt{2} \cdot V_{AC_{MIN}}}{V_{OUT} + V_F} \cdot \frac{D_{MAX}}{1 - D_{MAX}} \quad [3]$$

The primary to auxiliary winding turns-ratio is calculated to provide an auxiliary supply voltage of 20 V:

$$\frac{N_P}{N_A} = \frac{\sqrt{2} \cdot V_{AC_{MIN}}}{V_{AUX} + V_{F(AUX)}} \cdot \frac{D_{MAX}}{1 - D_{MAX}} \quad [4]$$

The transformer primary inductance is calculated according to the formula:

$$L_{PRI} = \frac{V_{AC_{MIN}}^2 \cdot \eta \cdot N \cdot (V_{OUT} + V_F)}{2 \cdot P_{OUT} \cdot f_{MIN} \cdot [N \cdot (V_{OUT} + V_F) + \sqrt{2} \cdot V_{AC_{MIN}}]} \quad [H] \quad [5]$$

### Dimensioning procedure

Where,  $\eta$  is the efficiency assumed to be 0.9 and minimum frequency is typically set to 65 kHz to occur at the peak of the low line input voltage.

The threshold for over voltage protection through the ZX input is given by the resistor divider consisting of RZX1 and RZX2, where  $V_{OVTH}$  is 5.1 V:

$$V_{OUTOV} = \frac{N_P}{N_A} \cdot \frac{1}{N} \cdot V_{OVTH} \cdot \frac{RZX1+RZX2}{RZX2} \quad [V] \quad [6]$$

The maximum reflected voltage appearing at the MOSFET drain is then calculated as follows based on the highest AC line input voltage:

$$V_{DMAX} = \sqrt{2} \cdot V_{ACMAX} + (V_{OUT(MAX)} + V_F) \cdot N \quad [V] \quad [7]$$

It is recommended to allow 30% headroom on top of the reflected voltage to accommodate the switch off transient and high voltage ringing. This requires a MOSFET with a minimum drain-source maximum rating of 765 V and therefore an 800 V part has been selected.

The maximum low frequency output ripple can be calculated as follows:

$$V_{RIPPLE} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(min)} \cdot C_{OUT}} \quad [V_{pp}] \quad [8]$$

Alternatively the capacitor value can be calculated according to the desired maximum ripple:

$$C_{OUT} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(min)} \cdot V_{RIPPLE}} \quad [F] \quad [9]$$

## 8 Control loop design

The basic closed loop system is represented by the following:

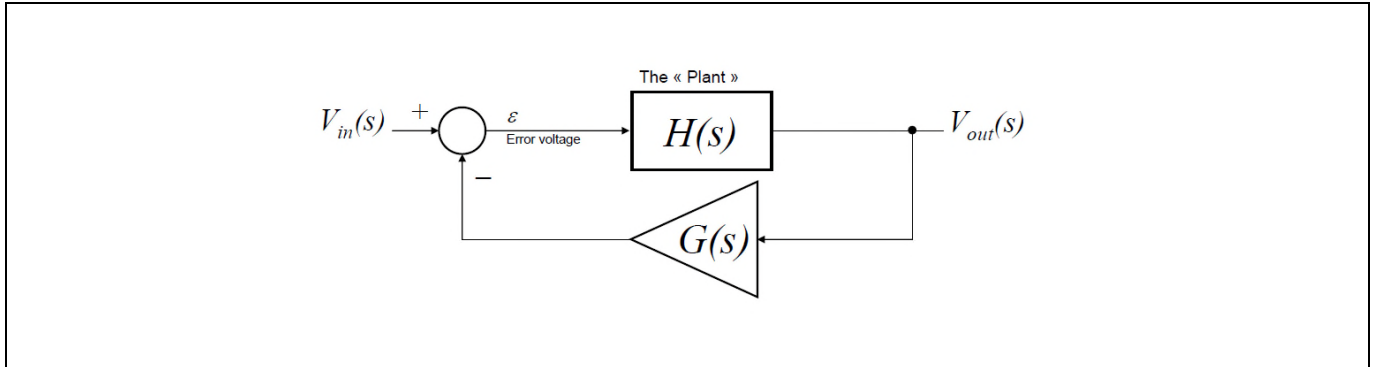


Figure 9 Closed loop system block diagram

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{H(s)}{1+H(s) \cdot G(s)} \quad [10]$$

Where  $H(s)$  is the gain of the converter power stage or “plant”,  $G(s)$  is the feedback gain and the loop gain  $T(s)$  is equal to  $H(s) \cdot G(s)$ . The system will oscillate if the magnitude of  $T(s)$  is equal to unity (0 dB) and the phase shift is  $180^\circ$  creating positive feedback where  $T(s) = -1$ . To design a stable system it is necessary to have sufficient phase margin at the cross-over frequency  $f_c$  where  $|T(s)| = 0$  dB and gain margin when the phase,  $\arg T(s)$  reaches  $-180^\circ$ .

In the Flyback converter the plant transfer function  $H(s)$  is represented by the IRS2982S COMP pin voltage  $V_{COMP}(s)$  to output voltage  $V_{OUT}(s)$  transfer characteristic and the feedback transfer function,  $G(s)$  by that of the  $V_{OUT}(s)$  to  $V_{COMP}(s)$  feedback circuit.

The IRS2982S COMP pin voltage determines the switching on time. The off time is determined by transformer de-magnetization and therefore varies depending on the AC line voltage, phase and load. The relationship between the COMP pin voltage and the on time is not linear and clearly the relationship between the on time and the duty cycle varies. It is therefore necessary for stability analysis that the small-signal transfer function must be determined at a specific operating point. Once this is accomplished the closed loop transfer function for the system may be constructed by multiplying the transfer functions of each of the relevant stages. To check system stability of the system the phase and gain margins may then be calculated. This must be done at each of the line and load operating point corners to ensure stability over the operating range.

### 8.1 Plant transfer function

The voltage mode Flyback converter operating in discontinuous (DCM) or critical conduction/boundary (CrCM/BCM) mode has a basic error amplifier output to output voltage small-signal transfer characteristic with a single pole formed by the output capacitor and load resistance and a zero formed by the output capacitor ESR:

$$F(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} \approx \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1 + \frac{s}{\omega_{z0}}}{1 + \frac{s}{\omega_{po}}} \quad [11]$$

## Control loop design

Where,

$$\omega_{po} = \frac{2}{R_{LOAD} \cdot C_{OUT}}, \quad R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} \quad \text{and} \quad \omega_{zo} = \frac{1}{R_{ESR} \cdot C_{OUT}}$$

The ESR zero occurs at a relatively high frequency and does not come into play in PFC Flyback converters, since these have a much slower loop speed than converters operating from DC that are required to compensate rapidly to step changes in line or load.

The plant transfer function may therefore be simplified to:

$$F(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} \approx \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1}{1 + \frac{s}{\omega_{po}}} = \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1}{1 + \left(\frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2}\right)} \quad [12]$$

While the pole can be easily calculated at each specific load, the relationship between  $V_{OUT}$  and  $V_{COMP}$  is not linear and depends on several system parameters, making it necessary to evaluate it at each operating point at which the small signal stability analysis is to be done.

For the Flyback converter operating in DCM the plant transfer characteristic is as follows:

$$\frac{V_{OUT}(s)}{d(s)} = \frac{V_{IN(RMS)}}{\sqrt{k}} \cdot \frac{1}{1 + \left(\frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2}\right)} \quad [13]$$

Where,

$$k = \frac{2 \cdot L_S}{R_{LOAD} \cdot T_S} = \frac{2 \cdot \frac{N_S}{N_P} \cdot L_P}{R_{LOAD} \cdot (T_{ON} + T_{OFF})} \quad [14]$$

Duty cycle depends on the input and output voltages and the transformer turns ratio. It varies during the line cycle so, for convenience the duty cycle operating point is evaluated at 45° phase angle where the instantaneous voltage is equal to the RMS voltage:

$$D = \frac{1}{1 + \left(\frac{V_{IN(RMS)}}{V_{OUT} + V_F}\right) \cdot \left(\frac{N_S}{N_P}\right)} \quad [15]$$

$T_{ON}$  is constant and can be evaluated according to:

$$T_{ON} = \frac{L_P \cdot P_{OUT}}{\eta \cdot V_{IN(RMS)}^2 \cdot D} = \frac{L_P \cdot V_{OUT}^2}{\eta \cdot V_{IN(RMS)}^2 \cdot R_{LOAD} \cdot D} \quad [16]$$

$T_{OFF}$  varies with the full wave rectified bus voltage so it is also evaluated at a phase of 45°:

$$T_{OFF} = \frac{\left(\frac{N_S}{N_P}\right) \cdot V_{IN(RMS)} \cdot T_{ON}}{V_{OUT} + V_F} \quad [17]$$



From equations (13) through (17) the small-signal duty cycle to output voltage transfer function can be evaluated at the operating point. The relationship between  $V_{COMP}$  and the  $T_{ON}$  for the IRS2982S is shown below:

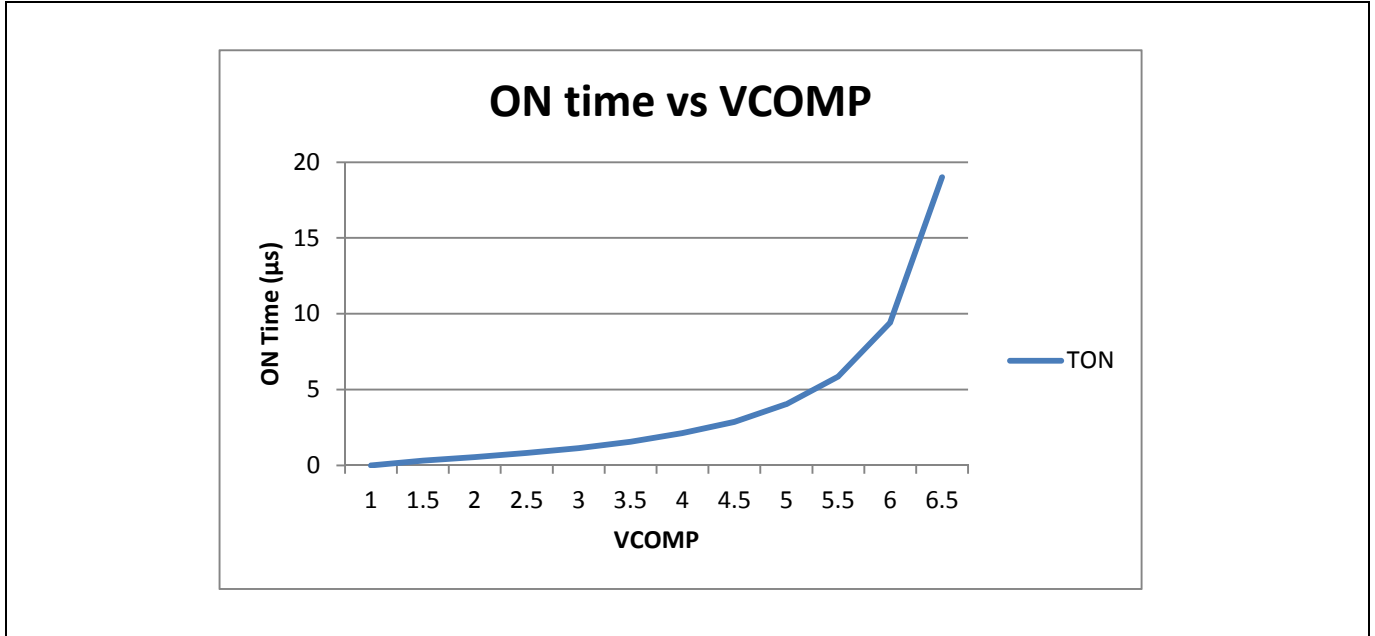


Figure 10 On time as a function of VCOMP

The relationship is non-linear, defined by the polynomial equation by curve fitting:

$$T_{ON} \approx 0.0178 \cdot V_{COMP}^6 - 0.3463 \cdot V_{COMP}^5 + 2.6845 \cdot V_{COMP}^4 - 10.426 \cdot V_{COMP}^3 + 21.192 \cdot V_{COMP}^2 - 20.642 \cdot V_{COMP} + 7.5426 \quad [18]$$

The derivative of this equation can be used to arrive at, which provides the small signal relationship at any operating point up to an on time of  $\sim 20\mu\text{s}$ :

$$\frac{\delta T_{ON}}{\delta V_{COMP}} \approx 0.1068 \cdot V_{COMP}^5 - 1.7315 \cdot V_{COMP}^4 + 10.738 \cdot V_{COMP}^3 - 31.278 \cdot V_{COMP}^2 + 42.384 \cdot V_{COMP} - 20.642 \quad [19]$$

Since

$$d = \frac{T_{ON}}{T_{ON} + T_{OFF}} \quad [20]$$

therefore,

$$\delta d = \frac{\delta T_{ON}}{T_{ON} + T_{OFF}} \quad [21]$$

Then

$$\frac{\delta d}{\delta V_{COMP}} \approx \frac{(0.1068 \cdot V_{COMP}^5 - 1.7315 \cdot V_{COMP}^4 + 10.738 \cdot V_{COMP}^3 - 31.278 \cdot V_{COMP}^2 + 42.384 \cdot V_{COMP} - 20.642)}{T_{ON} + T_{OFF}} \quad [22]$$

## Control loop design

VCOMP can be determined by extrapolating from figure 7 according to the on time operating point.

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} = \frac{\delta d}{\delta V_{COMP}} \cdot \frac{V_{IN(RMS)}}{\sqrt{k}} \cdot \frac{1}{1 + \left( \frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2} \right)} \quad [23]$$

By combining all of the above equations, the plant transfer function can be determined for a given set of conditions. From there the Bode plot can be generated for the control to output power conversion stage, which is valid for the specified operating point.

It is convenient to use MathCAD to generate the transfer function based on the input parameters as shown in the following example:

### General for of Flyback converter control to output transfer function

Vac\_low := 180 Minimum AC line input voltage

Lp := 250 · 10<sup>-6</sup> Transformer primary inductance

n := 1 Transformer turns ratio, Np/Ns

Pout\_max := 80 Iout\_max :=  $\frac{Pout\_max}{Vout} = 0.43$  Vf := 1 Output diode forward voltage

### Simplified model for control output (plant) transfer characteristic:

Pout := 80 Iout :=  $\frac{Pout}{Vout} = 0.43$  Rload :=  $\frac{Vout}{Iout} = 431.675$

ΔVripple := 10 fin := 50

### Output capacitors:

Cout\_min :=  $\frac{Pout}{2 \cdot \pi \cdot fin \cdot \Delta Vripple \cdot Vout} = 1.37 \times 10^{-4}$  Cout\_min\_uF := 10<sup>6</sup> · Cout\_min = 137.03

### Actual Value of Cout:

Cval := 82 · 10<sup>-6</sup> Ncaps := 2 Cout := Ncaps · Cval = 1.64 × 10<sup>-4</sup>

DF := 0.15 Resr :=  $\frac{DF \cdot (Ton + Toff)}{2 \cdot \pi \cdot Cout}$  ΔVripple :=  $\frac{Iout}{2 \cdot \pi \cdot fin \cdot Cout} = 8.356$

## Control loop design

IRS2982S on time against COMP voltage:

$$T_{on}(v) := \begin{cases} (0.0178v^6 - 0.3463v^5 + 2.6845v^4 - 10.426v^3 + 21.192v^2 - 20.642v + 7.5426) & \text{if } v > 1.4 \\ 0 & \text{otherwise} \end{cases}$$

$$D := \frac{1}{1 + \frac{V_{ac\_low}}{V_{out} + V_f} \cdot n} = 0.509$$

$$T_{on} := \frac{L_p \cdot V_{out}^2}{\eta \cdot V_{ac\_low}^2 \cdot R_{load} \cdot D} = 1.347 \times 10^{-6} \quad T_{off} := \frac{n \cdot V_{ac\_low} \cdot T_{on}}{V_{out} + V_f} = 1.297 \times 10^{-6}$$

$$k := \frac{2 \cdot n \cdot L_p}{R_{load} \cdot (T_{on} + T_{off})} = 0.438$$

$$\delta D(v) := \begin{cases} \frac{0.1068v^5 - 1.7315v^4 + 10.738v^3 - 31.278v^2 + 42.384v - 20.642}{(T_{on} + T_{off}) \cdot 10^6} & \text{if } v > 1.4 \\ 0 & \text{otherwise} \end{cases}$$

Extrapolate COMP voltage:

$$v := 3$$

Given

$$T_{on}(v) = T_{on} \cdot 10^6$$

$$V_{cmp} := \text{Minerr}(v) = 3.298$$

$$\delta D_{\delta V_{cmp}} := \delta D(V_{cmp}) = 0.36$$

Control to output (plant) transfer function DC gain at the operating point:

$$F_o := \delta D_{\delta V_{cmp}} \cdot \frac{V_{ac\_low}}{\sqrt{k}} = 97.857$$

Output Pole:

$$\omega_{po} := \frac{2}{R_{load} \cdot C_{out}}$$

ESR Zero:

$$\omega_z := \frac{1}{R_{esr} \cdot C_{out}}$$

$$F(s) := F_o \cdot \frac{1 + s \cdot R_{esr} \cdot C_{out}}{1 + \frac{s \cdot C_{out} \cdot R_{load}}{2}}$$

Control to output transfer function  
(Change in  $V_{out}$  as a function of change in  $V_{comp}$ )

## Control loop design

## 8.2 Feedback and TL431 error amplifier transfer function

The next stage is to determine the component values for the error amplifier and feedback network mentioned in 1-3 of section 4 and illustrated in figure 4. Since for power factor correction the gain must be reduced to a low level below the line frequency to prevent pulse width modulation from occurring within the line frequency half cycle the values must be chosen very carefully. The choice is somewhat restricted by the opto-isolator CTR, which should be no more than 100% in this type of design, and lower if possible.

The feedback circuit gain is denoted as:

$$G(s) = \frac{V_{COMP}(s)}{V_{OUT}(s)} \quad [24]$$

The feedback circuit gain is flat over the range from a low frequency zero up to a higher frequency pole. The mid band gain between these frequencies provides the necessary dynamic response to prevent overshoot during start-up, however it has to be kept low enough to avoid instability. The mid band gain is given by the following formula:

$$G_0 = \frac{R_{PULLUP} \cdot (R_{UPPER} + R_F) \cdot CTR}{R_{LED} \cdot R_{UPPER}} \quad [25]$$

Referring back to the MathCAD tool:

**Input parameters:**

$$R_{upper} := 220 \cdot 10^3$$

$$R_{lower} := 3 \cdot 10^3$$

$$V_{out} := \frac{R_{upper} + R_{lower}}{R_{lower}} \cdot V_{ref} = 185.833$$

$$V_{comp\_min} := 1.4$$

$$V_{supply} := 15$$

Secondary supply rail for opto isolator

$$V_{cc} := 15$$

Primary VCC supply rail

$$\eta := 0.9$$

Efficiency

$$V_{diode} := 1$$

Opto-diode forward voltage drop

$$CTR := 100 \cdot 10^{-2}$$

Opto-isolator current transfer ratio (expressed as a percentage x 10<sup>-2</sup>)

$$R_{led} := 2.7 \cdot 10^3$$

$$R_{bias} := 10000 \cdot 10^3$$

$$R_f := 47 \cdot 10^3$$

$$C_{zero} := 1 \cdot 10^{-6}$$

TL431 series RC feedback

$$R_{pullup} := 4.7 \cdot 10^3$$

$$C_{pole} := 0.1 \cdot 10^{-6}$$

(Connected from COMP to GND)

The above parameters are entered; where RUPPER and RLOWER refer to the voltage divider resistors RO1 and RO2 in the schematic (figure 5). Czero refers to CF and Cpole refers to CCMP.

## Control loop design

Calculate feedback circuit transfer function:

$$R_{led\_max} := \frac{V_{supply} - V_{diode} - V_{ref}}{V_{cc} - V_{comp\_min}} \cdot R_{pullup} \cdot CTR = 3.974 \times 10^3 \quad \text{Rbias connected to supply not across LED!}$$

$$I_{led\_max} := \frac{V_{supply} - V_{diode} - V_{ref}}{R_{led}} = 4.259 \times 10^{-3}$$

$$I_{431k\_max} := I_{led\_max} + \frac{V_{supply} - V_{ref}}{R_{bias}} = 4.261 \times 10^{-3}$$

The first step is to calculate the maximum possible value of  $R_{LED}$  based on the values of  $R_{PULLUP}$  and the current transfer ratio. The mid band gain is then calculated:

Mid band gain:

Reduce the gain as much as possible below the line frequency for PFC

$$G_o := -\frac{R_{pullup} \cdot (R_f + R_{upper})}{R_{led} \cdot R_{upper}} \cdot CTR \quad G_o = -2.113 \quad dB(G_o) = 6.496$$

The transfer function for the feedback loop and compensator is given by:

Compensator transfer function:

$$G(s) := -\left(\frac{s \cdot R_{upper} \cdot C_{zero} + 1}{s \cdot R_{upper} \cdot C_{zero}}\right) \cdot \left(\frac{1}{1 + s \cdot R_{pullup} \cdot C_{pole}}\right) \cdot G_o$$

Zero location:

$$f_z := \frac{1}{2 \cdot \pi \cdot R_{upper} \cdot C_{zero}} = 0.723 \quad \text{Hz}$$

Pole location:

$$f_p := \frac{1}{2 \cdot \pi \cdot R_{pullup} \cdot C_{pole}} = 338.628 \quad \text{Hz}$$

Having determined both the  $F(s)$  and  $G(s)$  a Bode plot is generated showing the magnitude of the gain and the phase shift in degrees for  $F(s)$  and  $G(s)$  separately and for the total loop gain  $F(s) \cdot G(s)$  where the gains expressed in dB are added together as are the phases.

The phase margin is then calculated by extrapolating the phase difference between the total loop gain and  $-180^\circ$  at the 0 dB cross-over frequency. By entering different values of  $P_{out}$  the phase margin may be checked under different load conditions.

$$P_{out} := 80 \quad I_{out} := \frac{P_{out}}{V_{out}} = 0.43 \quad R_{load} := \frac{V_{out}}{I_{out}} = 431.675$$

### 8.3 Closed loop transfer function

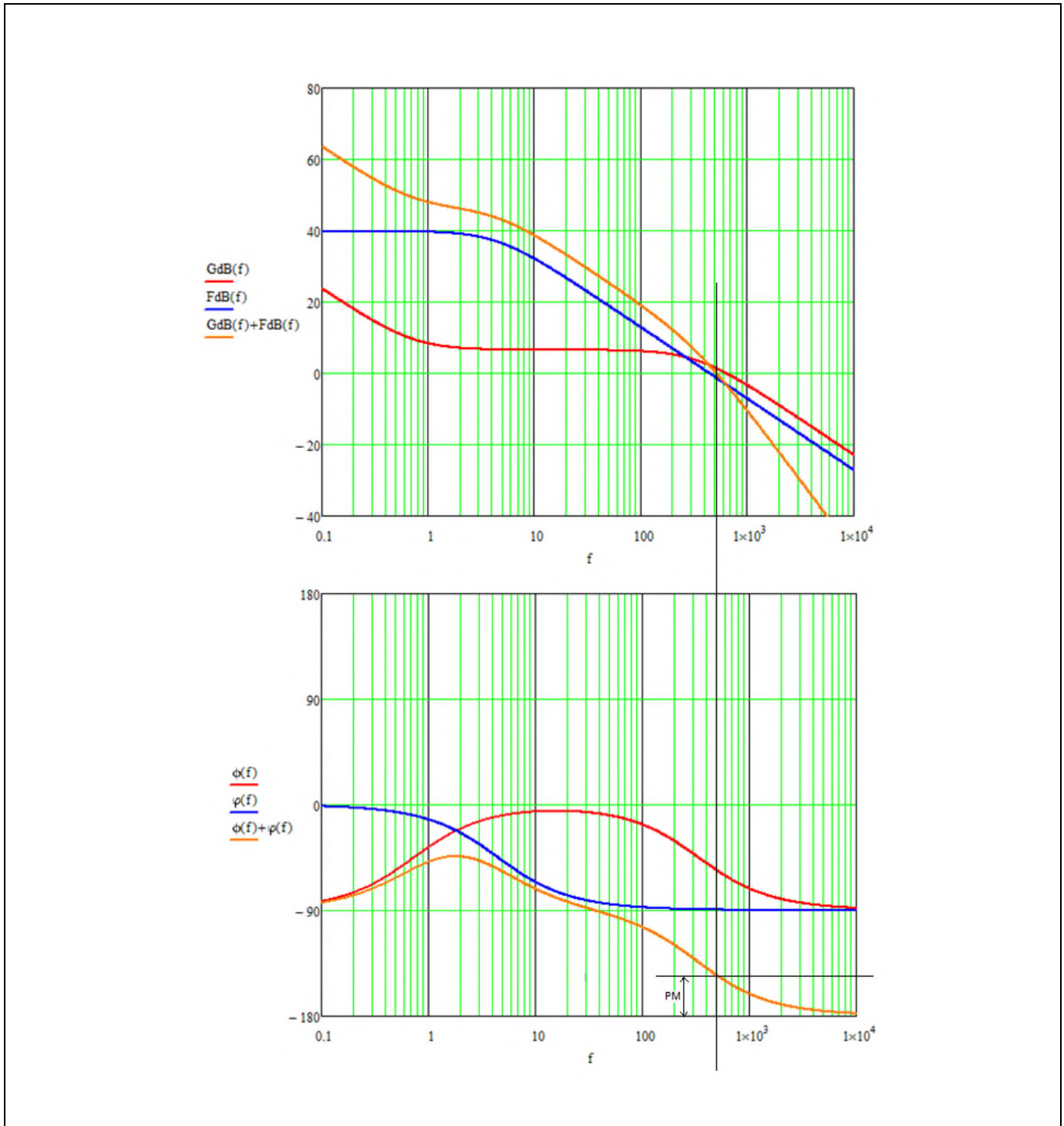


Figure 11 System Bode plots (Gain and Phase)

## Control loop design

Extrapolate crossover frequency and calculate phase margin:

$$f_c := 20$$

Given

$$F_{dB}(f_c) + G_{dB}(f_c) = 0$$

$$f_c := \text{Minerr}(f_c) = 512.444$$

$$PM := 180 + (\varphi(f_c) + \phi(f_c)) = 33.891$$

A phase margin a little above 30° may be the best result possible within the constraints of the topology and components. This will result in an under-damped system however it will not be unstable and will not oscillate.

## 9 Feedback circuit based on operational amplifiers

Though the TL431 solution is very popular for constant voltage regulating designs due to its simplicity and low cost, it is unsuitable for most current feedback applications because of its 2.5 V threshold. A 1.25 V version is also available but this is still too high for most applications.

Instead of using the TL431 many designs use operational amplifiers in conjunction with temperature compensated accurate voltage reference ICs. There are also ICs available which include the voltage reference and two error amplifiers. Designs based on this approach are less problematical since the gain of the error amplifier can be made small enough to provide adequate phase margin for stable operation.

Figure 12 shows an example of a current regulated PFC flyback LED driver, which provides a constant 600 mA up over a range of 30 to 50 V. R21 senses the LED current producing 162 mV feedback voltage in steady-state operation. A dual operational amplifier is used with the first stage (IC2A) providing a DC gain of 15.3 to provide a proportional DC feedback voltage close to 2.5 V. The second operational amplifier (IC2B) forms the error amplifier with a type 1 integrator to drive the opto-isolator diode.

A voltage regulated converter is implemented differently by using one operational amplifier for voltage feedback creating two separate error amplifiers one for voltage regulation and the other for current. Each has its own compensation network and reference and the outputs are OR'd together through diodes to supply sinking current for the opto-diode.

In figure 12 a reference voltage of 0 to 2.5 V is provided at the non-inverting IREF input at pin 5. In this example the LED driver is dimmable using a 0-10 V control input. The 0-10 V input may be referenced to the converter secondary output side since this is already safety isolated from the live parts in the primary circuit, which allows a very simple dimming interface circuit to be used. The TL431 (IC4) in this circuit does not form part of the feedback circuit, it is used to provide a 10V clamp for the 0-10 V dimming input. This input is pulled to maximum by connection through R24 to the secondary VCC supply, ensuring full output when the dimming interface is not connected. The secondary VCC supply is derived through Q2, which maintains a 17.4 V supply for IC2, IC3 and the dimming interface regardless of the LED load voltage.

Since there is no bias current needed as in the TL431 example, the IRS2982S COMP input pull-up resistor R14 can be a higher value. R16 is added to prevent the COMP pin from ever being pulled down below the cut-off threshold  $V_{COMP\ OFF}$ . This is necessary to set the minimum dimming level where there the system will not enter burst mode and there will be no flicker.

In this case the feedback and compensation circuit small signal transfer function is given by:

$$G(s) = \frac{V_{COMP}(s)}{I_{OUT}(s)} \quad [26]$$

The feedback circuit is shown in the following figure:



## Feedback circuit based on operational amplifiers

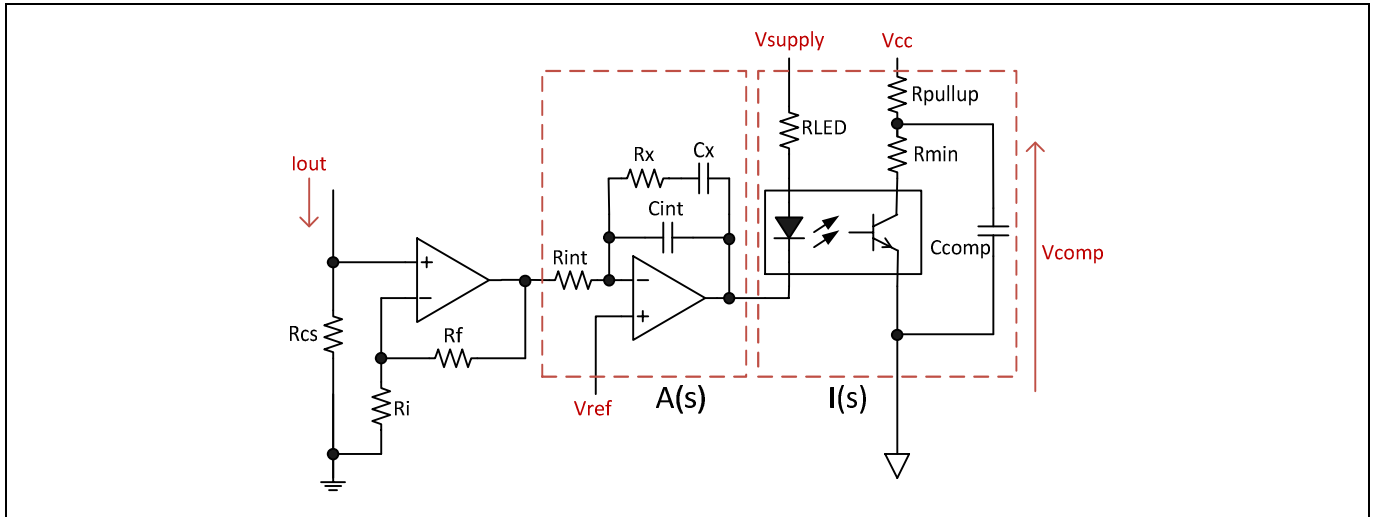


Figure 12 Feedback circuit for current regulation

The transfer function takes the form:

$$G(s) = R_{CS} \cdot \left(1 + \frac{R_f}{R_i}\right) \cdot A(s) \cdot I(s) \quad [27]$$

Where  $A(s)$  is the transfer function of the error amplifier and  $I(s)$  is the transfer function for the opto-isolator and COMP input network.

$$A(s) = \frac{\left(R_X + \frac{1}{s \cdot C_X}\right)}{\left(s \cdot R_X \cdot C_X + \frac{C_{INT}}{C_X} + 1\right)} \quad [28]$$

And

$$I(s) = \frac{CTR \cdot s \cdot R_{PULLUP} \cdot C_{COMP}}{R_{LED} \cdot (R_{PULLUP} + s \cdot C_{COMP})} \quad [29]$$

In this case since the transfer function  $G(s)$  is an impedance, that is a voltage derived from a current, it is necessary to modify the plant transfer function to produce a current at the output as well. Assuming the load consists of a string of LEDs, an approximation of the small signal change in current can be estimated based on the voltage and internal series resistance of the LED load (referred to as  $R_{loadLED}$  distinct from the total load  $R_{load} = V_{out}/I_{out}$ ). This internal resistance varies depending on the LED current rating as well as temperature. It can be measured by measuring LED voltage at two different currents around the operating point, for example at maximum rated current and 90% of rated current, then dividing the difference in voltage by the difference in current. If the resistance is not known and for the purposes of this analysis an approximation is made of 10% of the total LED voltage divided by the rated current.

10 Operational amplifier example schematic

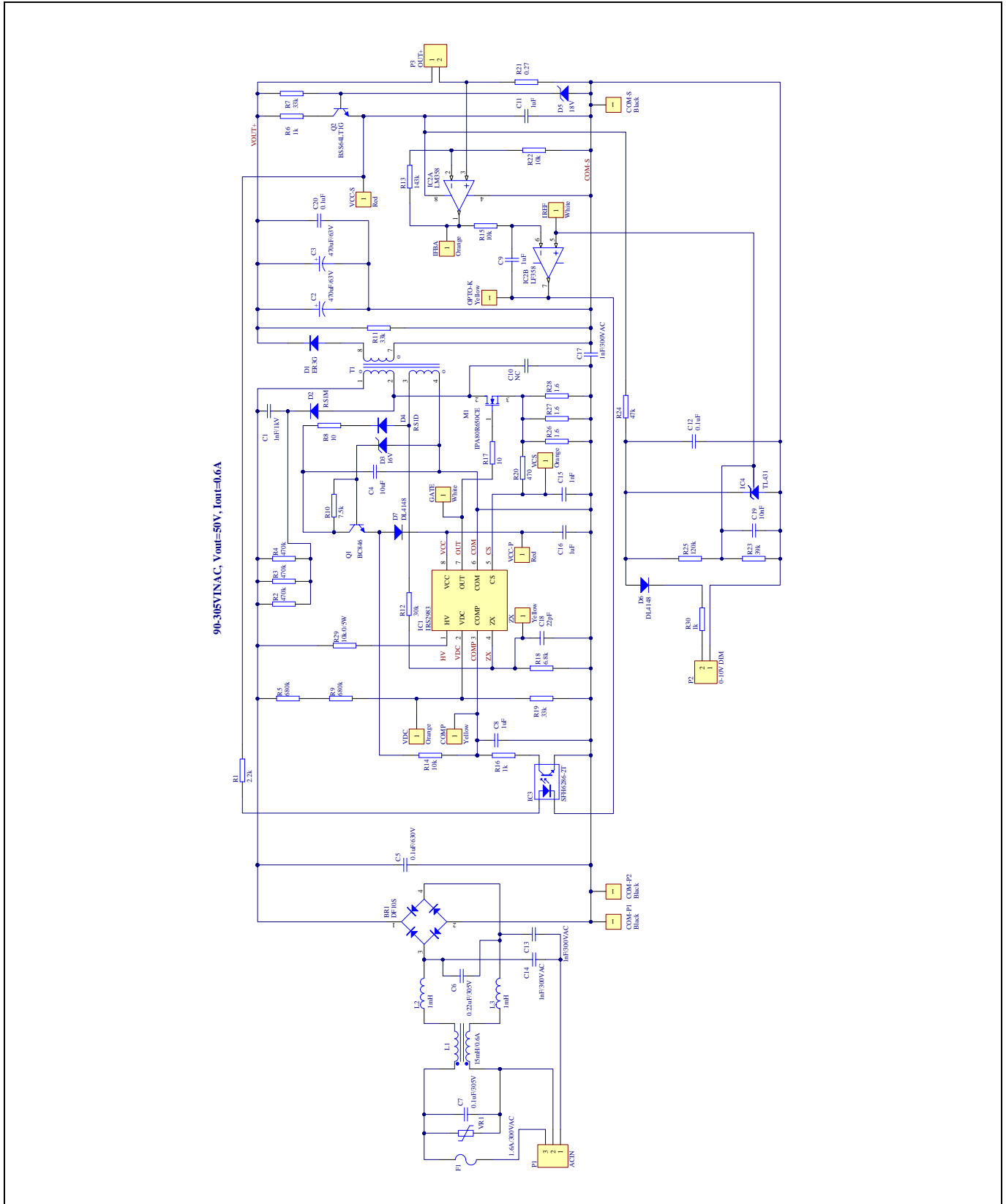


Figure 12 PFC Flyback with opto-isolator and operational amplifier CC feedback example schematic

The following analysis shows that in this case the feedback circuit gain rolls off at a low frequency:

$$V_{\text{comp\_min}} := 1.4$$

$$V_{\text{supply}} := 15 \quad \text{Secondary supply rail for op-amps and opto isolator}$$

$$V_{\text{cc}} := 15 \quad \text{Primary VCC supply rail} \quad \eta := 0.9 \quad \text{Efficiency}$$

$$V_{\text{diode}} := 1 \quad \text{Opto-diode forward voltage drop}$$

$$\text{CTR} := 100 \cdot 10^{-2} \quad \text{Opto-isolator current transfer ratio (expressed as a percentage } \times 10^{-2}\text{)}$$

$$R_{\text{led}} := 2.2 \cdot 10^3$$

$$R_{\text{int}} := 10 \cdot 10^3$$

$$R_{\text{pullup}} := 10 \cdot 10^3$$

$$R_{\text{setmin}} := 1 \cdot 10^3$$

$$C_{\text{int}} := 1 \cdot 10^{-6}$$

$$C_{\text{comp}} := 1 \cdot 10^{-6}$$

$$R_{\text{x}} := 0 \cdot 10^3$$

TL431 series RC feedback

(Connected from COMP to GND)

$$C_{\text{x}} := 0 \cdot 10^{-6}$$

### Calculate feedback circuit transfer function:

$$G(s) = V_{\text{comp}}(s) / I_{\text{out}}(s) \quad \text{(General form of plant transfer function)}$$

### Compensator transfer function:

$$I(s) := \frac{\text{CTR} \cdot R_{\text{pullup}}}{R_{\text{led}} \cdot (1 + s \cdot R_{\text{pullup}} \cdot C_{\text{comp}})}$$

$$Z_i(s) := R_{\text{int}}$$

$$Z_f(s) := \begin{cases} \frac{1}{s \cdot C_{\text{int}}} & \text{if } C_{\text{x}} = 0 \\ \left( R_{\text{x}} + \frac{1}{s \cdot C_{\text{x}}} \right) \cdot \left( \frac{1}{s \cdot C_{\text{int}}} \right) & \text{otherwise} \\ \left( R_{\text{x}} + \frac{1}{s \cdot C_{\text{x}}} + \frac{1}{s \cdot C_{\text{int}}} \right) & \end{cases}$$

$$A(s) := -\frac{Z_f(s)}{Z_i(s)}$$

$$G(s) := R_{\text{cs}} \cdot \left( 1 + \frac{R_{\text{f}}}{R_{\text{i}}} \right) \cdot A(s) \cdot I(s)$$

$R_{\text{x}}$  and  $C_{\text{x}}$  are not essential and may be omitted as in the full schematic.

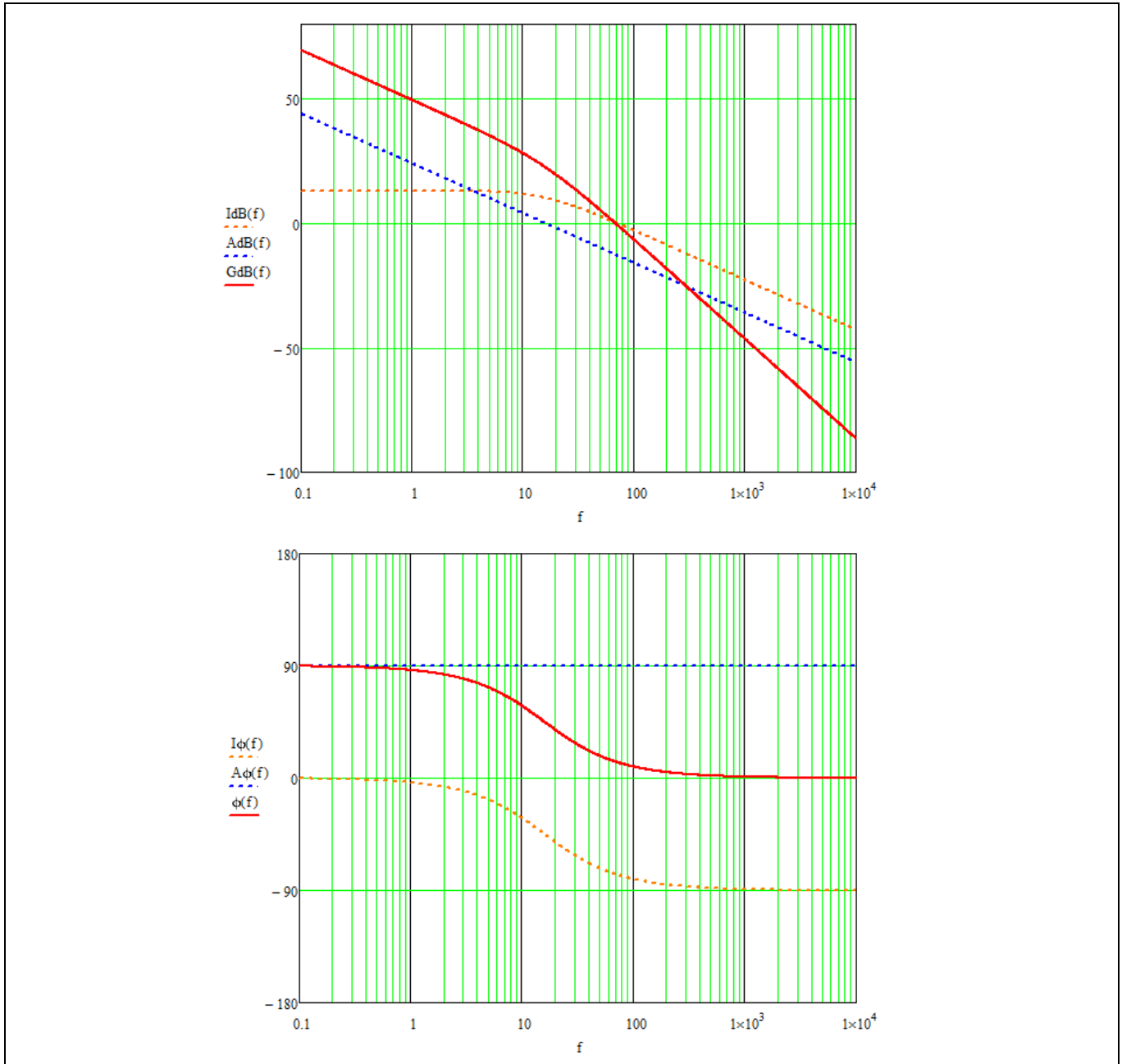


Figure 13 Feedback circuit Bode plots (Gain and Phase)

The determination of the DC gain term of the plant transfer function is similar to the previous example except that it now takes the form:

$$F(s) = \frac{I_{OUT}(s)}{V_{COMP}(s)} \tag{30}$$

Therefore the internal resistance of the LED load needs to be included as follows:

**Control to output (plant) transfer function DC gain at the operating point:**

$$F_o := \delta D_{\delta V_{cmp}} \cdot \frac{V_{ac\_low}}{\sqrt{k}} \cdot \frac{1}{R_{loadLED}} = 3.712$$

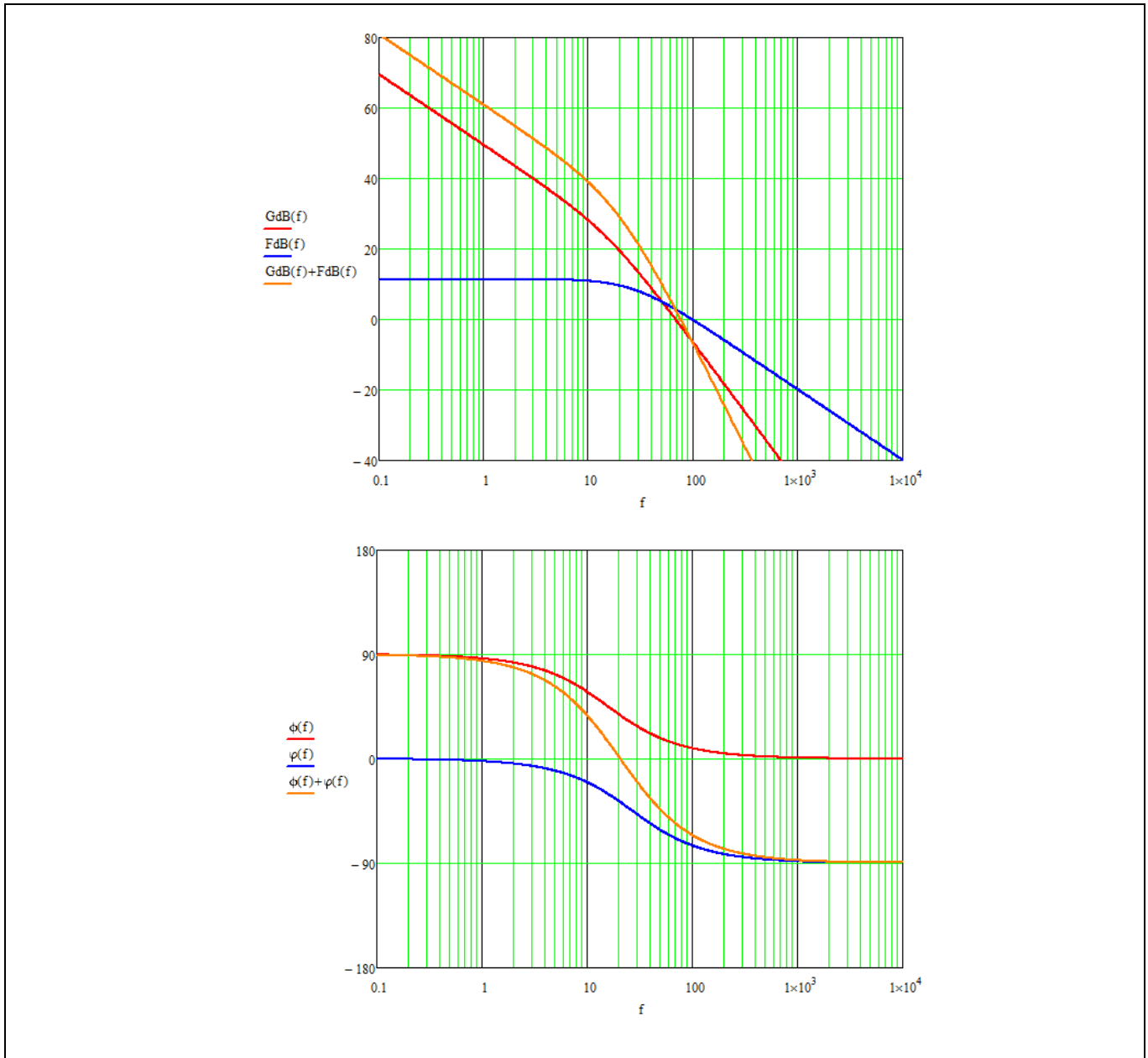


Figure 14 Closed loop transfer function Bode plots (Gain and Phase)

Extrapolate crossover frequency and calculate phase margin:

$$f_c := 20$$

Given

$$F_{dB}(f_c) + G_{dB}(f_c) = 0$$

$$f_{c_{minerr}} := \text{Minerr}(f_c) = 76.191$$

$$PM := 180 + (\varphi(f_c) + \phi(f_c)) = 121.431$$

In this example the phase margin is large, which would result in very stable and under-damped system. Such a system response should be acceptable for an LED lighting application.

## 11 PCB Layout guidelines for system optimization and EMI reduction

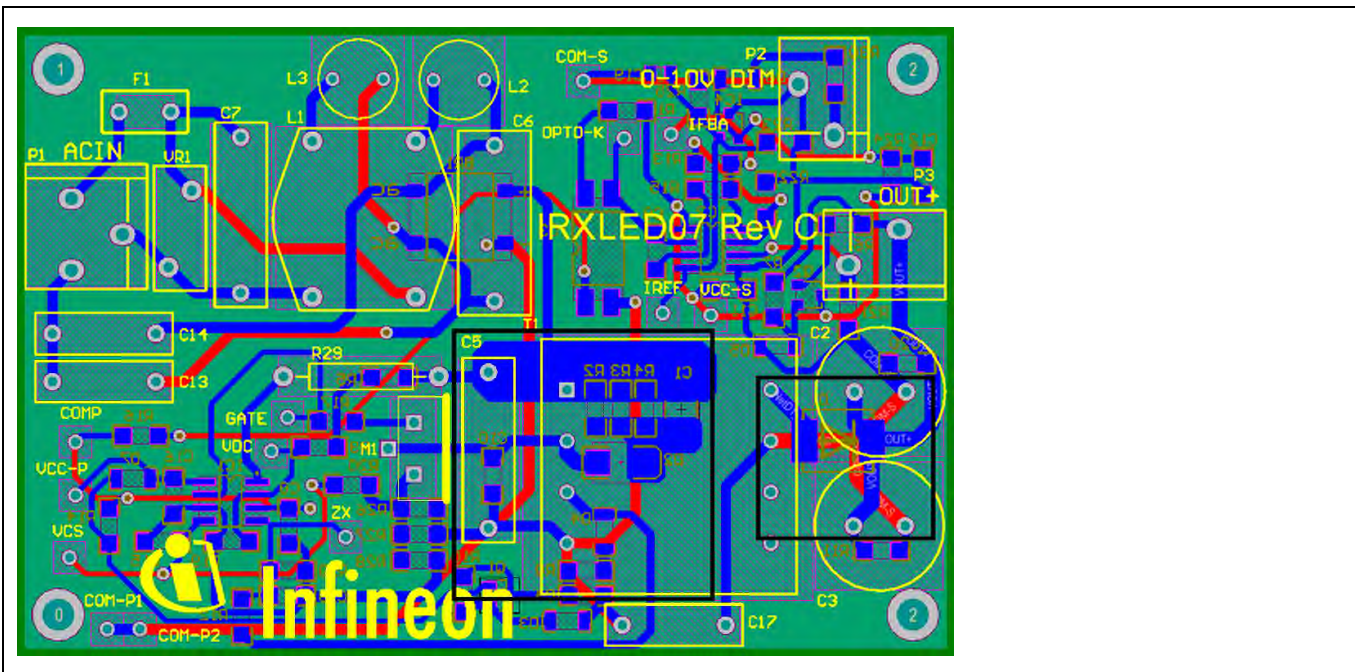


Figure 13 IRS2982S flyback converter PCB layout

The above figure shows the previously described IRS2982S based PFC flyback converter PCB layout. To the left the primary and secondary high frequency current loops are shown, surrounded by a black outline in each case. The primary loop on the left side of the board originates from CDC (C5) connecting first to the transformer (T1) primary (pin 1). The other side of the primary winding (pin 2) is connected to the drain of the MOSFET MFB (M1). To minimize EMI this trace should be kept as short as possible. The current sense resistors (R26-28) are located such that the connection to the high frequency 0V bus return of CDC is extremely short with the other end connected to the source of MFB through another short trace.

The secondary high frequency current loop originates from T1 pin 7 connecting through a short trace to DOUT (D1), which then connects through another very short trace to COUT (C2). The negative side of COUT returns directly back to T1 pin 8 again through another short trace providing the tightest possible HF current loop. Parallel output capacitors C2 and C3 are connected through heavy copper traces to provide minimum impedance and best possible HF ripple current sharing between the capacitors. The primary-secondary 0V Y capacitor CY3 (C17) is connected directly to each 0V HF point with the shortest possible traces. The layout techniques described must be used otherwise the converter will be unable to meet conducted EMI limits!

Aside from EMI considerations, it is essential to design the PCB so that the IRS2982S is able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. The picture on the right of the above figure shows the area around IC1. Pin 6 is the 0V (ground) connection, which is returned to the 0V side of CDC through a direct connection. It is also essential that decoupling capacitor CVCC1 be located directly next to IC1 with direct connections to the VCC and COM/0V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star point, which is at the negative side of the high frequency capacitor (CDC)

Components associated with the feedback loop IC1 and the feedback loop such as CCF (C15), CZX (C18) CCMP (C8) are connected to the signal ground with the shortest traces possible back to pin 6. Components associated with the feedback loop should also be connected to a common signal ground close to the TL431 anode or



operational amplifier ground pin. Additionally, clearance distances between high voltage traces and other parts of the circuit are kept as large as possible to comply with safety requirements.





Conclusion

## 12 Conclusion

Control loop design can be challenging in PFC Flyback applications when using a TL431 and opto-isolator in the feedback loop due to the minimum gain and the need to maintain effectively constant on time for PFC operation. This requires careful selection of the component values in the feedback loop and compensation network to prevent unstable operation and oscillation. The process of selection of these components is made much simpler and quicker by use of a MathCAD based tool that generates a Bode plot of the converter total loop gain and extrapolates the phase margin. This allows the designer to check for an adequate phase margin under different load conditions based on a specific set of component values thereby providing a means for determining a set of values that will result in stable system, which should greatly reduce lab optimization of the design.

Other important design considerations are also discussed, which avoid the possibility of encountering non-optimum performance in the finished LED driver design. Designers are recommended to read carefully through section 4 when using the IRS2982S with an opto-isolator feedback circuit.

Analysis of a feedback circuit implementation based around operational amplifiers shows that such an arrangement is much less prone to instability than the TL431 based system. Such a feedback circuit also has more freedom to design its frequency response to optimize system performance.

References

- [1] IRS2982SPBF IC datasheet, Infineon Technologies.
- [2] ANEVAL 201602\_PL16\_017, 55 W Flyback converter design using the IRS2982S controller – IRXLED04, Infineon Technologies.

**Attention:**

Revision History

Major changes since the last revision

Page or Reference	Description of change
	First Release

#### Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, Infineon™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Trademarks updated August 2015

#### Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2016-10-10**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2017 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference**

**AppNote Number**

**AN\_201610\_PL16\_001**

#### IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.