Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A

About this document

Scope and purpose

AN99497 explains how to select components and presents PCB layout guidelines for a power management system with S6BP201A, S6BP202A, and S6BP203, which are Cypress's one-channel power management ICs (PMICs).

Associated Part Family

S6BP201A, S6BP202A, S6BP203A

Related Documents

S6BP201A, **S6BP202A**, **S6BP203A** Datasheets

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1 Introduction

S6BP201A, S6BP202A, and S6BP203A are PMICs with a one-channel buck-boost DC/DC converter for automotive applications, as shown in **Figure 1**. These ICs can work in a wide range of input voltages, 2.5 V~42 V, and provide a stable output voltage up to 42 V from a cold crank condition of a car until the load dump condition.

This product has achieved high conversion efficiency in all conditions with a very low quiescent current of less than 20 µA. It has also automatically changed modes between pulse frequency modulation (PFM) and pulse width modulation (PWM) under light load conditions. Furthermore, it can reduce the size of the components via the high switching frequency operation of 2.1 MHz and four embedded switching FETs. This PMIC can also reduce the footprint area and the number of peripheral parts because the compensation circuit and the output setting resistors are built in.

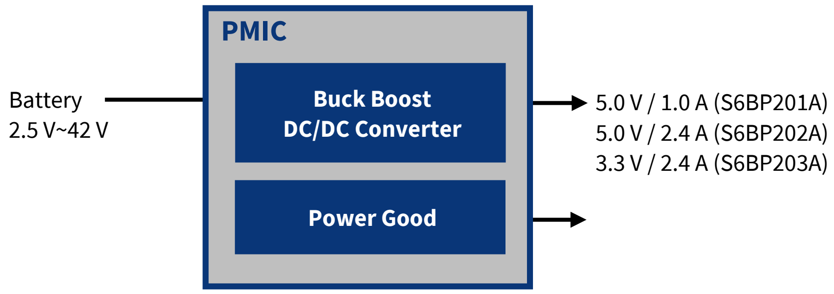

Figure 1 Power management system block diagram

2 Component selection

This section explains how to select components for a power management system with S6BP201A, S6BP202A, or S6BP203.

2.1 DC/DC converter parts selection

Figure 2 shows the DC/DC converter section of an example circuit that uses the S6BP201A, S6BP202A, or S6BP203A power management solution.

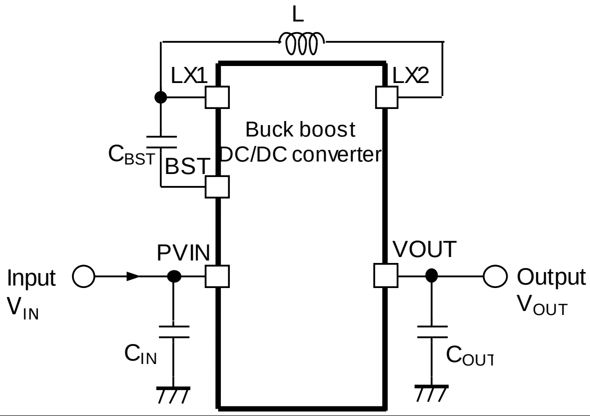

Figure 2 Connection of the DC/DC converter

PVIN, LX1, LX2, VOUT, and BST are the terminal names of the PMIC (refer to the **S6BP201A**, **S6BP202A** and **S6BP203A** datasheets).

2.1.1 Inductor (L)

Generally, the inductance of the coil will be selected along with the value of the E6 series. You do not need to design an inductor for a power management system based on the S6BP201A, S6BP202A, and S6BP203A devices because they are designed to operate efficiently with a 2.2-µH (2.1-MHz operation) or 22-µH (200-kHz operation) external inductor. At the same time, you should calculate the maximum current value to confirm whether the electric current that flows to the inductor is within the rated parameters for the inductor by using **Equation 1**.

Equation 1

$$IL_{MAX} \geq I_{Lpeak}$$

Where:

IL_{MAX}: Rated current of the inductor (A)

I_{Lpeak} : Peak current limit with overcurrent protection (A); S6BP201A: 2.0 A, S6BP202A: 4.8 A, S6BP203A: 4.8 A

2.1.2 Input capacitor (C_{IN})

A ceramic capacitor that has a low equivalent series resistance (ESR), typically less than 10 mΩ and excellent frequency characteristics—that is, the capacitance is not reduced up to the switching frequency—should be used. Generally, the capacitance will be selected along with the value of the E6 series. The recommended value is 10 µF. Calculate the necessary rated voltage of the input capacitor according to **Equation 2**.

Equation 2

$$V_{CIN} > V_{IN}$$

Where:

V_{CIN}: Rated voltage of input capacitor (V)

V_{IN}: Power supply voltage (V)

2.1.3 Output capacitor (C_{OUT})

A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. **Table 1** lists the recommended capacitance values for each switching frequency of the DC/DC converter. When you consider a ceramic capacitor, you should take into account the reduction of capacitance due to the DC bias characteristics of the capacitor itself. Generally, a large capacitor has a stable DC bias characteristic. Calculate the necessary rated voltage of the output capacitor by using **Equation 3**.

Equation 3

$$V_{COUT} > V_{OUT}$$

Where:

V_{COUT}: Rated voltage of output capacitor (V)

V_{OUT}: Output setting voltage (V)

The recommended component values for each switching frequency are shown in **Table 1**.

Table 1 Switching frequency of setting resistor, inductor, input capacitor, and output capacitor

Switching frequency	RT	L	C_{IN}	C_{OUT}
200 kHz	270 kΩ	22 µH	10 µF	22 µF x 8 pcs
330 kHz	160 kΩ	15 µH	10 µF	22 µF x 8 pcs
500 kHz	110 kΩ	10 µH	10 µF	22 µF x 8 pcs
1 MHz	51 kΩ	4.7 µH	10 µF	22 µF x 4 pcs
2.1 MHz	22 kΩ	2.2 µH	10 µF	22 µF x 2 pcs

2.1.4 Bootstrap capacitor (C_{BST})

To drive the gate of the high-side FET, the bootstrap capacitor must have enough stored charge. The recommended component value is 0.1 µF. Calculate the required rated voltage of the bootstrap capacitor by using **Equation 4**.

Equation 4

$$V_{CBST} > V_{VCC}$$

Where:

V_{CBST}: Rated voltage of bootstrap capacitor (V)

V_{VCC}: Voltage of VCC terminal (V)

2.2 Common parts selection

2.2.1 VIN bypass capacitor (C_{VIN}), VCC bypass capacitor (C_{VCC})

VIN and VCC are PMIC's terminals (refer to the **S6BP201A**, **S6BP202A**, and **S6BP203A** datasheets) that need a bypass capacitor. A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. **Table 2** gives the recommended values for these capacitors.

Table 2 Bypass capacitor

VIN	VCC
0.1 µF	4.7 µF

Calculate the necessary rated voltage of the capacitor by using **Equation 5**.

Equation 5

$$V_{CVIN} > V_{IN} \, , \, V_{CVCC} > V_{VCC}$$

Where:

V_{CVIN}: Rated voltage of VIN bypass capacitor (V)

V_{IN}: Power supply voltage (V)

V_{CVCC}: Rated voltage of VCC bypass capacitor (V)

V_{VCC}: Voltage of VCC terminal (V)

2.2.2 Power good (PG) pull-up resistor

PG terminals of the PMIC need a pull-up resister if the design uses the power good monitor function (refer to the **S6BP201A**, **S6BP202A**, and **S6BP203A** datasheets).Considering that the leakage current of each terminal is less than 1 µA, this IC must have a driving ability of 1 mA. The resistance should be selected in the range of 10 kΩ to 300 kΩ when the resistor is pulled up by 5 V.

2.2.3 Output voltage regenerative circuit (only for S6BP203A)

Figure 3 shows a regenerative circuit example. You need to select the components shown in **Figure 3**.

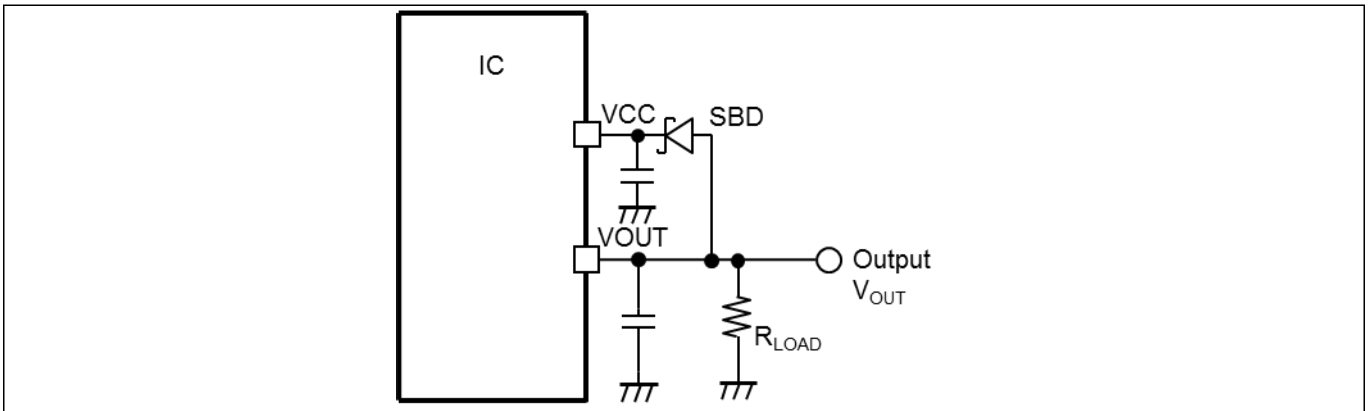

Figure 3 Connection of regenerative circuit

VCC and VOUT are the terminals name of the PMIC (refer to the **S6BP203A** datasheet).

Add the regenerative circuit according to the flow chart in **Figure 4**.

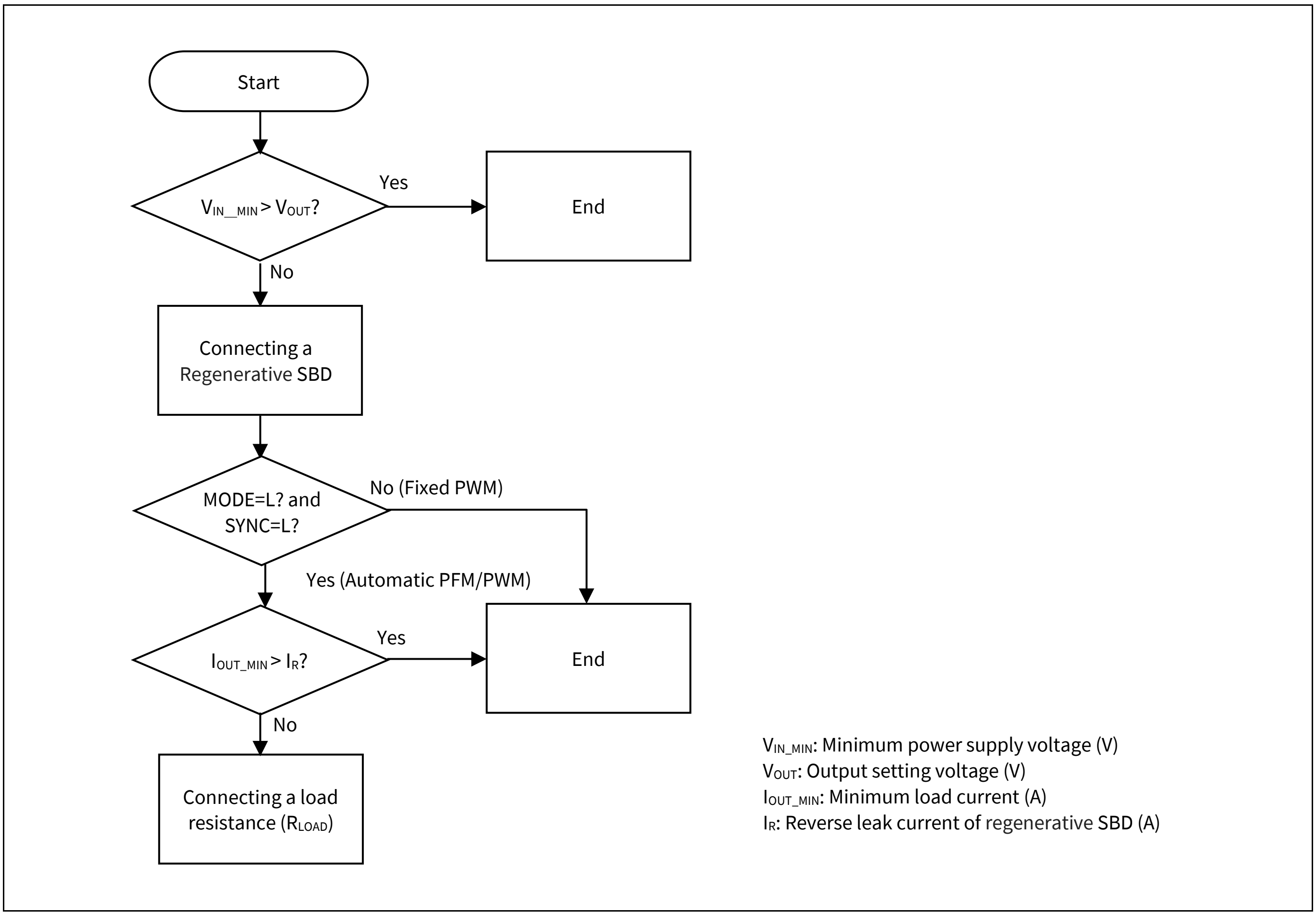

Figure 4 **Regenerative circuit selection flow chart**

The reverse leak current of the regenerative Schottky barrier diode (SBD) is for supplying V_{OUT} to the VCC terminal, and the rated current is sufficient at 100 mA. The rated voltage must be at VCC voltage and V_{OUT} or more.

Use **Equation 6** to calculate the required load resistance.

Equation 6

$$R_{LOAD} < \frac{V_{OUT}}{I_R}$$

Where:

R_{LOAD}: Load resistance of output (Ω)

V_{OUT}: Output setting voltage (V)

I_R: Reverse leak current of regenerative SBD (A)

A characteristic of the SBD is that the leakage current increases at high temperatures. Selecting the small leakage SBD permits increasing or eliminating the load resistance.

3 PCB layout guidelines

This section explains how to design the PCB for a power management system with S6BP201A, S6BP202A, or S6BP203A. **Figure 5** shows an example layout of the power management system.

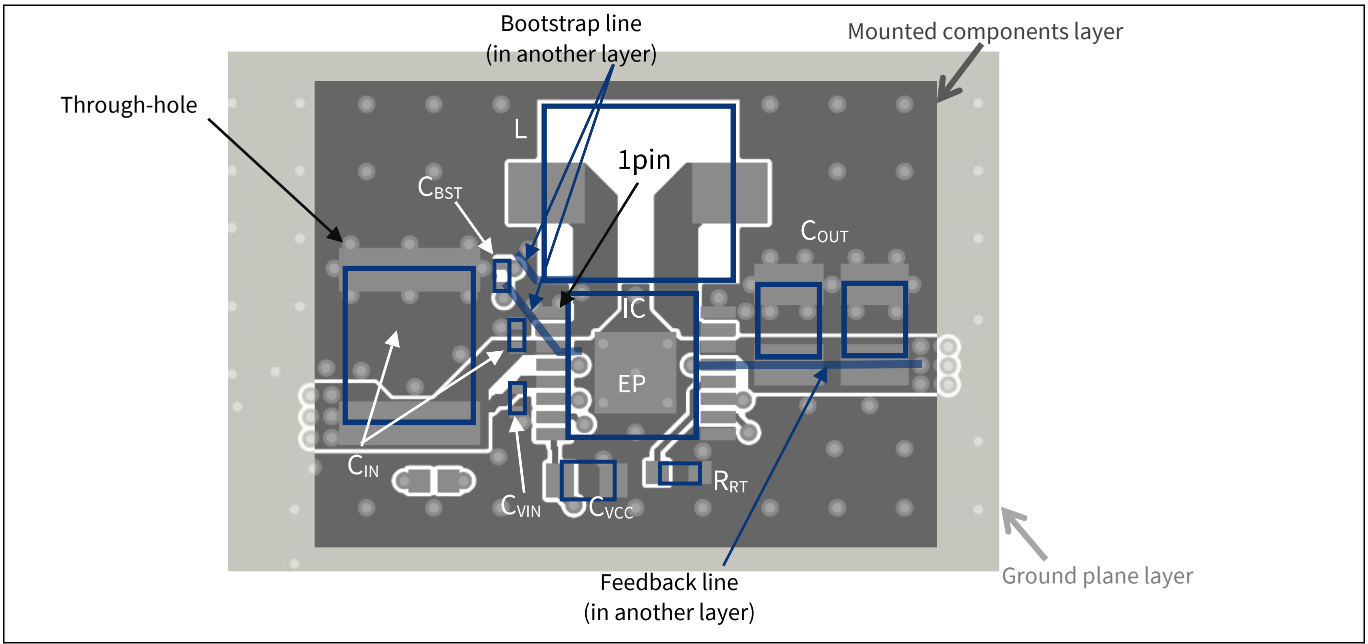

Figure 5 Layout example

The switching components, consisting of an input capacitor (C_{IN}), IC, coil (L), and output capacitor (C_{OUT}), are placed close to one another. These components should be connected with a wide and short plane. In particular, two current loops—the first from the input capacitor (C_{IN}) to the PMIC (PVIN and PGND1 terminal) and the second from the output capacitor (C_{OUT}) to the PMIC (VOUT and PGND2 terminal)—should be carefully chosen to decrease the total current loop. The ground terminal of the switching component should be connected to this ground plane by through-holes that are put near the ground terminal of the switching component.

The feedback line from the PMIC's FB terminal should be connected individually to the terminal of the output capacitor (C_{OUT}). This wiring is sensitive. It should be away from the pattern of the LX1 and LX2 terminal and the switching components.

The VIN and VCC bypass capacitors (C_{VIN}, C_{VCC}) should be placed close to the PMIC's VIN and VCC terminals. The VIN switching frequency setting resistor (R_{RT}) should be placed close to the PMIC's RT terminal. These resistors and capacitors should be connected with a short line. The ground terminals of the components and PMIC should be connected to the ground plane of another layer by through-holes that are placed near each ground terminal of these components and the PMIC.

There is a leakage flux near a coil or the backside of the PCB mounted coil. Sensitive wiring and components should be located away from the coil or the back of the PCB mounted coil.

If the DC/DC operation mode is fixed PWM mode, the PMIC's MODE terminal should be connected to the output capacitor (C_{OUT}) by another line different from the line to the PMIC's FB terminal.

The PMIC's exposed pad (EP) should be connected to the ground plane that will be placed on the IC mounting surface. The EP should be connected to the ground plane of another layer for heat dissipation and stable operation purposes.

Refer to the datasheets (**S6BP201A**, **S6BP202A**, and **S6BP203A**) to learn more about each terminal of the PMIC.

Revision history

Document version	Date of release	Description of changes
**	2015-12-04	New application note.
*A	2016-03-15	Updated Document Title to read as “AN99497 - Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A”. Added “PCB layout guidelines”.
*B	2017-08-31	Updated Cypress Logo and Copyright.
*C	2018-10-10	Updated to new template. Completing Sunset Review.
*D	2021-06-10	Updated to Infineon template.

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