



THIS SPEC IS OBSOLETE

Spec No: 001-99494

Spec Title: AN99494 - MIGRATING FROM S25FL204K TO  
S25FL208K

Replaced by: NONE

## Migrating from S25FL204K to S25FL208K

**Author:** Arthur Claus

**Associated Part Family:** S25FL204K S25FL208K

**Associated Code Examples:** None

**Related Application Notes:** None

AN99494 discusses the key differences that need to be considered when migrating from S25FL204K to S25FL208K. This application note explains how S25FL208K is a replacement for S25FL204K.

### 1 Introduction

S25FL208K, an 8-Mbit SPI Flash, is a replacement device for S25FL204K. The two devices are identical in terms of pinout, package composition and dimensions, and command set. This application note discusses the key differences between the two devices that need to be considered when migrating from the S25FL204K to the S25FL208K.

### 2 Drop-In Replacement or Not?

From a hardware point of view, the S25FL204K operates at clock speeds up to 85MHz and the S25FL208K is only able to operate up to 76MHz. From a software point of view, the command sets are identical; the device ID, Block protection features, and Chip Erase times are different. Thus, in many cases, a S25FL208K is a drop-in replacement for a S25FL204K. See [Critical Considerations](#) for more details.

Table 1 shows the compatibility chart of S25FL204K and S25FL208K. For a detailed comparison, see [Table 3](#).

Table 1. Compatibility Chart

S25FL204K Feature or Spec	Is S25FL208K Compatible?
Package	Yes
Pinout	Yes
Temperature Range	Yes
Operating Voltage	Yes
Operating Current	Yes
Standby Current	Yes
Command Set	Yes
Timing / Frequency	No
Data Retention	Yes
Endurance	Yes
Block Protection	No

### 3 Ordering Part Numbers

Table 2. Recommended Ordering Part Numbers for Migration

S25FL204K	S25FL208K	Comments
Ordering Part Number	Ordering Part Number	
S255FL204K0TMFI01	S25FL208K0RMFI01	Clocks above 76 MHz not supported. Software change required for Device ID update and Block protection.
S255FL204K0TMFI04	S25FL208K0RMFI04	

### 4 Comparison of S25FL204K and S25FL208K

Table 3. Detailed Comparison Table

		S25FL204K	S25FL208K	Comments
<b>Package Type</b>		01, 04	01, 04	Identical RoHS-compliant packages.
<b>Pinout/package Outline</b>		SOIC-8 (208 mil),SOIC-8 (150 mil)	SOIC-8 (208 mil),SOIC-8 (150 mil)	Identical pinout, outline, and board footprint.
<b>Temperature Range</b>		-40 °C to +85 °C	-40 °C to +85 °C	Identical
<b>Operating Voltage Range</b>		2.7 V to 3.6 V	2.7 V to 3.6 V	Identical
<b>Read Data Current<sup>1 2</sup></b>	<b>Typical</b>	10 mA @ 33 MHz	10 mA @ 33 MHz	Identical
	<b>Max</b>	15 mA @ 33 MHz	15 mA @ 33 MHz	
	<b>Max</b>	25 mA @ 100 MHz	25 mA @ 100 MHz	
<b>Dual Output Read Current<sup>1 2</sup></b>	<b>Typical</b>	12 mA @ 33 MHz	12 mA @ 33 MHz	Identical
	<b>Max</b>	18 mA @ 33 MHz	18 mA @ 33 MHz	
	<b>Max</b>	25 mA @ 100 MHz	25 mA @ 100 MHz	
<b>Page Program Current<sup>3</sup></b>	<b>Typical</b>	15 mA	15 mA	Identical
	<b>Max</b>	20 mA	20mA	
<b>Write Status Register Current<sup>3</sup></b>	<b>Typical</b>	10 mA	10 mA	Identical
	<b>Max</b>	18 mA	18 mA	
<b>Erase Current<sup>3</sup></b>	<b>Typical</b>	20 mA	20 mA	Identical
	<b>Max</b>	25 mA	25 mA	
<b>Standby Current<sup>4</sup></b>	<b>Typical</b>	15 µA	15 µA	Identical
	<b>Max</b>	35 µA	35 µA	
<b>Power-Down Current<sup>4</sup></b>	<b>Typical</b>	15 µA	15 µA	Identical
	<b>Max</b>	32 µA	32 µA	
<b>Command Set</b>		3-byte addressing, opcodes	3-byte addressing, opcodes	Identical

<sup>1</sup>SCK = 0.1 VCC / 0.9 VCC DO= Open

<sup>2</sup>Checker Board Pattern

<sup>3</sup> CS# = VCC

<sup>4</sup> CS# = VCC, VIN = GND or VCC

		S25FL204K	S25FL208K	Comments
<b>Clock Frequency</b>		85 MHz	76 MHz	Different. See the Clock Speed section in <a href="#">Critical Considerations</a> .
<b>Data Retention</b>		20-year data retention typical	20-year data retention typical	Identical
<b>Endurance (Program/Erase Cycles)</b>		100k erase/program cycles typical	100k erase/program cycles typical	Identical
<b>VCC (min) to CS# Low (t<sub>VSL</sub>)</b>		10 $\mu$ s Min	10 $\mu$ s Min	Identical
<b>Time Delay Before Write Instruction (t<sub>PW</sub>)</b>	Typical	1 ms	1 ms	Identical
	Max	10 ms	10 ms	
<b>Write Inhibit Threshold Voltage (V<sub>WI</sub>)</b>	Typical	1 V	1 V	Identical
	Max	2 V	2 V	
<b>Device ID</b>	ABh	12h	13h	Different. See the Device ID section in <a href="#">Critical Considerations</a> .
	90h	0112h	0113h	
	95h	014013h	014014h	
<b>Write Status Register Time</b>	Typical	10 ms	10 ms	Identical
	Max	15 ms	15 ms	
<b>Byte Program Time (First Byte)</b>	Typical	30 $\mu$ s	30 $\mu$ s	Identical
	Max	50 $\mu$ s	50 $\mu$ s	
<b>Additional Byte Program Time (After First Byte)</b>	Typical	6 $\mu$ s	6 $\mu$ s	Identical
	Max	12 $\mu$ s	12 $\mu$ s	
<b>Page Program Time</b>	Typical	1.5 ms	1.5ms	Identical
	Max	5 ms	5 ms	
<b>Sector Erase Time (4 kB)</b>	Typical	50 ms	50 ms	Identical
	Max	300 ms	300 ms	
<b>Block Erase Time (64 kB)</b>	Typical	0.5 s	0.5 s	Identical
	Max <sup>5</sup>	2 s	2 s	
<b>Chip Erase Time</b>	Typical	3.5 s	7 s	Different. See the Device Density section in <a href="#">Critical Considerations</a> .
	Max	7 s <sup>6</sup>	15 s <sup>7</sup>	
<b>Block Protection</b>		See <a href="#">Table 5</a>	See <a href="#">Table 5</a>	Different. See the Device Density section in <a href="#">Critical Considerations</a> .
<b>Number of Blocks (64K) / Sectors (4K)</b>		8/128	16/256	Different. See the Device Density section in <a href="#">Critical Considerations</a> .
<b>Flash Array Size</b>		524,288 bytes	1,048,576 bytes	Different. See the Device Density section in <a href="#">Critical Considerations</a> .

<sup>5</sup>Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 5.3 s

<sup>6</sup> Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 8.4 s

<sup>7</sup> Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 18 s.

## 5 Critical Considerations

You should consider all the parameter differences mentioned in [Table 3](#) during the migration to S25FL208K. This section discusses the critical differences. System designers should also review the datasheet when migrating to the new part.

### 5.1 Clock Speed

The S25FL204K operates at a maximum clock rate of 85 MHz. The S25FL208K operates at a maximum clock rate of 76 MHz. If the system being migrated operates at more than 76 MHz, the clock rate will need to be reduced so that it is 76 MHz or less. If it is not possible to change the clock rate, contact Cypress for other migration options.

### 5.2 Device ID

[Table 4](#) lists the opcodes that could be used to retrieve the device ID from the flash device and their values. Software that checks the device ID of the S25FL204K will need to be changed to recognize the device ID returned by the S25FL208K.

Table 4. Device ID Values

Opcode	S25FL204K Value	S25FL208K Value
ABh	12h	13h
90H	0112h	0113h
9FH	014013h	014014h

### 5.3 Device Density

The fact that the S25FL208K has a higher density than the S25FL204K raises several issues that must be accounted for. The sections below detail these issues.

#### 5.3.1 Chip Erase

Because the S25FL208K has a flash array that is twice as large as the S25FL204K, the time required to execute the Chip Erase (C7h) opcode will be twice as long. Any software that uses time delays instead of checking the Write In Progress (WIP) bit in the status register will need to be modified to account for the longer chip erase time.

#### 5.3.2 Block Protection

The S25FL208K has twice as many blocks (64K) and sectors (4K) as the S25FL204K. The behavior of the Block Protection bits in the Status register is different. [Table 5](#) summarizes the differences.

Table 5. Block Protection Details

Status Register Bit				S25FL204K	S25FL208K
BP3	BP2	BP1	BP0		
0	0	0	0	None	None
0	0	0	1	Block 7 (070000h - 07FFFFh)	Block 15 (0F0000h-0FFFFFFh)
0	0	1	0	Blocks 6-7 (060000h-07FFFFh)	Blocks 14-15 (0E0000h-0FFFFFFh)
0	0	1	1	Blocks 4-7 (040000-07FFFFh)	Blocks 12-15 (0C0000h-0FFFFFFh)
0	1	0	0	Blocks 0-7 (000000h-07FFFFh)	Blocks 8-15 (080000h-0FFFFFFh)
0	1	0	1	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFFh)
0	1	1	0	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFFh)
0	1	1	1	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFFh)
1	0	0	0	None	None
1	0	0	1	Sectors 0-126 (000000h-07EFFFh)	Sectors 0-254 (000000h-0FEFFFh)
1	0	1	0	Sectors 0-123 (000000h-07BFFFh)	Sectors 0-252 (000000h-0FCFFFh)

Status Register Bit				S25FL204K	S25FL208K
BP3	BP2	BP1	BP0		
1	0	1	1	Sectors 0-119 (000000h-076FFFh)	Sectors 0-247 (000000h-0F6FFFh)
1	1	0	0	Sectors 0-111 (000000h-06FFFFh)	Sectors 0-239 (000000h-0EFFFh)
1	1	0	1	Sectors 0-95 (000000h-005FFFFh)	Sectors 0-223 (000000h-0DFFFFh)
1	1	1	0	Sectors 0-63 (000000h-03FFFFh)	Sectors 0-191 (000000h-0BFFFFh)
1	1	1	1	Sectors 0-127 (000000h-07FFFFh)	Sectors 0-255 (000000-0FFFFh)

### 5.3.3 Addressable Flash Array

The flash array in the S25FL208K is twice as large as the one in the S25FL204K so it requires one extra address bit to address it (A19). Migrated software must control address bit A19. If A19 is not constant (either 0 or 1), it is possible that data will not be where it is expected to be.

## 6 Summary

AN99494 discussed the differences between S25FL204K and S25FL208K that need to be considered during migration to the S25FL208K.

## 7 Related Documents

[S25FL204K Datasheet](#)

[S25FL208K Datasheet](#)

## Document History

Document Title: AN99494 - Migrating from S25FL204K to S25FL208K

Document Number: 001-99494

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4898638	AHCL	08/27/2015	New application note.
*A	5866782	AESATMP8	08/29/2017	Updated logo and Copyright.
*B	6351987	BWHA	10/16/2018	Obsolete document. Completing Sunset Review.

## Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

### Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

All other trademarks or registered trademarks referenced herein are the property of their respective owners.



Cypress Semiconductor  
198 Champion Court  
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2015-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.