Designing a Power Management System with S6BP501A and S6BP502A

About this document

Scope and purpose

AN99435 explains how to select the components and presents PCB layout guidelines for a power management system with S6BP501A or S6BP502A, which are Cypress' three-channel power management ICs (PMICs).

Associated Part Family

S6BP501A, **S6BP502A**

Related Documents

S6BP501A, **S6BP502A** Datasheet

Table of contents

1 Introduction

S6BP501A and S6BP502A are PMICs for automotive clusters optimized with Cypress's Traveo™ MCU family, as listed in **Table 1**. These PMICs have a three-channel output: one high-voltage step-down DC/DC controller (DD3V), one step-down DC/DC converter with built-in switching FETs (DD1V), and one step-up DC/DC converter with built-in switching FETs (DD5V), as shown in **Figure 1**. Each output voltage can be set by an external resistor. DD1V and DD5V can operate at a high switching frequency of 2.1 MHz; therefore, reducing the footprint area by miniaturizing components is possible.

You should keep certain considerations in mind when you design a power supply system with S6BP501A or S6BP502A. This application note describes the component selection process and PCB layout guidelines in the power supply design using S6BP501A or S6BP502A.

Table 1 PMICs

Part Number	Output Voltage (V) / Maximum Supply Current (A)		
	DD3V	DD5V	DD1V
S6BP501A	3.2 V~3.4 V / 1.6 A	5.0 V~5.2 V / 1.3 A	1.0 V~1.3 V (1.15 V recommended) / 1.4 A
S6BP502A	3.2 V~3.4 V / 1.9 A	5.0 V~5.2 V / 1.3 A	1.0 V~1.3 V (1.20 V recommended) / 2 A

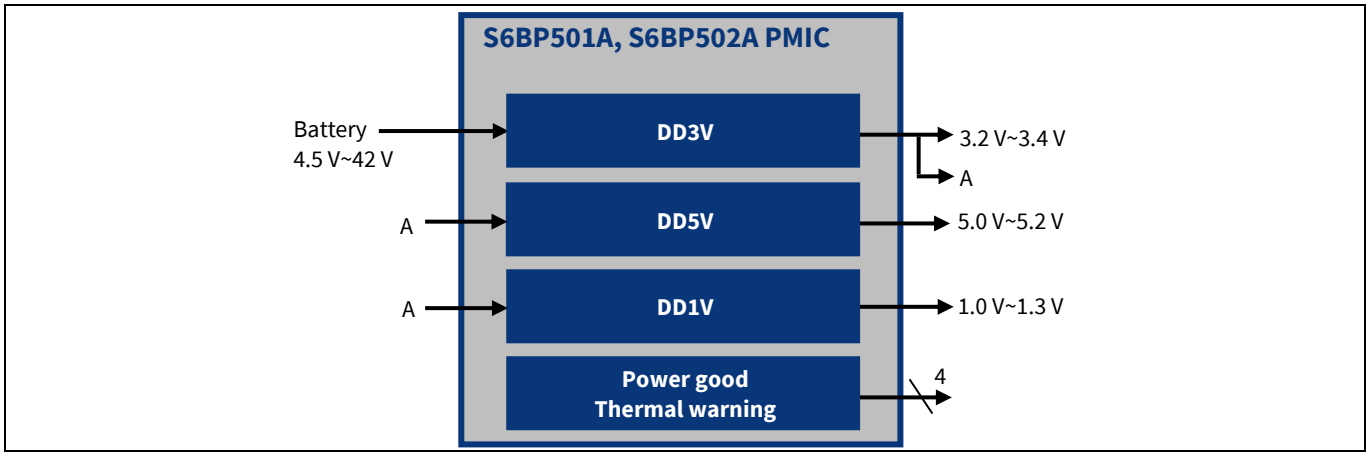

Figure 1 Power management system block diagram

Power good and thermal warning are the function names of the PMIC (refer to the **datasheet**).

2 Component selection

This section explains how to select the components for a power management system with S6BP501A or S6BP502A.

2.1 DC/DC converter (DD1V)

Figure 2 depicts the DD1V DC/DC converter section in the S6BP501A/S6BP502A application example. PVCC1V, LX1, FB1V, and PGND1V are the terminal names of the PMIC (refer to the **datasheet**). This section explains how to choose each component shown in **Figure 2**.

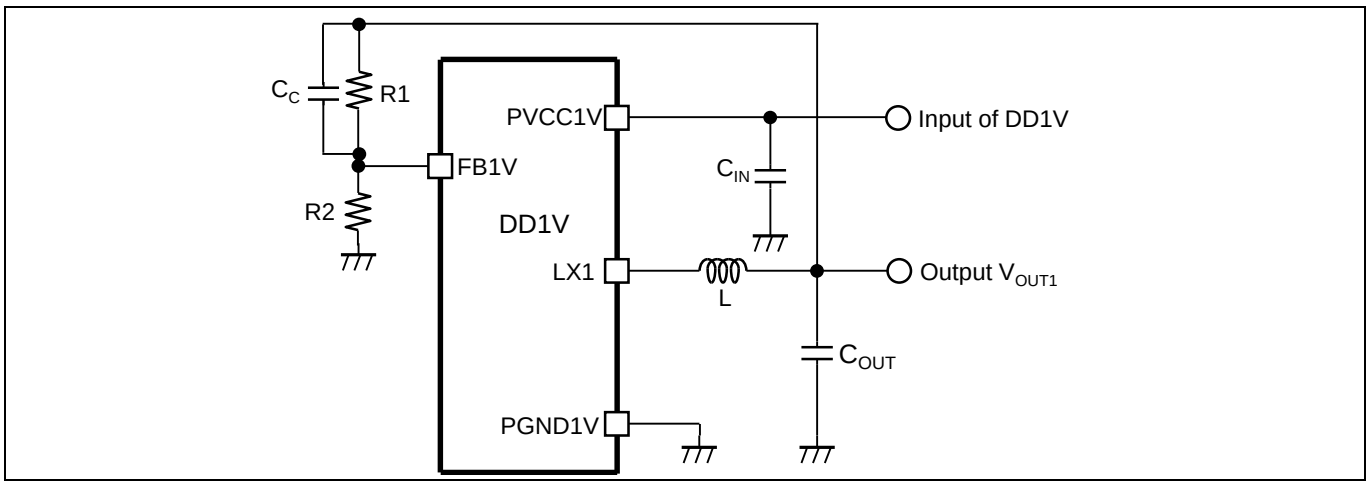

Figure 2 Connection of DD1V

2.1.1 Output setting resistors (R1, R2) and phase compensation capacitor (C_C)

A pair of voltage-dividing resistors (R1 and R2) configures the output voltage (V_{OUT1}) according to **Equation 1**. Refer to the DD1V output voltage setting range in the datasheet for the range of V_{OUT1}. Choose approximately 270 kΩ for R1 so that the built-in phase compensation network works well. The recommended resistor values are listed in **Table 2**.

Equation 1

$$V_{OUT1} = V_{FB1V} \times \frac{R1 + R2}{R2}$$

Where:

R1, R2: Output voltage setting resistance (Ω)

V_{FB1V}: DD1V FB voltage = 0.6 (V)

V_{OUT1}: DD1V output setting voltage (V)

Table 2 DD1V output voltage setting resistor

Part No	DD1V setting voltage	R1	R2	C_C
S6BP501A	1.15 V	274 kΩ	301 kΩ	12 pF
S6BP502A	1.20 V	270 kΩ	270 kΩ	

2.1.2 Inductor (L)

Generally, the inductance of the inductor should be selected from among values of the E6 series of preferred numbers[1]. The recommended inductor value for S6BP501A/S6BP502A is 1.5-µH. Also, you should calculate the maximum current value using **Equation 2** to confirm whether the electric current that flows through the inductor is within the rated parameters for the inductor.

Equation 2

$$IL_{MAX} \geq I_{OUT1\_MAX} + \frac{\Delta I_L}{2},$$

$$\Delta I_L = \frac{V_{PVCC1V} - V_{OUT1}}{L} \times \frac{D_1}{f_{OSC1}}, D_1 = \frac{V_{OUT1}}{V_{PVCC1}}$$

Where:

IL_{MAX}: Rated current of inductor (A)

I_{OUT1_MAX}: Maximum load current (A)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

L: Inductance of inductor (H)

D_1: On-duty for DD1V

V_{PVCC1V}: Power supply voltage of DD1V (V)

V_{OUT1}: Output setting voltage of DD1V (V)

f_{OSC1}: Switching frequency of DD1V (Hz)

If the inductor peak current reaches the overcurrent protection (OCP) detection current, OCP lowers the output voltage, thus preventing the inductor peak current from exceeding the inductor's rated current limit, IL_{MAX}. You need to consider the inductance change due to the inductor's DC bias characteristic.

2.1.3 Input capacitor (C_{IN})

A ceramic capacitor that has a low equivalent series resistance (ESR), typically less than 10 mΩ, and excellent frequency characteristics—that is, the capacitance does not diminish at the switching frequency—should be used. Generally, the capacitance should be selected among the value of the E6 series of preferred numbers. The recommended value is no less than 4.7 µF. Calculate the necessary rated voltage of the input capacitor by using **Equation 3**.

Equation 3

$$V_{CIN} > V_{PVCC1V}$$

Where

V_{CIN}: Rated voltage of input capacitor (V)

V_{PVCC1V}: Power supply voltage of DD1V (V)

[1] E6 series is the number series with the two significant digits (10, 15, 22, 33, 47, 68) defined in IEC 60063:2015.

2.1.4 Output capacitor (C_{OUT})

A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. The recommended capacitance values is no less than 22 µF. Use a large capacitance (two 22-µF capacitors recommended) to prevent power good 1 false triggering by mitigating the voltage deviation caused by load transients (e.g., from 0 A to the max load current in 10 µs). An approximate output voltage undershoot / overshoot value of the load transient response without load regulation variant is calculated by using **Equation 4**.

Equation 4

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} \times \left(\frac{1}{2 \times f_{OSC1}} + \frac{1}{8 \times f_{BW}}\right)}{C_{OUT}}$$

Where:

ΔV_{OUT}: Output voltage undershoot / overshoot caused by the load transient (V)

ΔI_{OUT}: Transient value of the output current (A)

f_{OSC1}: Switching frequency of DD1V (Hz)

f_{BW}: Feedback loop bandwidth of DD1V (Hz)

The **Gain-Phase calculation tool** can simulate its approximately value.

C_{OUT}: Output capacitor (F)

The switching ripple voltage is calculated using **Equation 5**.

Equation 5

$$\Delta V_{OUT\_SW} = \Delta V_{OUT\_SW\_C} + \Delta V_{OUT\_SW\_ESR},$$

$$\Delta V_{OUT\_SW\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{OSC1}},\ \Delta V_{OUT\_SW\_ESR} = \Delta I_L \times ESR$$

Where:

ΔV_{OUT_SW}: Output switching ripple total voltage (V)

$\Delta V_{OUT\_SW\_C}$: Output switching ripple voltage caused by the capacitance (V)

$\Delta V_{OUT\_SW\_ESR}$: Output switching ripple voltage caused by ESR of the output capacitor (V)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

f_{OSC1}: Switching frequency of DD1V (Hz)

C_{OUT}: Output capacitor (F)

ESR: ESR of the output capacitor (Ω)

Component selection

When choosing a ceramic capacitor, you should take into account the reduction of capacitance due to the DC bias characteristics of the capacitor itself. Generally, a large-sized capacitor has a stable DC bias characteristic.

Calculate the necessary rated voltage of the output capacitor by using **Equation 6**.

Equation 6

$$V_{COUT} > V_{OUT}$$

Where:

V_{COUT}: Rated voltage of output capacitor (V)

V_{OUT}: Output setting voltage of DD1V (V)

2.2 DC/DC converter (DD5V)

Figure 3 depicts the DD5V DC/DC converter section in the S6BP501A/S6BP502A application example. LX5, VOUT5V, FB5V, and PGND5V are the terminal names of the PMIC (refer to the **datasheet**). This section explains how to choose each component in **Figure 3**.

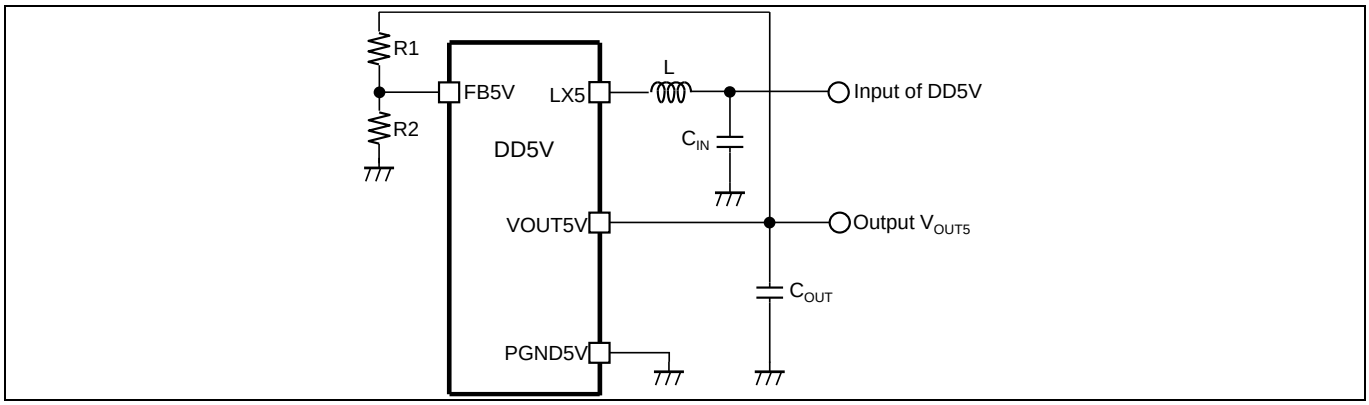

Figure 3 Connection of DD5V DC/DC converter

2.2.1 Output setting resistors (R1, R2)

A pair of voltage dividing resistors (R1 and R2) configures the output voltage (V_{OUT5}) according to **Equation 7**. Refer to the DD5V output voltage setting range in the datasheet. By increasing the resistance value, the efficiency will be improved with a light load. But with a high resistance value, the load tends to be vulnerable to noise. **Table 3** gives the recommended value, considering the efficiency improvement at light loads.

Equation 7

$$V_{OUT5} = V_{FB5V} \times \frac{R1 + R2}{R2}$$

Where:

R1, R2: Output voltage setting resistance (Ω)

V_{FB5V}: DD5V FB voltage = 1.2 V

V_{OUT5}: DD5V output setting voltage (V)

Table 3 DD5V output voltage setting resistor

DD5V setting voltage	R1	R2
5.00 V	3.8 MΩ (2 MΩ + 1.8 MΩ)	1.2 MΩ

If each resistance value is reduced to a tenth as listed in **Table 4**, the supply current increases about 5 µA (when VIN = 12 V).

Table 4 DD5V output voltage setting resistor

DD5V setting voltage	R1	R2
5.00 V	380 kΩ (200 kΩ + 180 kΩ)	120 kΩ

2.2.2 Inductor (L)

Generally, the inductance of the inductor should be selected from among values of the E6 series of preferred numbers. The recommended inductor value for S6BP501A/S6BP502A is 1.5 µH. Also, you should calculate the maximum current value using **Equation 2** to confirm whether the electric current that flows through the inductor is within the rated parameters for the inductor.

Equation 8

$$IL_{MAX} \geq \frac{I_{OUT5\_MAX}}{D_5'} + \frac{\Delta I_L}{2}, \quad D_5' = \frac{V_{IN\_DD5V}}{V_{OUT5}}, \quad \Delta I_L = \frac{V_{IN\_DD5}}{L} \times \frac{(1\text{-}D_5')}{f_{OSC1}}$$

Where:

IL_{MAX}: Rated current of inductor (A)

I_{OUT5_MAX}: Maximum load current (A)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

L: Inductance of inductor (H)

D_5': Off-duty for DD5V

V_{IN_DD5V}: Power supply voltage of DD5V (V)

V_{OUT5}: Output setting voltage of DD5V (V)

f_{OSC1}: Switching frequency of DD5V (Hz)

If the inductor peak current reaches the overcurrent protection (OCP) detection current, OCP lowers the output voltage thus preventing the inductor peak current from exceeding the inductor's rated current limit, IL_{MAX}. You need to consider the inductance change due to the inductor's DC bias characteristic.

2.2.3 Input capacitor (C_{IN})

A ceramic capacitor that has a low ESR, typically less than 10 mΩ, and excellent frequency characteristics, where the capacitance does not diminish at switching frequency, should be used. Generally, the capacitance should be selected among the value of the E6 series of preferred numbers. The recommended value is no less than 4.7 µF. Calculate the necessary rated voltage of the input capacitor by using **Equation 9**.

Equation 9

$$V_{CIN} > V_{IN\_DD5V}$$

Where

V_{CIN}: Rated voltage of input capacitor (V)

V_{IN_DD5V}: Power supply voltage of DD5V (V)

2.2.4 Output capacitor (C_{OUT})

A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. The recommended capacitance values is no less than 88 µF. Use a large capacitance (five 47-µF capacitors recommended) to prevent power good 5 (PG5) false triggering by mitigating the voltage deviation caused by load transients (e.g., from 0 A to the max load current in 10 µs). Approximate output voltage undershoot / overshoot caused by the load transient response without load regulation variant is calculated by using **Equation 4**.

Equation 10

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} \times \left(\frac{1}{2 \times f_{OSC1}} + \frac{1}{8 \times f_{BW}}\right)}{C_{OUT}}$$

Where:

ΔV_{OUT}: Output voltage undershoot / overshoot caused by the load transient (V)

ΔI_{OUT}: Transient value of the output current (A)

f_{OSC1}: Switching frequency of DD5V (Hz)

f_{BW}: Feedback loop bandwidth of DD5V (Hz)

The **Gain-Phase calculation tool** can simulate its approximately value.

C_{OUT}: Output capacitor (F)

When you consider a ceramic capacitor, you should take into account the reduction in capacitance due to the DC bias characteristics of the capacitor itself. Generally, a large-sized capacitor has a stable DC bias characteristic.

Calculate the necessary rated voltage of the output capacitor by using **Equation 11**.

Equation 11

$$V_{COUT} > V_{OUT5}$$

Where:

V_{COUT}: Rated voltage of output capacitor (V)

V_{OUT5}: Output setting voltage of DD5V (V)

2.3 DC/DC converter (DD3V)

Figure 4 depicts the DD3V DC/DC converter section in the S6BP501A/S6BP502A application example. CSN, CSP, BST3V, DRVH3V, DRVL3V, LX3V, FB3V, IN3V, VOUT3V and PGND3V are the terminal names of the PMIC (refer to the **datasheet**). This section explains how to choose each component in **Figure 4**.

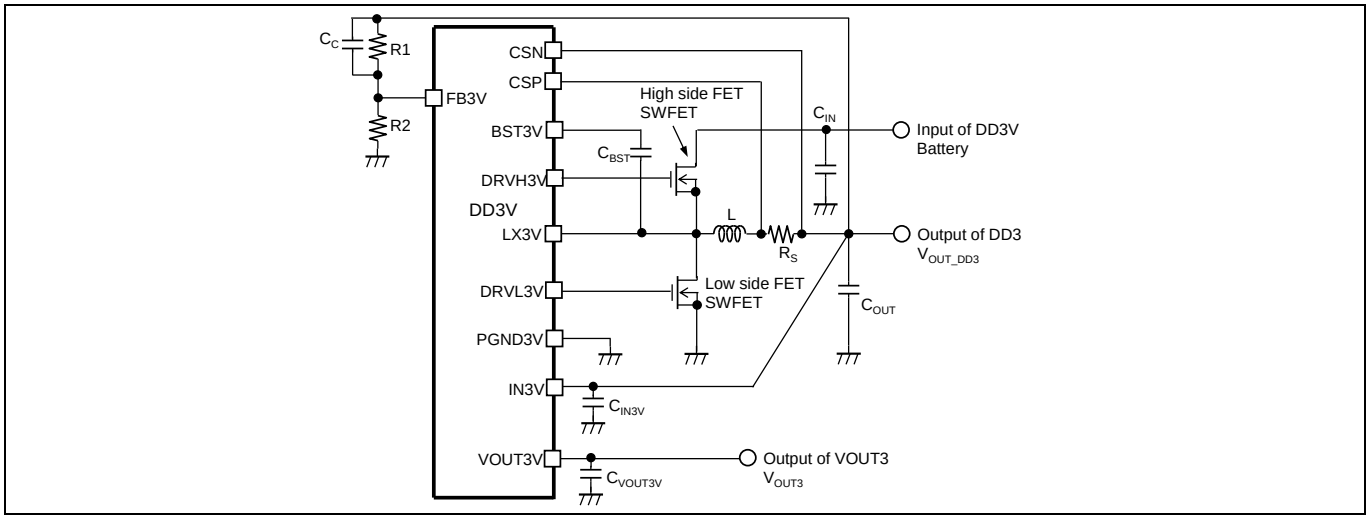

Figure 4 Connection of DD3V DC/DC converter

2.3.1 Output setting resistors (R1, R2) and phase compensation capacitor (C_C)

A pair of voltage dividing resistors (R1 and R2) configures the output voltage (V_{OUT_DD3}) according to **Equation 12**. Refer to the DD3V output voltage setting range in the datasheet. Calculate the output voltage by using **Equation 12**. By increasing the resistance value, the efficiency will be improved with a light load. But with a high resistance value, the load tends to be vulnerable to noise. **Table 5** gives the recommended value.

Equation 12

$$V_{OUT\_DD3} = V_{FB3V} \times \frac{R1 + R2}{R2}$$

Where:

R1, R2: Output voltage setting resistance (Ω)

V_{FB3V}: DD3V FB voltage = 0.9 V

V_{OUT_DD3}: DD3V output setting voltage (V)

Table 5 DD3V output voltage setting resistor and phase compensation capacitor

DD3V setting voltage	R1	R2	C_C
3.30 V	320 kΩ (200 kΩ + 120 kΩ)	120 kΩ	10 pF

If the resistance of R1 and R2 is increased, the output capacitance should be increased to the same degree.

Changing the output capacitors or output voltage setting resistors may lead to changes in gain-phase characteristics, and therefore, results in possible lower phase margin. In this case, the low phase margin can be boosted by optimizing the compensation capacitance (Cc). Compensation capacitance (Cc) can be calculated by using **Equation 13**.

Equation 13

$$C_c = \frac{1 - \sqrt{1 - 1.2 \times V_{OUT\_DD3}/(V_{OUT\_DD3} - 0.9)^2}}{7.3 \times f_{co} R_2}$$

Where:

f_{co}: Crossover frequency by measurement of gain-phase characteristic without Cc.

R2: Output voltage setting resistance (Ω)

V_{OUT_DD3}: DD3V output setting voltage (V)

2.3.2 Inductor (L)

Generally, the inductance of the inductor should be selected from among values of the E6 series of preferred numbers. The recommended inductor value for S6BP501A/S6BP502A is 4.7 µH. Also, you should calculate the maximum current value using **Equation 2** to confirm whether the electric current that flows through the inductor is within the rated parameters for the inductor.

When connecting the output of DD3V to the input of DD5V and DD1V:

Equation 14

$$IL_{MAX} \geq I_{DD3\_MAX} + \frac{\Delta I_L}{2}$$

$$I_{DD3\_MAX} = I_{OUT3\_MAX} + I_{IN1\_MAX} + I_{IN5\_MAX}$$

$$I_{IN1\_MAX} = D_1 \times I_{OUT1\_MAX}$$

$$I_{IN5\_MAX} = \frac{I_{OUT5\_MAX}}{D_5'}, \quad \Delta I_L = \frac{V_{IN} - V_{OUT3}}{L} \times \frac{V_{OUT3}}{V_{VIN} \times f_{OSC2}}$$

Where:

IL_{MAX}: Rated current of inductor (A)

I_{DD3V_MAX}: Maximum load current (A)

I_{OUT3_MAX}: Maximum load current (A)

I_{IN5_MAX}: DD5V maximum input current (A)

I_{IN1_MAX}: DD1V maximum input current (A)

D_5': OFF Duty for DD5V

D_1: ON Duty for DD1V

V_{IN}: Power supply voltage of DD3V (V)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

L: Inductance of inductor (H)

f_{OSC2}: Switching frequency of DD3V (Hz)

If the inductor peak current reaches the overcurrent protection (OCP) detection current, OCP lowers the output voltage thus preventing the inductor peak current from exceeding the inductor's rated current limit, IL_{MAX}. You need to consider the inductance change due to inductor's DC bias characteristic.

The ESR of the inductor (RDC) affects the minimum required supply voltage for maintaining the output voltage of DD3V. Consider this power supply voltage along with the on-resistance described in the **2.3.5 Switching FET (SWFET)** section.

2.3.3 Input capacitor (C_{IN})

A ceramic capacitor that has a low ESR, typically less than 10 mΩ, and excellent frequency characteristics—that is, the capacitance does not diminish at switching frequency—should be used. Generally, the capacitance should be selected among the value of the E6 series of preferred numbers. The recommended value is no less than 10 µF. Calculate the necessary rated voltage of the input capacitor by using **Equation 15**.

Equation 15

$$V_{CIN} > V_{IN}$$

Where

V_{CIN}: Rated voltage of input capacitor (V)

V_{IN}: Power supply voltage of DD3V (V)

2.3.4 Output capacitor (C_{OUT})

A ceramic capacitor that has a low ESR and excellent frequency characteristics—that is, the capacitance is not reduced up to the switching frequency—should be used. Generally, the capacitance should be selected from among values of the E6 series of preferred numbers. The recommended capacitance value for the DC/DC converter of the device is more than 132 µF (six 22-µF capacitors). Because the output of DD3V is connected to the input of DD1V and DD5V, the output capacitance value of DD3V includes the input capacitances of DD1V and DD5V. Reduce the required capacitance, if possible, by increasing the value of the current sense resistor.

Use a large capacitance (ten 47-µF capacitors recommended) to prevent power good 3 (PG3) false triggering by mitigating the voltage deviation caused by load transients (e.g. from 0 A to max load current in 10 µs). An approximate output voltage undershoot / overshoot caused by the load transient response without the load regulation characteristic is calculated by using **Equation 16**.

Equation 16

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} \times \left(\frac{1}{2 \times f_{OSC2}} + \frac{1}{8 \times f_{BW}}\right)}{C_{OUT}}$$

Where:

ΔV_{OUT}: Output voltage undershoot / overshoot caused by the load transient (V)

ΔI_{OUT}: Transient value of the output current of DD3V (A)

f_{OSC2}: Switching frequency of DD3V (Hz)

f_{BW}: Feedback loop bandwidth of DD3V (Hz)

The **Gain-Phase calculation tool** can simulate its approximately value.

C_{OUT}: Output capacitor (F)

When you consider a ceramic capacitor, you should take into account the reduction of capacitance due to the DC bias characteristics of the capacitor itself. Generally, a large-sized capacitor has a stable DC bias characteristic. Calculate the necessary rated voltage of the output capacitor by using **Equation 17**.

Equation 17

$$V_{COUT} > V_{OUT\_DD3}$$

Where:

V_{COUT}: Rated voltage of output capacitor (V)

V_{OUT_DD3}: Output setting voltage of DD3V (V)

2.3.5 Switching FET (SWFET)

The total loss of the high-side FET can be reduced if it has the same conduction loss and switching loss. The power loss of the high-side FET should be lower than the rating power loss. Use **Equation 18** to calculate the power loss of the high-side FET.

Equation 18

$$P_{HighFET} = P_{RON\_High} + P_{SW\_High}$$

Where:

$P_{HighFET}$: Loss of high-side FET (W)

P_{RON_High}: Conductive loss of high-side FET (W)

P_{SW_High}: Switching loss of high-side FET (W)

Calculate the conductive loss of the high-side FET using **Equation 19**.

Equation 19

$$P_{RON\_High} = I_{OUT\_MAX}{}^2 \times \frac{V_{OUT\_DD3}}{V_{IN}} \times R_{ON\_High}$$

Where:

P_{RON_High}: Conductive loss of high-side FET (W)

I_{OUT_MAX} : Maximum load current (A)

V_{IN}: Power supply voltage of DD3V (V)

V_{OUT_DD3}: DD3V output setting voltage (V)

R_{ON_High}: High-side FET on-resistance (Ω)

Calculate the approximate switching loss of the high-side FET by using **Equation 20**.

Equation 20

$$P_{SW\_High} \approx 1.5 \times V_{IN} \times f_{OSC2} \times I_{OUT\_MAX} \times Q_{SW}$$

Where:

P_{SW_High}: Switching loss of high-side FET (W)

V_{IN}: Power supply voltage of DD3V (V)

f_{OSC2}: Switching frequency of DD3V (Hz)

I_{OUT_MAX}: Maximum load current (A)

Q_{SW}: Switching gate charge of high-side FET (C)

The on-resistance of the high-side FET and the ESR of the inductor (RDC) affect the required minimum supply voltage for maintaining the output voltage of DD3V. The lowest power supply voltage value can be calculated using **Equation 21**. Make sure that each resistance value is within the allowable range in the use conditions.

Equation 21

$$V_{IN\_MIN} = (R_{ON\_High} + RDC) \times I_{DD3V\_MAX}$$

Where:

$V_{IN\_\_MIN}$: Minimum required power supply voltage of DD3V to maintain output voltage (V)

R_{ON_High}: High-side FET on-resistance (Ω)

RDC: ESR of inductor (Ω)

I_{DD3V_MAX}: Maximum load current of DD3V (A)

Total gate charge of the low-side FET being too large may cause switching of DD3V to stop. Low-side FET with total gate charge less than 19 nC at gate-source voltage of V_{GS}=5V is required (In the case of PMIC T_J=+125°C, low-side FET total gate charge must be less than 20 nC at V_{GS}=5V). Additionally, FET with low on-resistance is recommended for the low-side FET, thereby effectively decreasing the loss, especially in the low on-duty mode. The loss of the low-side FET can be calculated by using **Equation 22**.

Equation 22

$$P_{LowFET} = P_{Ron\_Low} = I_{OUT\_MAX}{}^2 \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{on\_Low}$$

Where:

P_{Ron_Low}: Conductive loss of low-side FET (W)

I_{OUT_MAX}: Maximum load current (A)

V_{IN}: Power supply voltage of DD3V (V)

V_{OUT_DD3}: DD3V output setting voltage (V)

R_{on_Low}: Low-side FET on-resistance (Ω)

ON/OFF voltage of the low-side FET is generally minimal, so the switching loss is small enough to be ignored. Therefore, it is omitted here.

The average current that flows through the switching FET should be calculated to determine whether it is within the rated value.

Calculate the required rated current of the switching FET by using **Equation 23**.

Equation 23

$$I_{D\_High} > I_{OUT\_MAX} \times D \text{ , } I_{D\_Low} > I_{OUT\_MAX} \times (1-D)$$

Where:

I_{D_High}: High-side FET drain current (A)

I_{D_Low}: Low-side FET drain current (A)

I_{OUT_MAX}: Maximum load current (A)

D: On-duty

Calculate the required rated voltage of the switching FET by using **Equation 24**.

Equation 24

$$V_{DSS} > V_{IN}$$

Where:

V_{DSS}: High-side FET and low-side FET voltage between drain and source (V)

V_{IN}: DD3V input voltage (V)

2.3.6 Boot strap capacitor (C_{BST})

To drive the gate of the high-side FET, the bootstrap capacitor must have enough stored charge: 0.1 µF as the standard value. However, it is necessary to adjust that number when the high-side FET Q_G is large. The limit is 0.47 µF. The required minimal bootstrap capacitance value can be calculated by using **Equation 25**.

Equation 25

$$C_{BST} \geq 10 \times Q_G$$

Where:

C_{BST}: Boot strap capacitance (F)

Q_G: Total gate charge of high-side FET (C)

Moreover, when the load suddenly changes to the light load in automatic PWM/PFM switching mode, the switching operation is paused until the DD3V output overshoot voltage is eliminated by load discharge. After that, sufficient charge of bootstrap capacitor is necessary to drive the gate of the DD3V high-side FET, and the bootstrap capacitance value must be over the minimum value, which can be calculated using the **Equation 26**.

Equation 26

$$C_{BST} \geq \frac{(6.79\times10^{2}\times C_{OUT}{}^{2}-0.595\times C_{OUT}+280\times10^{-6})\times C_{OUT}}{(5-V_{TH\_High})\times(0.1\times10^{-3}+I_{OUT5\_MIN}+\frac{V_{OUT\_DD3}}{R1+R2})\times10^{3}}$$

Where:

C_{BST}: Bootstrap capacitance (F)

Q_G: Total gate charge of high-side FET (C)

C_{OUT}: DD3V output capacitance(F)

V_{TH_High}: Threshold voltage of DD3V high-side FET(V)

I_{OUT5_MIN}: DD5V minimum load current (A)

V_{OUT_DD3} : DD3V output setting voltage (V)

R1, R2: DD3V output voltage setting resistance (Ω)

When the DD3V input voltage drops below V_{IN_MIN}, which can be calculated by **Equation 21**, the high-side FET has to keep the on-state because the high-side FET on-duty becomes 100%. In this period, the bootstrap capacitor is not charged and the high-side FET gate voltage may drop. Therefore, it necessary that DD3V power supply voltage dropping time is shorter than the high-side FET on-duration time (T_{ONDT}). T_{ONDT} can be calculated by the following equation:

Equation 27

$$T_{ONDT} = \{1.675-2\times\ln(\frac{1.34+V_{TH\_High}}{3.45})\}\times C_{BST}\times10^{6}$$

Where:

T_{ONDT}: DD3V input voltage dropping Period (s)

C_{BST}: Bootstrap capacitance (F)

V_{TH_High}: Threshold voltage of DD3V high-side FET(V)

Figure 5 shows a graph example of the value calculated by **Equation 26** and **Equation 27**.

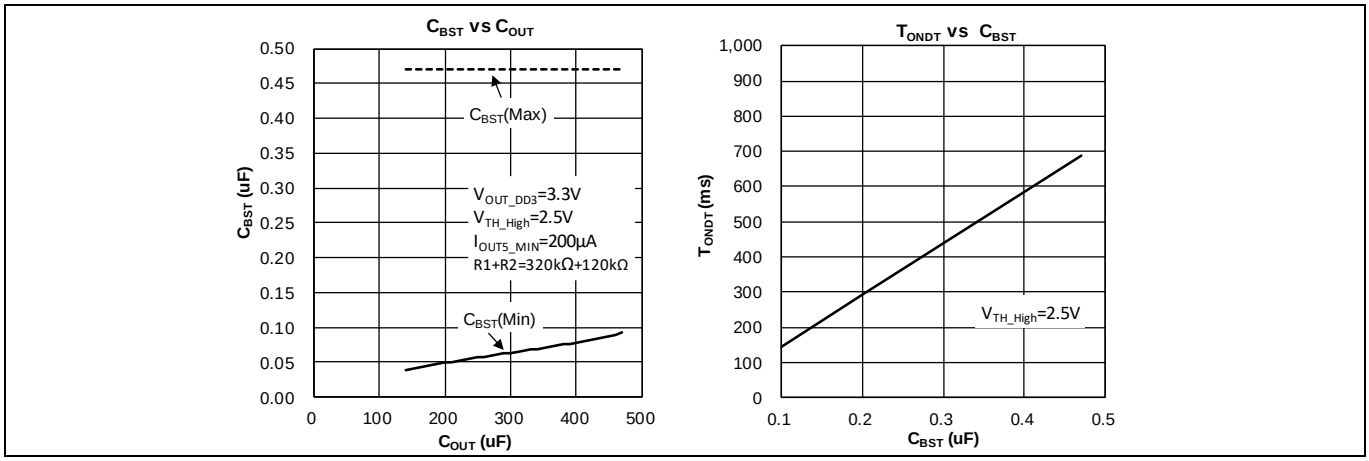

Figure 5 Bootstrap capacitance graph

Calculate the required rated voltage of the boot strap capacitor by using **Equation 28**.

Equation 28

$$V_{CBST} > V_{VB}$$

Where:

V_{CBST}: Rated voltage of boot strap capacitor (V)

V_{VB}: Output voltage of VB regulator (V)

2.3.7 Current sense resistor (R_S)

This resistance affects the stable operation of the DD3V. **Table 6** gives the recommended value.

Table 6 DD1V current sense resistance

Part Number	R_S
S6BP501A	12 mΩ or 10 mΩ
S6BP502A	10 mΩ

Use **Equation 29** to calculate the DD3V output current limit with each current sense resistance.

Equation 29

$$I_{DD3V\_LIM} = \frac{V_{LIM3}}{R_S} - \frac{\Delta I_L}{2}$$

Where:

I_{DD3V_LIM}: Output current limit of DD3V (A)

V_{LIM3}: Threshold voltage overcurrent monitor of DD3V = 0.08 V

R_S: Current sense resistance (Ω)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

When increasing the current sense resistance to reduce output capacitance, you should pay attention to the lower output current limit which might affect your system performance, as described above. Calculate the rated dissipation of the current sense resistor by using **Equation 30**.

Equation 30

$$P_{RS} > I_{DD3\_MAX}{}^{2} \times R_S$$

Where:

P_{RS}: Rated dissipation of current sense resistor (W)

I_{DD3_MAX}: Maximum output current of DD3V (A)

R_S: Current sense resistance (Ω)

2.3.8 Load switch capacitor (C_{IN3V}, C_{VOUT3V})

DD3V block has a load switch that is connected to IN3V and VOUT3V of PMIC terminal. These terminals need to be connected to capacitor. **Table 7** gives the recommended value.

Table 7 IN3V and VOUT3V capacitors

C_{IN3V}	C_{VOUT3V}
0.1 µF	1 µF

The rated voltage of these capacitors must be at least equal to the DD3V output voltage.

2.4 Common section

Figure 6 depicts the common section in the S6BP501A/S6BP502A application example. VIN, VOUT5V, VB, and VDD are the terminal names of the PMIC (refer to the **datasheet**).

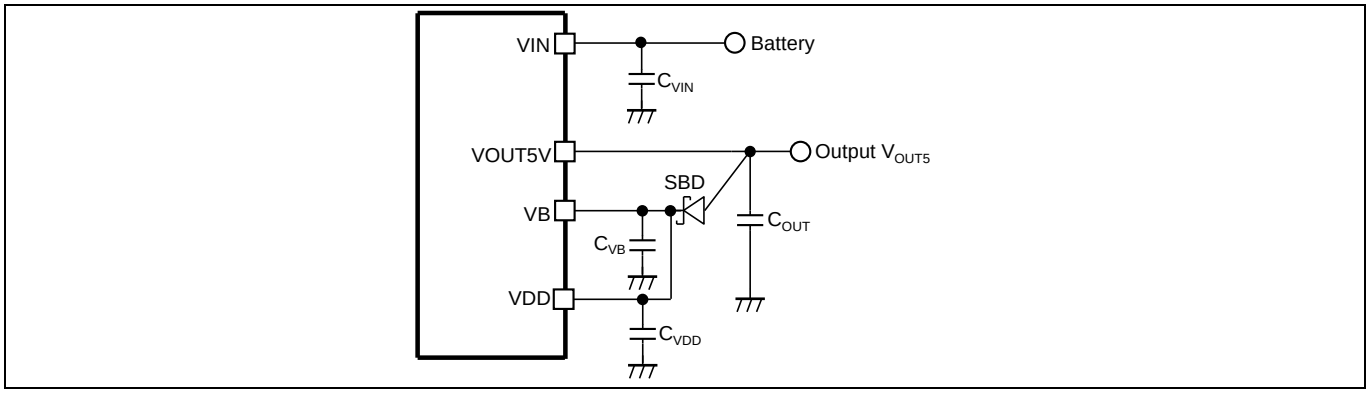

Figure 6 Connection of regenerative diode and bypass capacitor

2.4.1 Regenerative schottky barrier diode (SBD)

SBD is a diode for supplying voltage from the VOUT5V pin to the VB and VDD pins. A sufficient current rating is 100 mA. The rated voltage must be at least equal to the VB voltage and the DD5V out voltage.

2.4.2 VIN bypass (C_{VIN}), VB bypass (C_{VB}), and VDD bypass capacitor (C_{VDD})

A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. The recommended value for these capacitors is 1 µF. **Table 8** gives the recommended capacitance values.

Table 8 Bypass output capacitance

C_{VIN}	C_{VB}	C_{VDD}
0.1 µF	4.7 µF	0.1 µF–4.7 µF

Calculate the necessary rated voltage of the capacitor by using **Equation 31**.

Equation 31

$$V_{CVIN} > V_{IN}, V_{CVB} > V_{VB}, V_{CVDD} > V_{VB}$$

Where:

V_{CVIN}: Rated voltage of bypass input capacitor (V)

V_{IN}: Power supply voltage (V)

V_{CVB}: Rated voltage of VB bypass capacitor (V)

V_{CVDD}: Rated voltage of VDD bypass capacitor (V)

V_{VB}: VB voltage (V)

2.4.3 PG1V, PG2V, PG3V and HOT pull-up resistor

PG1V, PG2V, PG3V, and HOT are the terminal names of the PMIC (refer to the **datasheet**).Considering that the leakage current of each terminal is less than 1 µA and the driving ability of this IC is 3 mA, the resistance should be selected in the range of 2 kΩ to 100 kΩ with a 5 V pull-up.

3 PCB layout guidelines

This section explains how to design the PCB for a power management system with S6BP501A or S6BP502A.

3.1 DC/DC converter (DD1V)

Figure 7 shows an example layout of the DC/DC converter (DD1V) section shown in **Figure 2**.

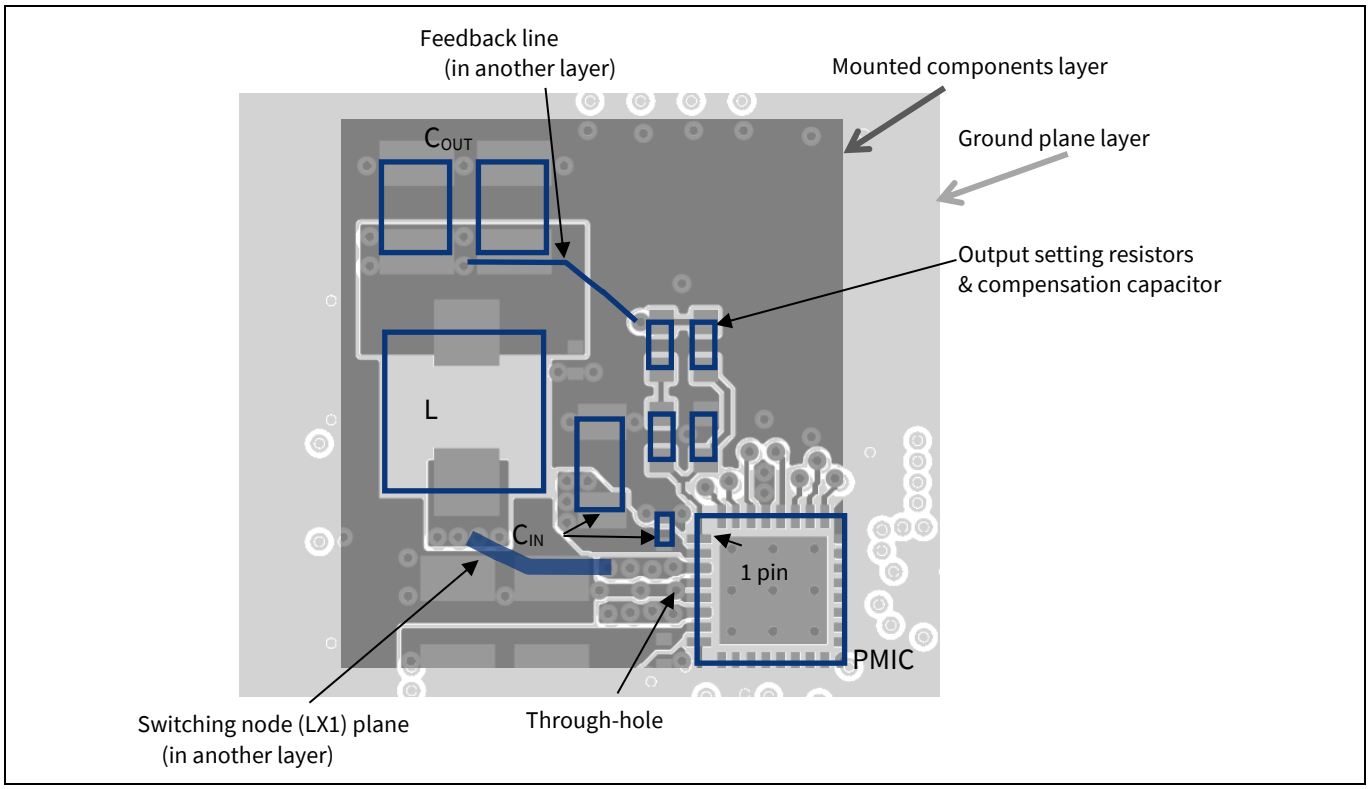

Figure 7 Layout example of DD1V

Place the switching components (C_{IN}, L, PMIC, and C_{OUT}) on the same side of the PCB. These components should be connected to a wide and short plane. In particular, the current loop that includes the input capacitor (C_{IN}) and PMIC (PVCC1V and PGND1V terminal) should be carefully chosen to minimize the loop size. Another PCB layer, without any component mounted, should be used as a ground plane. The ground terminal of the switching component should be connected to this ground plane by through-holes placed nearby.

Output setting resistors and a phase compensation capacitor should be placed near the PMIC. The feedback line from the output of DD1V to the output voltage setting resistor should be wired separately from the power line.

This line should be kept away from the switching components and the pattern of the LX1V terminal as much as possible because it is sensitive to noise. There is leakage flux near the inductor (L) location on both its mounted plane and its back plane. Sensitive wiring and components should be placed away from the inductor (L) location on both its mounted plane and its back plane.

3.2 DC/DC converter (DD5V)

Figure 8 shows an example layout of the DC/DC converter (DD5V) section shown in **Figure 3**.

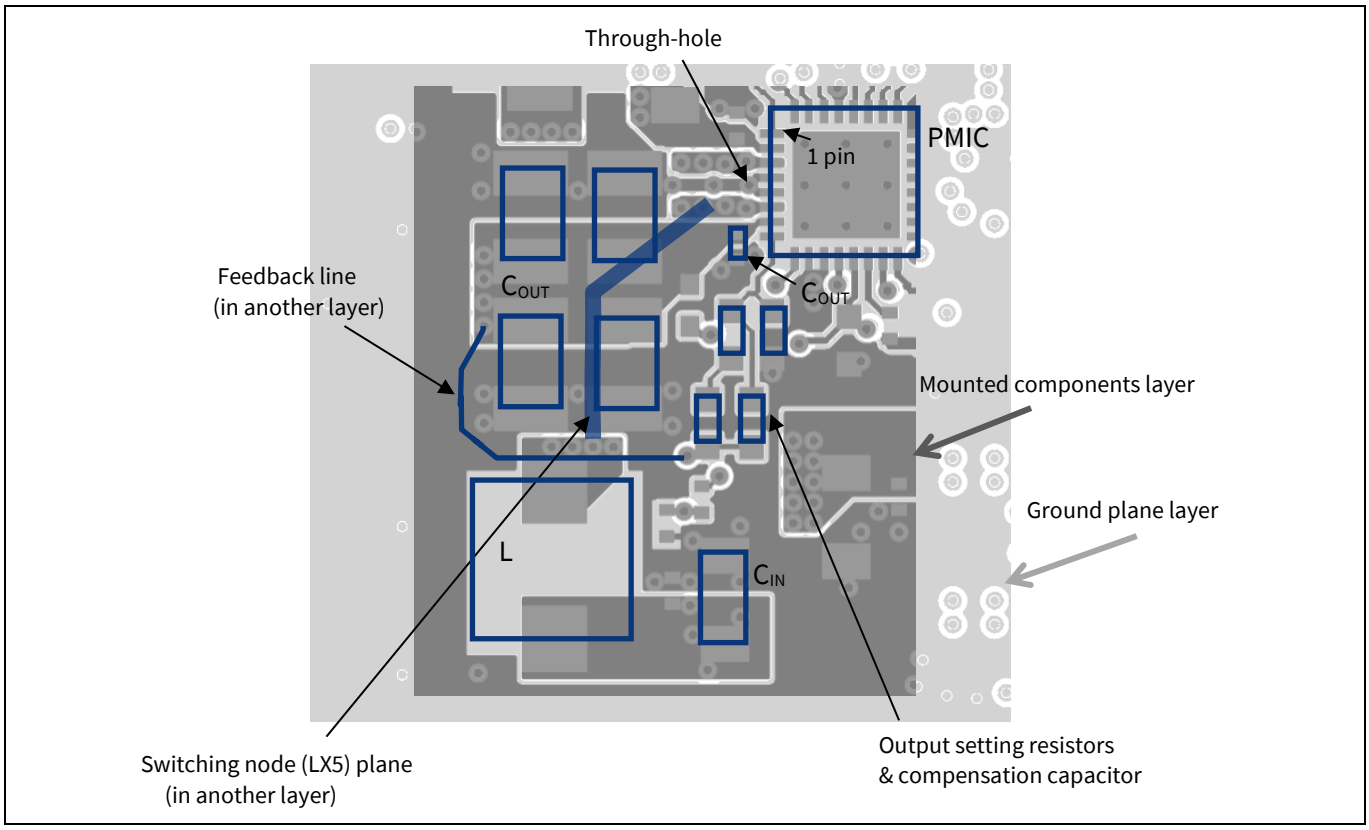

Figure 8 Layout example of DD5V

Place the switching components (C_{IN}, L, PMIC, and C_{OUT}) on the same side of the PCB. These components should be connected to a wide and short plane. In particular, the current loop that includes the output capacitor (C_{OUT}) and PMIC (VOUT5V and PGND5V terminal) should be carefully chosen to minimize the loop size. Another PCB layer, without any component mounted, should be used as a ground plane. The ground terminal of the switching component should be connected to this ground plane by through-holes placed nearby.

Output setting resistors and a phase compensation capacitor should be placed near the PMIC. The feedback line from the output of DD5V to the output voltage setting resistor should be wired separately from the power line.

This line should be kept away from the switching components and the pattern of the LX5V terminal as much as possible because it is sensitive to noise. There is a leakage flux near the inductor (L) location on both its mounted plane and its back plane. Sensitive wiring and components should be placed away from the inductor (L) location on both its mounted plane and its back plane.

3.3 DC/DC converter (DD3V)

Figure 9 shows an example layout of the DC/DC converter (DD3V) section shown in **Figure 4**.

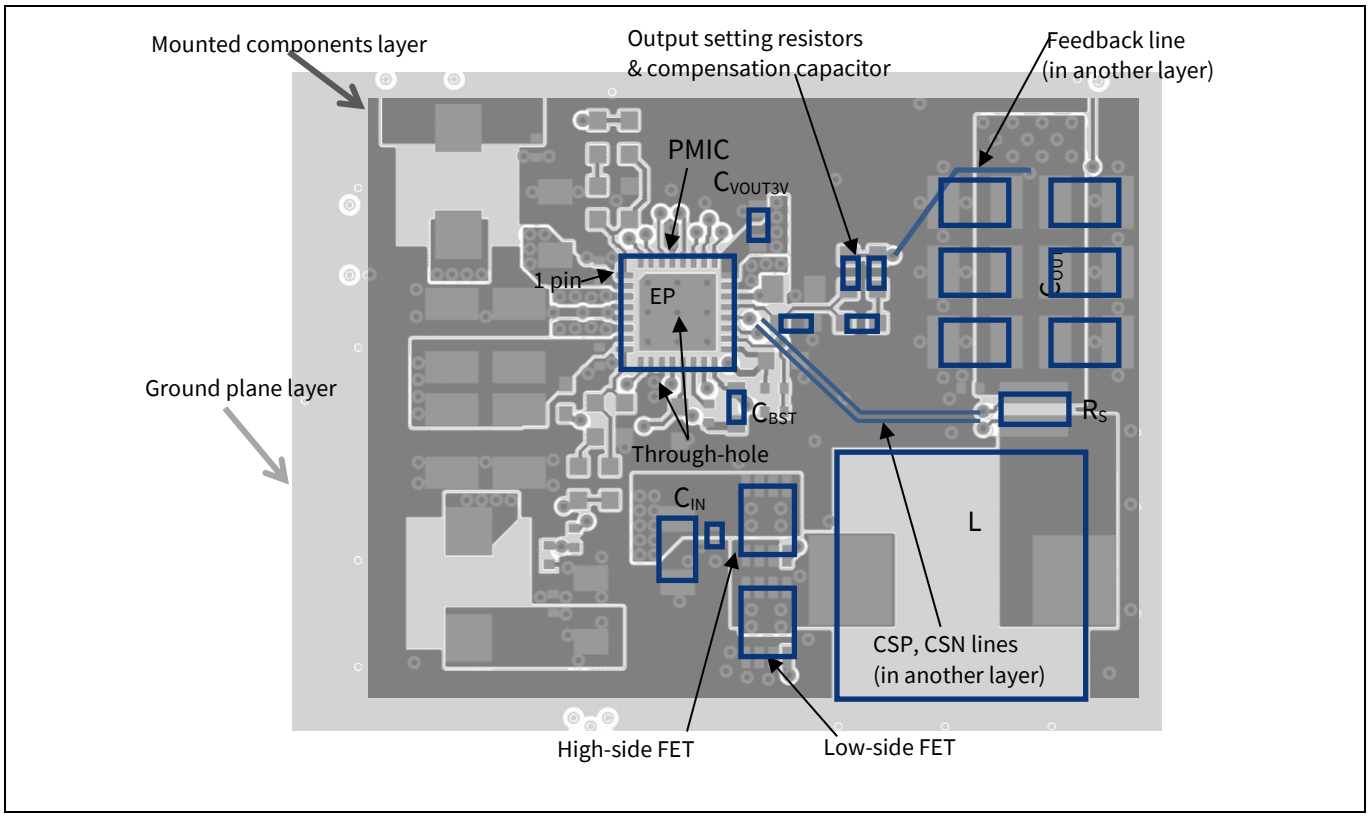

Figure 9 Layout example of DD3V

The switching components (C_{IN}, L, SWFETs [high-side FET and low-side FET], Rs, and C_{OUT}) should be placed on the same side of the PCB. These components should be connected to a wide and short plane. In particular, the current loop that includes the input capacitor (C_{IN}) and SWFET (from drain to source of high-side FET and from drain to source of low-side FET) should be carefully chosen to minimize the loop size. Another PCB layer, without any component mounted, should be used as a ground plane. The ground terminal of the switching component should be connected to this ground plane by through-holes placed nearby.

The pattern of the DRVH3V and DRVL3V terminals should be wired to handle the momentary current flow of approximately 1 A to drive the gate of the FET. DRVL3V terminal should be shorted to the synchronous FET gate.

The bootstrap capacitor (C_{BST}) should be placed near the PMIC (BST3V and LX3V terminals).

The output setting resistors and the phase compensation capacitor should be placed near the PMIC. The feedback line from the output of DD3V to the output voltage setting resistor should be wired separately from the power line.

This line should be kept away from the switching components and the pattern of the LX3V terminal as much as possible because it is sensitive to noise.

The wires from the current sense resistor should be separated from the plane with a large current flow. They should also be wired parallel and close to each other and connected to the CSP CSN terminal. The wires to the CSP and CSN terminals should be kept away from switching components as much as possible because the wiring is sensitive to noise.

There is a leakage flux near the inductor (L) location on both its mounted plane and its back plane. Sensitive wiring and components should be placed away from the inductor (L) location on both its mounted plane and its back plane.

The VOUT3V capacitor (C_{VOUT3V}) should be placed near the PMIC (VOUT3V terminals).

3.4 Common section

Bypass capacitors (C_{VIN}, C_{VDD}, C_{VB}) should be placed near the VIN, VDD, and VB terminals of the PMIC. The GND terminals of the bypass capacitors should be connected to the inner GND layer by through-holes proximal to the terminals.

Place a solder pad under the exposed pad (EP) of the PMIC. For heat dissipation, connect this EP footprint to the inner GND layer by through-holes. (Refer to **Figure 9**.)

Revision history

Document version	Date of release	Description of changes
**	2015-12-04	New application note.
*A	2016-05-19	Updated Document Title to read as “AN99435 - Designing a Power Management System with S6BP501A and S6BP502A”. Updated Introduction: Updated Table 1. PMICs lineup. Updated Component selection: Updated DC/DC converter (DD1V): Updated Output setting resistors (R_1, R_2) and phase compensation capacitor (C_C): Updated Table 2. DD1V output voltage setting resistor. Updated DC/DC converter (DD3V): Added “Load switch capacitor (C_{IN3V}, $C_{VOUT\ 3V}$)”. Added “PCB layout guidelines”. Updated to new template.
*B	2017-08-30	Updated Cypress Logo and Copyright.
*C	2017-09-25	Updated Component selection: Updated DC/DC converter (DD5V): Updated Inductor (L): Updated Equation 6. Updated DC/DC converter (DD3V): Updated Switching FET (SWFET): Updated Equation 15. Updated Boot strap capacitor (C_{BST}): Updated description. Updated Current sense resistor (R_S): Updated Equation 24.
*D	2018-03-14	Updated Component selection: Updated DC/DC converter (DD3V): Updated Output setting resistors (R_1, R_2) and phase compensation capacitor (C_C): Updated description. Updated to new template.
*E	2018-12-21	Updated Component selection: Updated DC/DC converter (DD1V): Updated Output capacitor (C_{OUT}): Updated description.
*F	2021-06-11	Updated to Infineon template.

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