AN99207

Understanding AC Characteristics

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AN99207 provides a basic explanation of AC characteristics and clarifies some frequently misunderstood ones t_{OE}, t_{ACC}, t_{CE}, t_{PACC}, t_{IACC}, t_{BACC}, and t_{RDYS}.

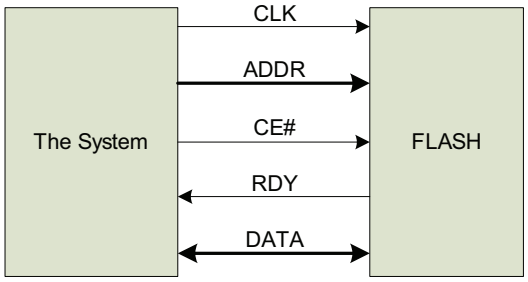
1 Introduction

Obtaining the maximum performance from Flash devices requires a clear understanding of their AC characteristics. AC characteristics define the bus cycle timing of the Flash. This application note provides a basic explanation of AC characteristics and clarifies some frequently misunderstood ones t_{OE}, t_{ACC}, t_{CE}, t_{PACC}, t_{IACC}, t_{BACC}, and t_{RDYS}.

2 The System and the Flash

Figure 1 shows a simplified block diagram of a Flash connected to the 'System'. The 'System' block represents all the non-Flash parts of the circuit. This includes the microprocessor, power supply, printed circuit board, and other components.

Figure 1. System and Flash Block Diagram



Flash data sheets are written from the point-of-view of the Flash and define two things:

1. What the Flash will provide to the System.
2. What the Flash requires of the System.

Figure 1 shows examples of the three types of Flash signals: Input (CLK), Output (RDY), and Bi-directional (DATA).

Input — The CLK, ADDR, and CE# are input signals to the Flash. For an input signal, the data sheet defines what the Flash requires of the System.

Output — The RDY signal is an output from the Flash. For an output signal, the data sheet defines what the Flash will provide to the System.

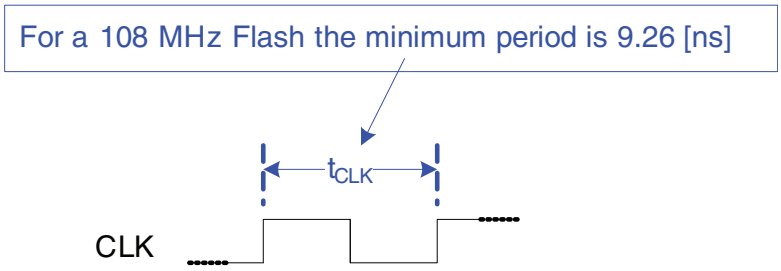
Bi-directional — The DATA signals are bi-directional. At times they are inputs to the Flash and at other times they are outputs. For bi-directional signals, the data sheet defines what the Flash requires and provides in each of these modes respectively.

In the following sub-sections some simple examples of the AC characteristics for the CLK and RDY signals are discussed.

2.1 CLK – t_{CLK}

CLK is an input to Burst mode Flash devices. The t_{CLK} AC timing characteristic defines the time period requirements that the System must satisfy. For example, a 108 MHz S29WS256P has a minimum clock period t_{CLK} of 9.26 [ns]. See Figure 2. CLK has additional requirements such as the minimum high and low times and slew rate.

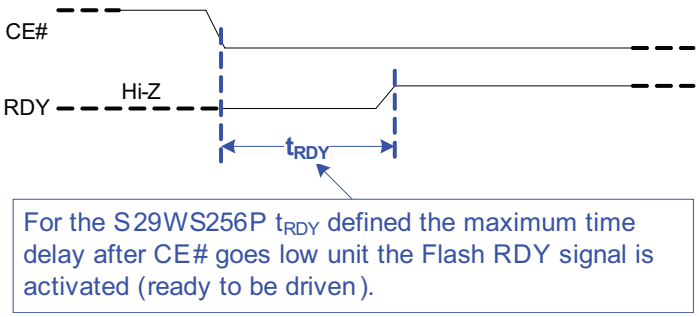
Figure 2. Minimum CLK Period



2.2 RDY – t_{RDY}

RDY is a Flash output. See Figure 3. For the S29WS-P family t_{RDY} defines the maximum delay in from the fall of CE# until the Flash has activated its RDY output. When the RDY output is activated the Flash is ready to drive it. This does not mean that the RDY output is driven high, or low, or Hi-Z. It only means that at this time the Flash can drive it. The System designer must wait until the RDY signal is activated before he can assume the Flash has control over it. Note that the t_{RDY} characteristic applies in both asynchronous and synchronous mode.

Figure 3. Asynchronous Mode t_{RDY}



3 Asynchronous Read – AC Characteristic

The following sub-sections discuss some asynchronous mode AC characteristics. Asynchronous mode does not use the CLK signal in defining bus cycle timing.

3.1 t_{ACC}, t_{OE}, and t_{CE}

The AC characteristics t_{ACC}, t_{OE}, and t_{CE} are used in asynchronous reads. The time when valid read data can first be expected is determined by the satisfaction of all of the AC characteristics involved in an asynchronous read bus cycle.

The following defines t_{ACC}, t_{OE}, and t_{CE}.

t_{ACC} — The memory access time from stable address to data output valid provided that all other relevant AC timing characteristics are satisfied.

t_{OE} —The data buffer output delay from OE# low to data output valid provided that all other relevant AC timing characteristics are satisfied.

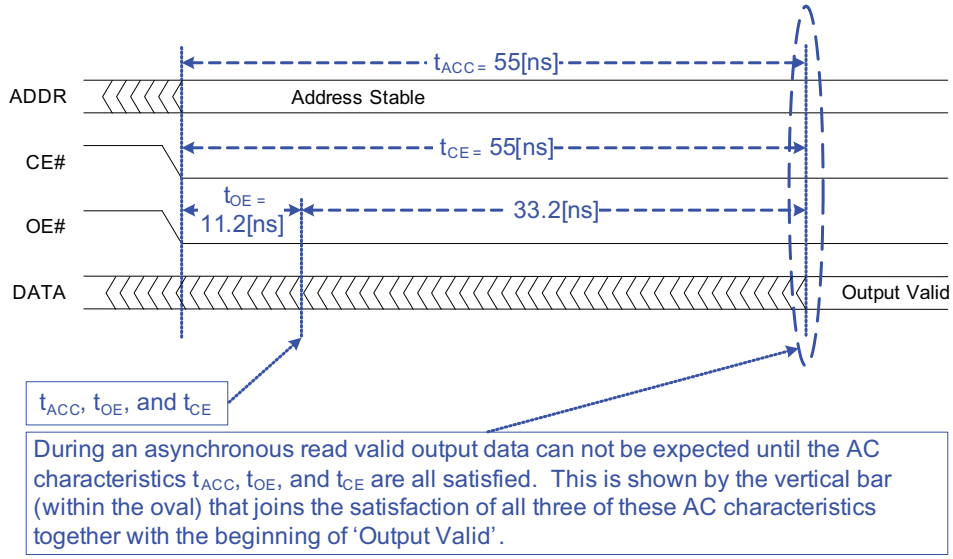
t_{CE} — The memory access time from CE# low to data output valid provided that all other relevant AC timing characteristics are satisfied.

It is a common misunderstanding that output read data should be valid after the t_{OE} time period without satisfying the other AC characteristic like t_{ACC} and t_{CE}.

Figure 4 shows a simplified S29WS128J asynchronous read bus cycle. Only t_{ACC}, t_{OE}, and t_{CE} are considered. In this example all three of the following things happen at the same time:

- Address becomes stable.
- CE# goes low.
- OE# goes low.

Figure 4. S29WS128J Asynchronous Read Timing

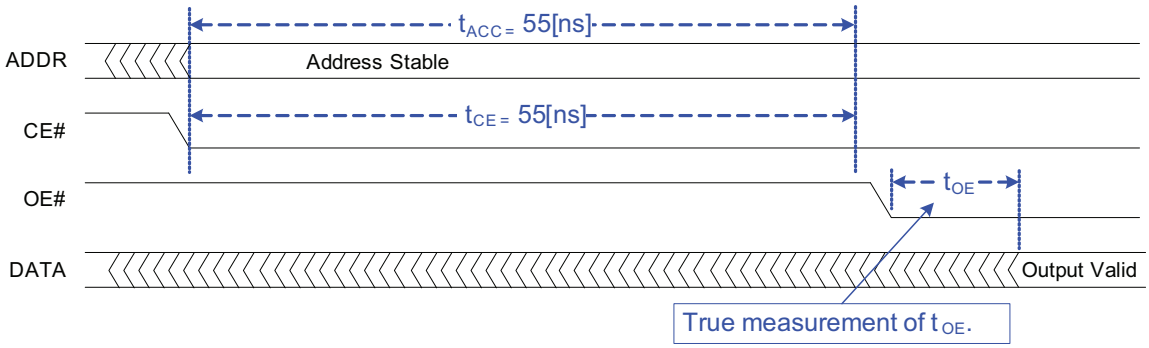


In Figure 4 valid read data can not be expected by 11.2 [ns] after OE# goes low. The output data will not be assured valid until 55 [ns] after CE# and OE# both go low. This is because t_{ACC} and t_{CE} must also be satisfied. The blue oval around the vertical bar emphasizes that all three AC characteristics must be satisfied before valid read data can be expected. Even if OE# went low as much as 43.8 [ns] after CE# went low it still would not make the read data become valid any earlier.

To measurement t_{OE} both t_{ACC} and t_{CE} should both be satisfied before OE# is brought low as shown in Figure 5.

Note that Figure 5 does not mean that it will always take 66.2 [ns] (55+11.2) to access memory. Only if the ADDR, CE#, and OE# signals are changed as show in Figure 5 will this be so. As shown in Figure 4, reads can be faster.

Figure 5. True Measurement of t_{OE}

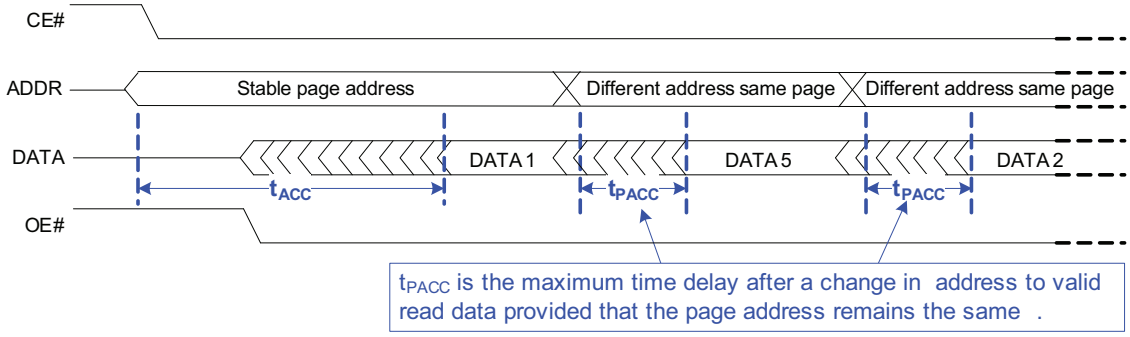


3.2 Page Mode Initial Read Access Time – t_{ACC}

Page mode devices have the main memory divided into pages. This allows for faster data read because all of the addresses of a given page can be read in the same bus cycle just by changing the address bits as shown in Figure 6.

However, the first read of data (DATA 1) from a given page is slower when compared to the following ones (DATA 5, and DATA 2). This is because the first read must allow for the initial read access time, t_{ACC}, which takes longer than the same page read access time, t_{PACC}. Note that page mode bus cycles must still allow for all the other AC timing characteristics too. Burst mode devices use t_{ACC} when they are in asynchronous mode.

Figure 6. Page Mode Asynchronous Read Bus Cycle – t_{ACC} and t_{PACC}



3.3 Same Page Read – t_{PACC}

The t_{PACC} characteristic is provided by Page mode devices like the S29GL128. For a Same Page Read, t_{PACC} defines the time from stable ADDR until valid data output. In Figure 6, three different memory addresses of the same page are read in random order. The first data DATA_1 is assured valid by the longer initial access time t_{ACC} while DATA_5 and DATA_2 will be valid by the shorter Page access time t_{PACC}.

So long as the read bus cycle is not terminated, other addresses in the memory page can be read randomly. Reading addresses from a different page will terminate the current page read bus cycle and t_{ACC} is required to read data.

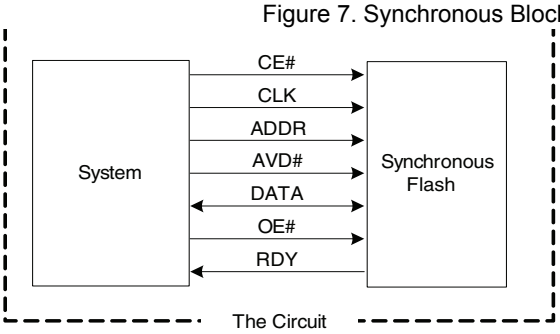
For an address to remain on the same page only the lowest few address bits are allowed to change. The identity of these changeable address bits depends on the device page size and its mode (word or byte). For example, if the page size is 16 bytes and the device is in byte mode then the page address bits are A2, A1, A0, and A-1.

For more information on Page mode refer to the Cypress® Application Note, “Understanding Page mode Flash Memory Devices”.

3.4 Burst Mode Initial Read Access Time – t_{IACC}

Figure 7 shows a block diagram for a Synchronous Flash and the System. In synchronous bus cycles CLK is used to define bus timing.

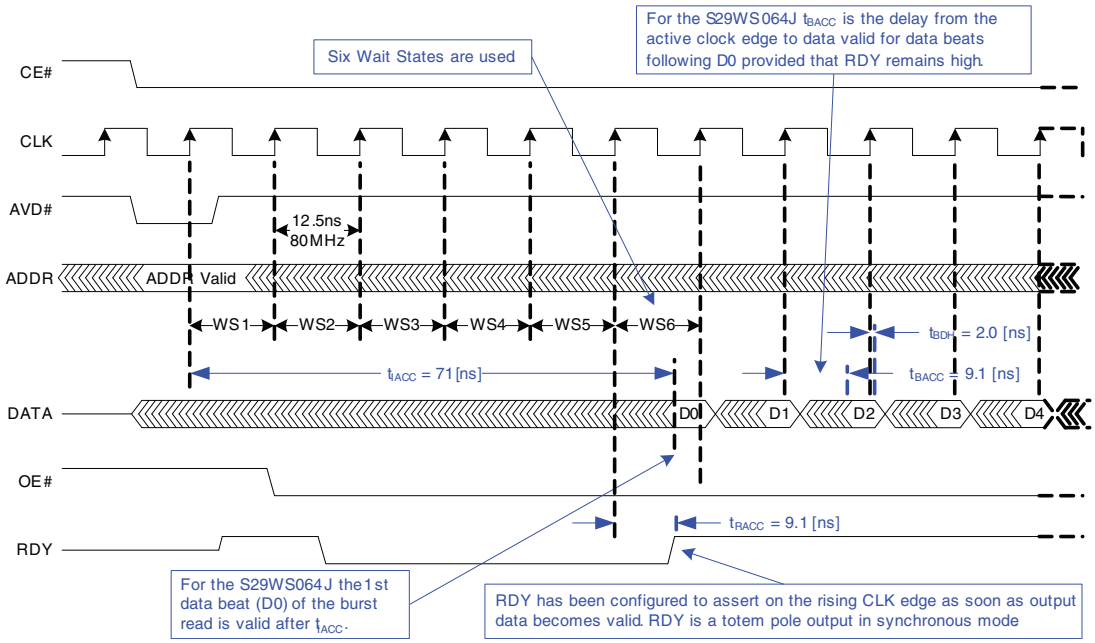
Figure 7. Synchronous Block Diagram



3.5 t_{IACC}

The t_{IACC} (not equal t_{ACC}) characteristic defines the time delay between the first active (rising) clock edge when CE# and AVD# are both low until the first data of a burst read, D0, is valid. A burst read bus cycle for an 80 MHz S29WS064J is shown in Figure 8.

Figure 8. S29WS064J Synchronous Burst Read Bus Cycle - t_{IACC}



Burst Read performance is increased by minimizing the number of wait states needed for the first read of data, D0. Every active clock edge from AVD# low until D0 is valid is another wait state. In Figure 8 the number of needed wait states is 6. D0 becomes valid during WS6.

Shown below is an equation for calculating the minimum number of wait states. The number of wait states is equal to the initial access time, t_{IACC}, divided by the clock period, t_{CLK}, and the result rounded up to the next whole number.

wait states = rounded up (t_{IACC} / t_{CLK})

Using t_{IACC} equals 71 [ns] and t_{CLK} equals 12.5[ns]:

wait states = rounded up (71 / 12.5)

wait states = rounded up (5.68)

wait states = 6

The System can have other time factors that could increase the number of wait states. For example, data setup time, propagation delays, and clock skew will add other time factors to the wait state calculation. In most cases their effect is to add to the delay when DO is valid at the System processor. For such factors their delays are grouped together under the label ‘other_time_factors’. The above equation is modified as follows:

wait states = rounded up { (t_{IACC} + other_time_factors) / t_{CLK} }

3.6 Burst Access Time – t_{BACC}

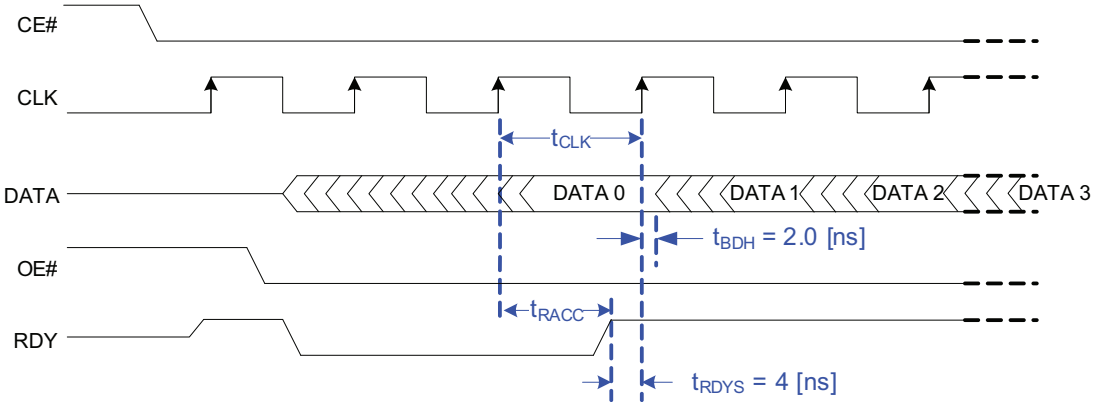
As shown in Figure 8 above, t_{BACC} defines the maximum time delay between the active clock edge and the next data beat provided that the Flash continues to assert RDY. The Flash uses the CLK signal to increment an internal address counter. In Figure 8 the Flash outputs the next sequential data beats D1, D2, and D3 after t_{BACC} time from the active edge of the CLK. The t_{BDH} characteristic is the minimum data hold time.

Note that the S29WS128J will pulse the RDY signal low and insert wait states when needed to handle the initial access delay and the crossing of internal memory boundaries. The System used the RDY signal to wait until the next burst data is valid.

3.7 t_{RDYS}

As shown in Figure 9, t_{RDYS} is the minimum amount of time the Flash will assert RDY before the next active clock edge. Figure 9 shows a waveform of with t_{RDYS} for a S29WS256 66 Mhz device with a clock of 66 MHz.

Figure 9. Synchronous Burst Read Bus Cycle - tRDYS



This minimum time for t_{RDYS} is defined by taking the minimum allowed clock period, t_{CLK}, and subtracting the maximum data RDY assertion time, t_{RACC}.

$t_{CLK} - t_{RACC} = t_{RDYS}$

or

$t_{RDYS} = t_{CLK} - t_{RACC}$

t_{RDYS} = 15.2 [ns] - 11.2 [ns] = 4 [ns]

For more information on Synchronous mode refer to the Cypress Application Note, “Understanding Burst mode NOR Flash Devices”.

4 Additional Delays

The System contains sources of delay other than just the active devices like trace delays, and load capacitance, and more. The effects of these sources must be accounted for in bus cycle timing.

5 Things to Remember

All of the involved AC timing characteristics must be satisfied.

All sources of delay must be considered in bus cycle timing.

The System must be able to handle a transition of a Flash signal at anytime within the signal's minimum and maximum transition times.

Document History Page

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*A	4958611	MSWI	10/12/2015	Updated in Cypress template
*B	5822956	AESATMP8	07/18/2017	Updated logo and Copyright.

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