Simultaneous Read/Write versus Erase Suspend/Resume

About this document

Scope and purpose

This application note discusses the considerations of using the Simultaneous Read/Write and Suspend/Resume features on flash devices.

Table of contents

1 Introduction

By their nature some operations on flash memory take a relatively long time. A typical Write Buffer Program operation takes 400 µs. A typical Sector Erase operation takes 180 ms to 800 ms, depending on the flash family. During one of these embedded operations, reads from the flash return status information. Many systems require access to read data stored in the flash memory before these operations complete. Infineon offers two flash features to solve this problem: Simultaneous Read/Write and Suspend/Resume. Simultaneous Read/Write devices are designed to allow reading from a flash device at the same time an embedded erase (or program) operation is being executed. The Erase Suspend/Resume and Program Suspend/Resume features allow the user to interrupt an embedded (erase or program) operation in order to read data from the flash device. The application designer will need to take several performance factors into account when deciding which of these methods is correct for the application.

2 Simultaneous Read/Write versus Suspend/Resume Flash Features

Flash devices with the Simultaneous Read/Write feature consist of several independent banks. Each bank encompasses many sectors. One of these devices with an active erase or program operation will only report status for reads from the same bank. Data from other banks are available for reading immediately, regardless of the embedded operation in progress. This design requires a careful division of the flash memory between banks used for code storage and banks used for data storage. The Suspend/Resume feature usually still exists in these multi-bank devices. However, it is only useful when reading data from the same bank where an embedded operation is ongoing.

Single bank devices have a simpler implementation. Because there is only one bank in the whole device, there is no Simultaneous Read/Write feature available. The Suspend/Resume feature must be used to read array data out of the flash during an embedded operation. This allows the application to read data that is anywhere in the device as long as it is not in the sector being erased or programmed. But there is a latency between issuing the suspend operation and when the flash is ready for reading array data. For example, the S29GL01GS has Erase Suspend Latency (t_{ESL}) defined in the device data sheet as 40 µs, as of this writing. Please consult the data sheet for the most up-to-date information.

3 Simultaneous Read/Write versus Suspend/Resume Timing

Most systems that use either the Simultaneous Read/Write feature or Suspend/Resume feature do so because of interrupt-driven events that could require access to the flash device during an erase or program. When the Suspend/Resume feature is used, the applicable interrupt service routines must be designed to consider the maximum suspend latency. This latency is not an issue when using a Simultaneous Read/Write device.

When the Suspend/Resume feature is used to handle an interrupt, the erase or program operation is paused while reading takes place. This serial sequence can significantly increase the total time of the erase operation (see **Figure 1** for details). Erase operations take longer than programs, so they are the main concern for system latency, and are the focus of our examples here.

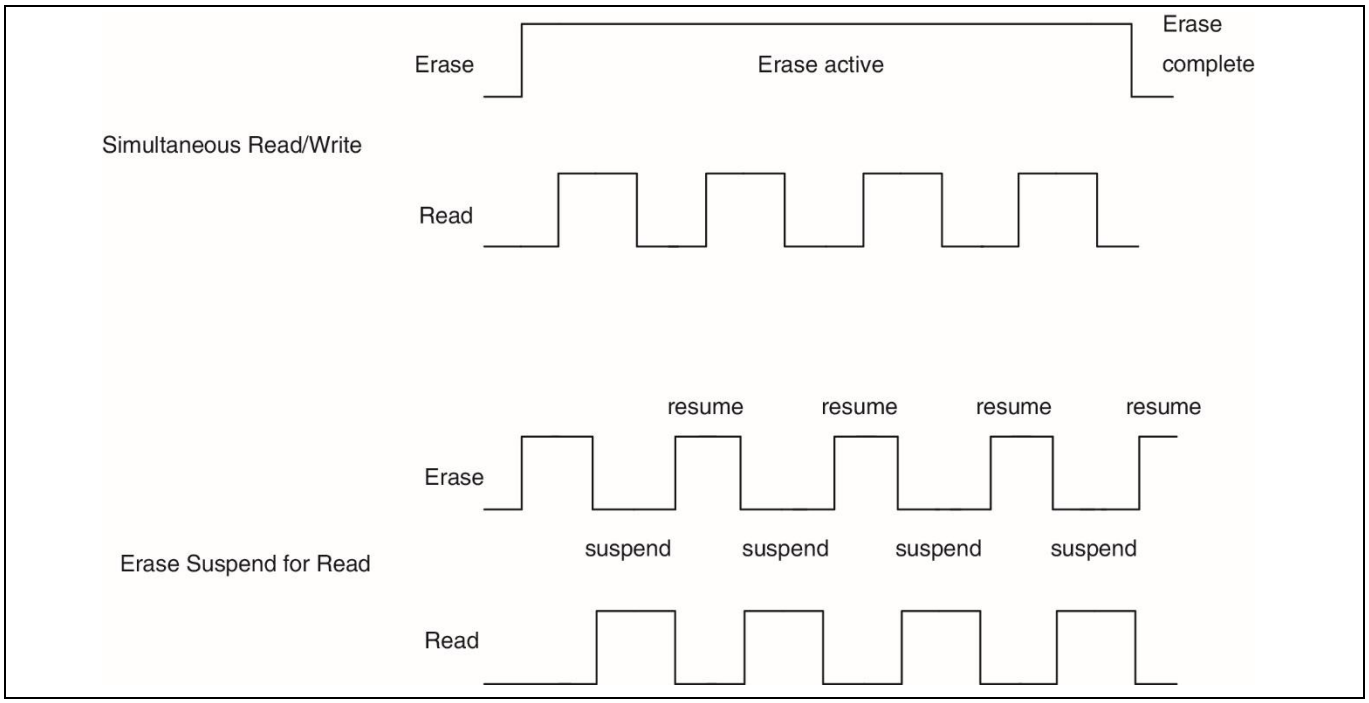

Figure 1 Simultaneous Read/Write vs. Erase Suspend/Resume Timing

4 Simultaneous Read/Write versus Erase Suspend/Resume Performance

As the number of Erase Suspend/Resume cycles increases, the sector erase operation becomes less efficient. During an erase, the flash device issues a number of erase pulses to the memory array. The completion of a given erase pulse is required in order to progress to the next erase pulse. When an erase is suspended, any erase pulse that was not complete must be restarted (see **Figure 2**). Thus, if Erase Suspend/Resume commands are issued in rapid succession, the device will restart many of the erase pulses. This will greatly degrade the performance of the erase function, and possibly extend the total erase time beyond the specified maximum value. Each device requires a minimum time between the beginning of an erase (or resume) command and the suspend command. Please consult the device data sheet for the required delay between resume and suspend. Another solution is to use flash with the Simultaneous Read/Write feature instead of Suspend/Resume.

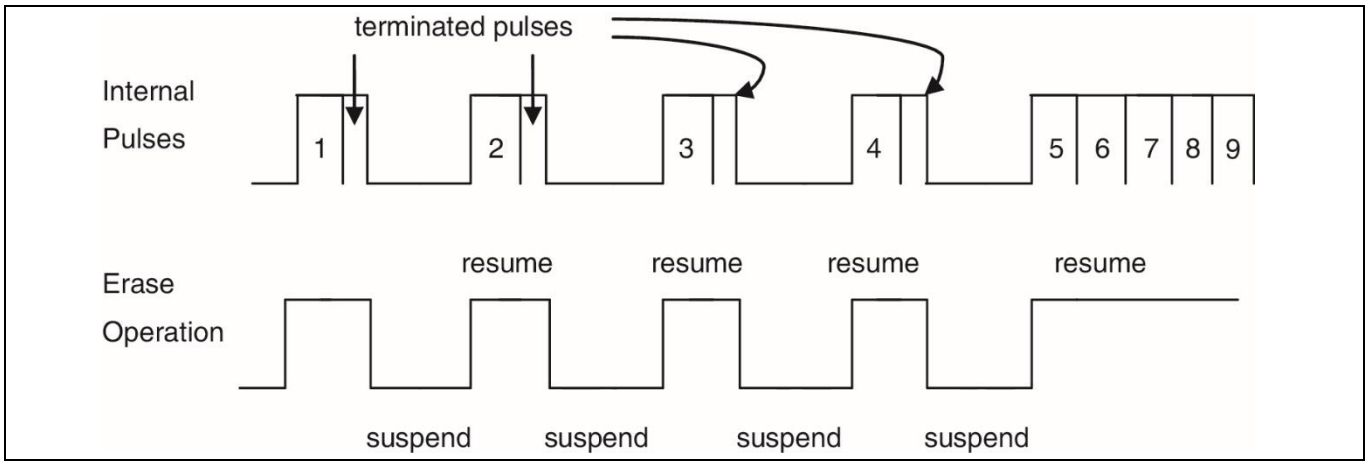

Figure 2 Incomplete Internal Erase Pulses Get Restarted

5 How Often Can an Erase be Suspended?

Erase operations can be suspended any number of times on MirrorBit™ technology flash. However, these devices still require complete erase pulses for progress on an erase operation.

6 Conclusion

For systems that need to suspend embedded operations occasionally, such as interrupt-driven controllers or computer systems, the Suspend/Resume feature provides for adequate overall performance. But if a system is real-time and will frequently need to read from the device, or must have immediate access to flash contents, a flash device with the Simultaneous Read/Write feature could achieve optimal erase performance and minimum read latencies.

Characteristic	Simultaneous Read/Write	Suspend/Resume with multi-bank Flash	Suspend/Resume with single-bank Flash
Location for Flash Array Reads	Any sector in a different bank	Different sector in same bank	Any other sector
Read Latency	None	See data sheet, typically 20-40 µsec	See data sheet, typically 20-40 µsec
Performance Impact	None	Embedded operation completion delayed. Application impact varies by application	Embedded operation completion delayed. Application impact varies by application
Chip Complexity	Complex	Complex	Simple

Revision history

Document version	Date of release	Description of changes
**	2004-07-06 to 2011-07-25	Initial version Changed “Read/Write Operation” to “Read/Write Feature”. Replaced “Flash” with “Flash devices”. Changed “Erase Suspend/Resume Operation” to “Erase/Suspend Resume feature”. In Simultaneous Read/Write vs. Erase Suspend/Resume Performance section: Deleted paragraph number two (“The required length...”) added first sentence to paragraph number one “Regardless of the type”. Paragraph 2 - Deleted “(10ms between the beginning of an erase (or resume) command and the suspend command, or to use the Simultaneous Read/Write feature for the Erase Suspend/Resume latency)” and added (10ms erase pulses)”. Updated last paragraph for language consistency. Erase Time Multiple vs. Frequency of Erase Suspends: Updated horizontal axis of drawing for accuracy. In How Often Can an Erase be Suspended? section: Updated paragraph for language consistency. Changed “MirrorBit Devices” to “Devices based on MirrorBit™ technology”. Changed “BDD” to Am29BDD”. Deleted “(assuming the number of suspends is limited to under 5,980)” and added “(assuming this erase command is limited to under 5,980 suspends)”. In Conclusion: Updated paragraph for language consistency. Updated to new format. Complete rewrite. In Simultaneous Read/Write versus Erase Suspend/Resume Performance: Updated paragraph.
*A	2015-10-22	Updated to template.
*B	2018-06-13	Updated to new template. Completing Sunset Review.
*C	2021-04-22	Updated to Infineon template.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-04-22
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Go to www.cypress.com/support

Document reference
001-99127 Rev. *C

IMPORTANT NOTICE
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.