Reset voltage and timing requirements for MIRRORBIT™ Flash

About this document

Scope and purpose

AN99123 describes the considerations of reset control signal timing when using MIRRORBIT™ NOR flash devices in an application.

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1 Synopsis

MIRRORBIT™ NOR flash has several unique reset control signal timing requirements. Timing requirements vary by MIRRORBIT™ processes and families. System designers must accommodate these requirements for reliable operation.

2 Applicable device families

- 90 nm MIRRORBIT™ process: S29GLxxxP, S29WSxxxP
- 65 nm MIRRORBIT™ process: S29VS/XSxxxR
- 65 nm MIRRORBIT™ process: S29GLxxxS (≤ 1 GBit), S70GL02GS
- 45 nm MIRRORBIT™ process: S29GLxxxT (≤ 1 GBit), S70GL02GT

3 Parameters of interest

VLKO	Low VCC lock-out voltage
t_{VCS}	$V_{CC} > V_{CC-MIN}$ setup requirement prior to RESET# negation or CE# assertion
t_{VIOS}	$V_{IO} > V_{IO-MIN}$ setup requirement prior to RESET# negation or CE# assertion
t_{RP}	RESET# pulse width (assertion period)
t_{RH}	RESET# high requirement prior to CE# assertion
t_{READY}	Period from RESET# assertion to RY/BY# negation
t_{RB}	PERIOD from RY/BY# negation to CE# assertion

4 Reset requirements – 90 nm process node products

Reset conditions are required for the 90 nm MIRRORBIT™ devices because of circuit changes implemented to reduce die size and to improve endurance of Advanced Sector Protection PPB bits. The power-on-reset and warm reset requirements for these new device families are reviewed in this section.

4.1 Power-on-reset requirements

During Power-On, V_{CC} should rise monotonically and must remain greater than V_{LKO} during all reset operations. V_{IO} can either be tied to V_{CC} or can be driven to a different voltage level. In the latter case, V_{IO} must exceed V_{IO_MIN} before RESET# is negated and must be maintained between V_{IO_MIN} and V_{CC} +100 mV.

During V_{CC} ramp-up, RESET# must be asserted (low). From the time when V_{CC} exceeds V_{CC_MIN}, RESET# must remain asserted for a period of t_{VCS}) prior to negation (see **Figure 1**). Control signal transitions can be initiated t_{RH} following RESET# negation.

4.1.1 Power-on-reset timing

Table 1 90 nm process node products - power-on-reset timing

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{VCS}	V_{CC} setup time to CE# assertion (min)	30 µs	35 µs
t_{VIOS}	V_{IO} setup time to CE# assertion (min)	30 µs	35 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

Note:

1. *For S29WSxxxP, V_{CC} ramp rate must exceed 1V/400 µs otherwise a hardware reset would be required.*
2. *For S29WSxxxP, VIO pin is named $V_{CC}Q$.*
3. *V_{CC} and V_{IO} (resp. $V_{CC}Q$) must be ramped up simultaneously for proper power-up.*
4. *If RESET# is not stable for t_{VCS} or t_{VIOS}: The device does not permit any read and write operations, a valid read operation returns FFh and a hardware reset is required.*

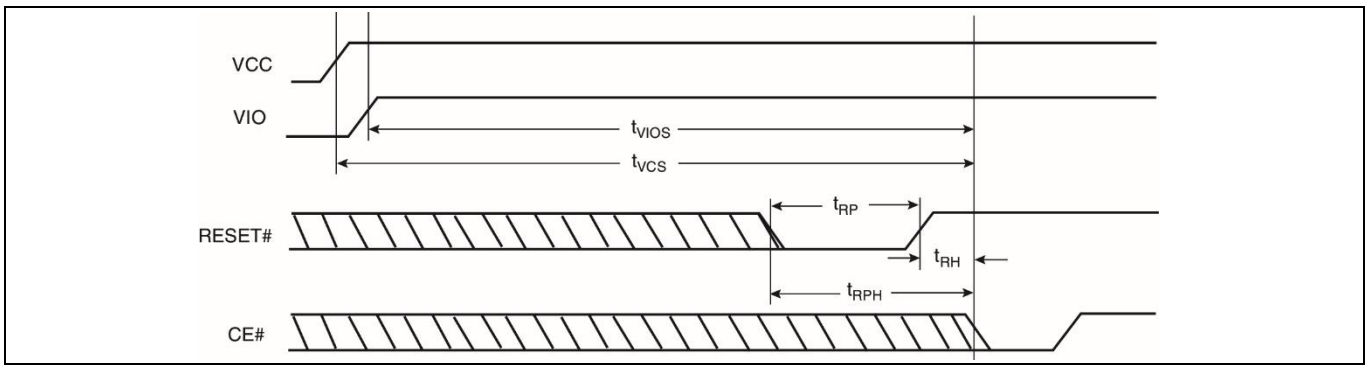

Figure 1 90 nm process node products- power-on reset timing

4.2 Warm-reset requirements

Warm-reset, also known as hard reset, requires RESET# to pulse from high to low to high. timing requirements vary by the state of the device prior to RESET# assertion, specifically whether or not the device is performing an embedded operation (program or erase operation in progress).

During warm-reset operations, V_{CC} must be maintained greater than V_{LKO}.

4.2.1 Warm-reset timing while embedded operation not in progress

In the event of the warm-reset being initiated when an embedded operation is not in progress (see **Figure 2**), the internal reset operation requires t_{RP} to be completed. Control signal transitions can be initiated t_{RH} following internal reset operation completion. RY/BY# will stay in the ready state as the device operates during non-embedded operations.

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

Table 2 90 nm process node products - warm reset timing - embedded operation not in progress

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{RP}	RESET# pulse width (min)	30 µs	35 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

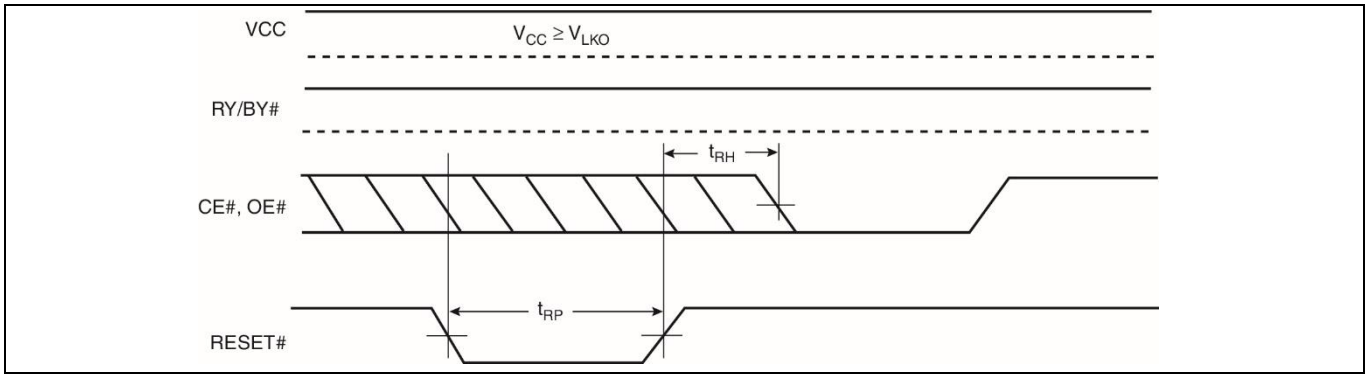

Figure 2 90 nm process node products– warm reset timing – embedded operation not in progress

4.2.2 Warm-reset timing while embedded operation in progress

In the event of the warm-reset being initiated when an embedded operation is in progress (see **Figure 3**), the internal reset operation requires t_{READY} to be completed. t_{READY} is comprised of the time required to gracefully exit an embedded programming operation, followed by the standard internal reset operation and the set-up time from reset operation completion until a control signal transition detection can be guaranteed.

The complete reset operation is triggered by the falling edge of RESET#. RESET# must remain asserted for a period of t_{RP}. Control signals transition can be initiated by t_{READY} after the falling edge of RESET#.

Table 3 90 nm process node products - warm reset timing - embedded operation in progress

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{READY}	RESET# assertion to RY/BY# negation (min)	30.2 µs	35.2 µs
t_{RB}	RY/BY# high to CE# assertion (min)	0 ns	0 ns
t_{RP}	RESET# Pulse Width (min)	30 µs	35 µs

Reset requirements – 90 nm process node products

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

Note:

1. *For S29WSxxxP and S29GLxxxP, $t_{READY} = t_{RP} + t_{RH}$. No additional waiting time is required.*

A typical implementation would have RESET# asserted a period of t_{READY} with a short delay from RESET# negation before asserting CE# and initiating a read operation.

An alternate implementation is asserting RESET# for a shorter period of t_{RP} and employing a delay loop to prevent flash control signal accesses for t_{READY} from the assertion of RESET#.

An additional option is to monitor RY/BY# following the rising edge of a RESET# pulse at least t_{RP} in duration. When RY/BY# is detected high, control signal transitions can be initiated.

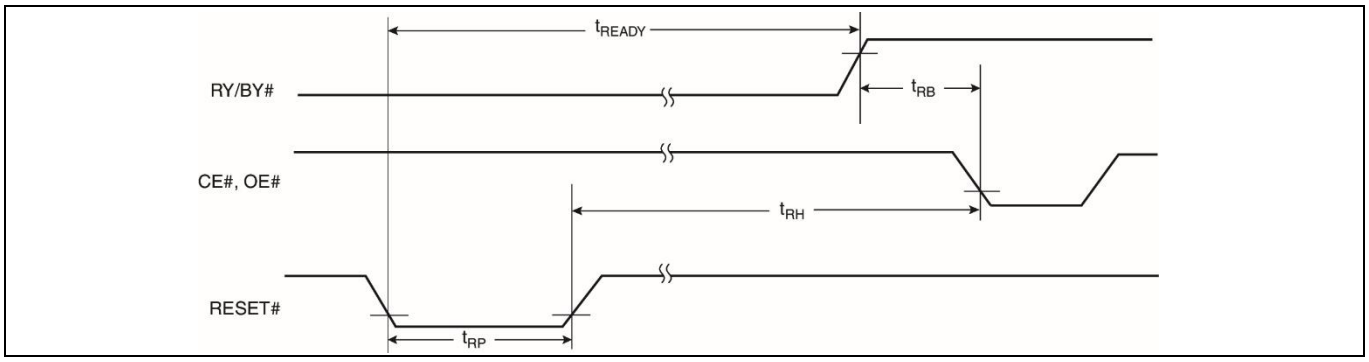

Figure 3 90 nm Process node products - warm reset timing – embedded operation in progress

5 Reset requirements - 65 nm process node products

Reset conditions are required for the 65 nm MIRRORBIT™ devices because of circuit changes implemented to reduce die size. The power-on-reset and warm reset requirements for these new device families are reviewed in this section.

5.1 Power-on-reset requirements

During Power-On, the V_{CC} and V_{IO} ramp rate could be non-linear. However, V_{CC} and V_{IO} must remain greater than V_{LKO} during all reset operations. It is also recommended to ramp up those two signals simultaneously.

5.1.1 Power-on-reset timing

Table 4 65 nm process node products - power-on-reset timing

Parameter	Description	S29VS/XSxxxR
t_{VCS}	V_{CC} setup time to CE# assertion (min)	300 µs
t_{VIOS}	V_{IO} setup time to CE# assertion (min)	300 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns
t_{RP}	RESET# Pulse Width (min)	50 ns
t_{RPH}	RESET# Low to CE# Low (min)	10 µs

Note:

1. *V_{CC} and V_{IO} ramp rate could be non-linear.*
2. *RESET# must be high after V_{CC} and V_{IO} are higher than V_{CC} minimum.*
3. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*

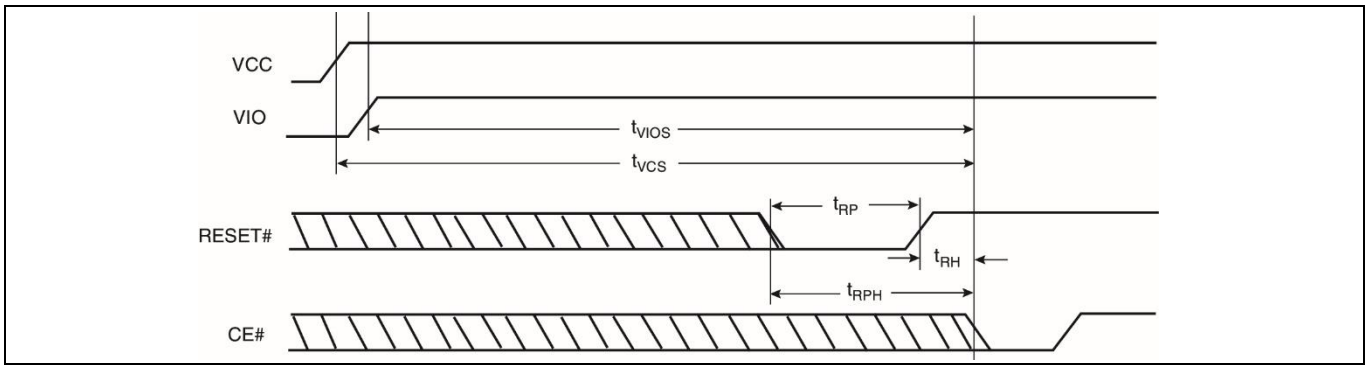

Figure 4 65 nm process node products - power-on reset timing

5.2 Warm-reset requirements

Warm-reset, also known as hard reset, requires RESET# to pulse from high to low to high. Starting from the 65 nm MIRRORBIT™ products, the warm reset timing requirements will be totally independent from the state of the device prior to RESET# assertion, namely whether an embedded operation was in progress or not.

During warm-reset operations, V_{CC} must be maintained greater than V_{LKO}.

During warm-reset (see **Figure 5**), the internal reset operation requires t_{RP} to be completed. Control signal transitions may be initiated t_{RH} following RESET# negation.

5.2.1 Warm-reset timing

Table 5 65 nm process node products - warm reset timing

Parameter	Description	S29VS/XSxxxR
t_{RPH}	RESET# low to CE# Low (min)	10 µs
t_{RP}	RESET# pulse width (min)	50 ns
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns

Note:

1. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
2. *CE#, OE# and WE# must be at logic high during Reset Time.*

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

An equally effective and alternate implementation for the 65 nm MIRRORBIT™ devices is asserting RESET# for a short period followed by a long delay to allow the completion of the internal reset operation prior to initiating control signal transitions.

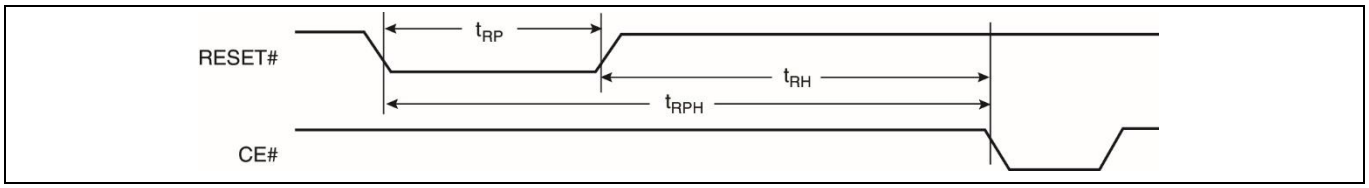

Figure 5 65 nm process node products – warm reset timing

6 Reset requirements - 65 nm/45 nm MIRRORBIT™ products

Reset conditions are required for the 65 nm and 45 nm MIRRORBIT™ devices because of circuit changes implemented to reduce die size. The power-on-reset and warm reset requirements for these new device families are reviewed in this section.

6.1 Power-on-reset Requirements

During power-on, V_{CC} and V_{IO} ramp rate could be non-linear. However, V_{CC} and V_{IO} must remain greater than V_{LKO} during all reset operations. It is also recommended to ramp up those two signals simultaneously.

6.1.1 Power-up sequencing

V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$). V_{IO} must track the rise and fall of V_{CC} within 200 mV ($V_{IO} \geq V_{CC}$ - 200 mV) when V_{IO} is below the V_{IO} minimum.

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above, the minimum V_{CC} and V_{IO} thresholds. During t_{VCS} the device is performing power on reset operations.

Table 6 65 nm/45 nm MIRRORBIT™ products - power-up timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{VCS}	V_{CC} setup time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{VIOS}	V_{IO} setup time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs

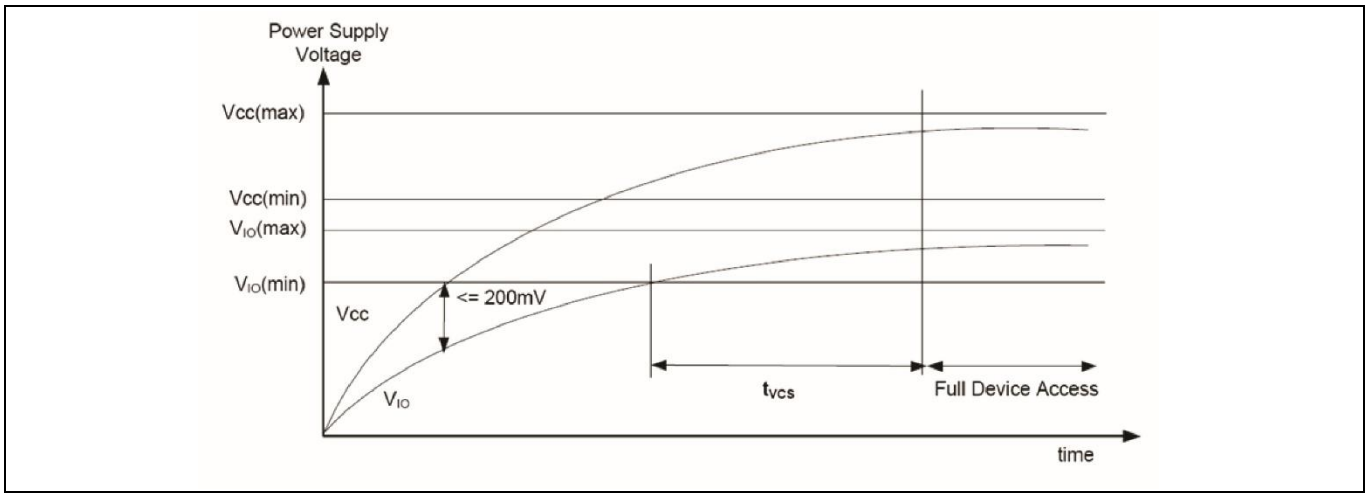

Figure 6 65 nm/45 nm MIRRORBIT™ products - power-up timing

6.1.2 Power-on-reset timing

Table 7 65 nm/45 nm MIRRORBIT™ products - power-on-reset timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{VCS}	V_{CC} setup time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{VIOS}	V_{IO} setup time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{RH}	RESET# high prior to CE# assertion (min)	50 ns	50 ns	50 ns	50 ns
t_{RP}	RESET# pulse width (min)	200 ns	200 ns	200 ns	200 ns
t_{RPH}	RESET# low to CE# low (min)	35 µs	70 µs	35 µs	70 µs

Note:

1. *V_{CC} and V_{IO} ramp rate could be non-linear.*
2. *RESET# Low is optional during POR. If RESET# is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CE# may go Low. If RESET# remains low after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET# must also be high t_{RH} before CE# goes low.*
3. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
4. *RY/BY# pin is low during power-up.*

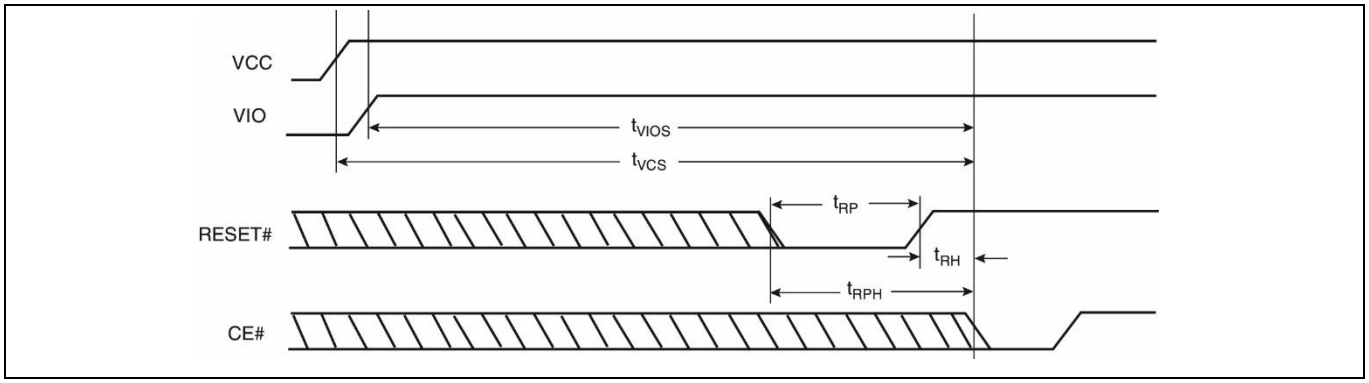

Figure 7 65 nm/45 nm MIRRORBIT™ products – power-on-reset timing

6.2 Warm-reset requirements

Warm-reset, also known as hard reset, requires RESET# to pulse from high to low to high. For the 65 nm and 45 nm MIRRORBIT™ products, the warm reset timing requirements will be also totally independent from the state of the device prior to RESET# assertion, namely whether an embedded operation was in progress or not.

During warm-reset operations, V_{CC} must be maintained greater than V_{LKO}.

During warm-reset (see **Figure 8**), the internal reset operation requires t_{RP} to be completed. Control signal transitions may be initiated t_{RH} following RESET# negation.

6.2.1 Warm-reset timing

Table 8 65 nm/45 nm MIRRORBIT™ products - warm reset timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{RPH}	RESET# low to CE# Low (min)	35 µs	70 µs	35 µs	70 µs
t_{RP}	RESET# pulse width (min)	200 ns	200 ns	200 ns	200 ns
t_{RH}	RESET# high prior to CE# assertion (min)	50 ns	50 ns	50 ns	50 ns

Note:

1. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
2. *CE#, OE# and WE# are recommended to be at logic high during Reset Time.*

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

An equally effective and alternate implementation for the 65 nm and 45 nm MIRRORBIT™ devices is asserting RESET# for a short period followed by a long delay to allow the completion of the internal reset operation prior to initiating control signal transitions.

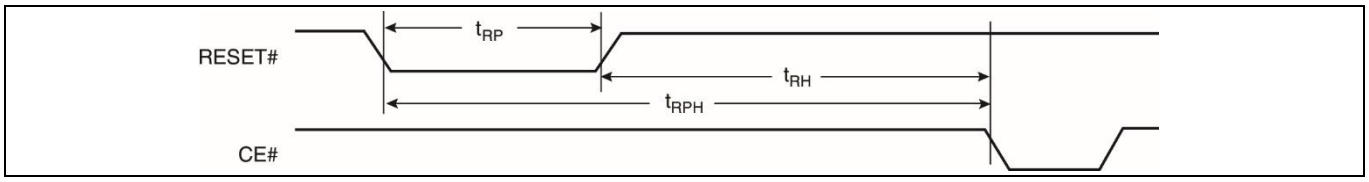

Figure 8 65 nm/45 nm MIRRORBIT™ products - warm reset timing

Revision history

Document version	Date of release	Description of changes
**	2006-11-14 to 2010-10-04	Initial version Updated document format Removed all references to AM29LVxxxM, MBM29PLxxxM, S29GLxxxM, S29PLxxxP and S29GLxxxA Added POR and Reset requirements for 90 nm, 65 nm and 65 nm Eclipse products
*A	2015-10-22	Updated in template
*B	2017-09-05	Updated logo and Copyright
*C	2018-10-17	Removed references to 110 nm products Removed references to S29NSxxxP, S29GLxxxR, S29WSxxxR and S29NSxxxR Updated with the 45nm products requirements
*D	2021-03-30	Updated to Infineon template
*E	2022-01-18	Updated to Infineon branding and style

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