MirrorBit Parallel NOR Flash Write Buffer Programming and Page Buffers

About this document

Scope and purpose

This application note explains MirrorBit™ Parallel NOR Flash Write Buffer Programming and Page Buffers.

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1 Introduction

The write buffer in MirrorBit Parallel NOR Flash memory devices is designed to reduce the overall system programming time when writing to the Flash device. The host system first fills the write buffer with data, and then issues the write buffer programming command. The flash device pro- grams the buffered data in parallel, and thus reduces the programming time compared to programming bytes or words one at a time. Depending on the device design, a write buffer can store up to 256 words (512 bytes) of data that can then be written using a single programming operation.

MirrorBit Parallel NOR Flash devices use a specific, additional set of commands to accomplish write buffer programming. Refer to the appropriate data sheet for the complete list of device commands.

The page buffer read function accelerates read operations for addresses within a specific range.

2 Write Buffers

2.1 Benefits of Using the Write Buffers

The main benefit is pure programming speed. Data can be written into the write buffers by conforming to the Write Cycle time timings parameter (t_{WC} = 60 ns). In addition, the write buffers program the Flash memory array in parallel (four words at a time), greatly decreasing the time needed to write to the Flash.

2.2 Write Buffer Operation

Write buffer programming is only available through the *Write to Buffer* and *Program Buffer to Flash* command sequences. The *Write-to-Buffer Abort Reset* command sequence is used to exit out of the Write-Buffer-Abort state. **Table 1** lists all software program sequences associated with the write buffer.

Table 1 Write Buffer Operation

Command Sequence	Interface	Bus Cycles											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Write to Buffer	Word	555	AA	2AA	55	SA	25	SA	WC (Note)	PA	PD	WBL (Note)	PD
	Byte	AAA		555									
Program Buffer to Flash (Confirm)	Both	SA	29										
Write-to-BufferAbort	Word	555	AA	2AA	55	XXX	F0						
	Byte	AAA		555									

Note: The sixth cycle must be repeated to complete the number of buffer writes specified by the WC in cycle four.

Legend

- PA = Program Address of the memory location to be programmed. This can be any address within the target write buffer page.
- PD = Program Data to be programmed at location PA.
- SA = Sector Address containing locations to be programmed. This can be any valid address within the sector.
- WC = Write Count is the number of write buffer locations to load minus one (to load 7 locations the WC would be 6).
- WBL = Write Buffer Location. The address must be within the same write buffer page (32-byte range located on a 32-byte boundary) as PA.

In **Table 2**, the host system first loads data at any location in the target write buffer page. Sub- sequent write buffer locations do not need to be loaded in any particular order as long as they reside in the same write buffer page and sector. A write buffer page, for a device with a 256-word write buffer (e.g.: S29GL-T), is defined as the address from xxx0h to xxFFh (any sequence of address where A_{MAX} – A_8 do not change).

Note: The internal write counter decrements for every data load operation, not for each unique write buffer address location. If the same write buffer location is loaded multiple times, the internal write counter will decrement after each load operation. The last data loaded into a given write-

buffer location will be programmed into the device after the Program Buffer to Flash command. The host system must therefore account for the effects of loading a write-buffer lo- cation more than once.

When the Write to Buffer command programming sequence has been completed, the Program Buffer to Flash command must be issued to move the data from the write-buffer into the flash memory array.

2.3 Write Buffer Programming Abort

As stated earlier, write buffer programming cannot be performed across multiple write buffer pages or across multiple sectors. If this is attempted, the write buffer programming operation will be automatically aborted. The abort condition is detected by performing a polling read operation, in which the data shows DQ1 = 1, DQ7 = DATA# (for the “Last Loaded Address”), DQ6 = TOGGLE, DQ5=0, or Status Register read operation, in which bit 3 (WBASB) of the status register is cleared to 1.

The write buffer programming sequence aborts in the following cases:

- Loading a value that is greater than the write buffer size (write-buffer-page) during the “fourth cycle (WC) Numbers of Locations to Program” step.
- Writing to an address in a sector that is different than the one specified during the Write-Buffer-Load command.
- Writing an Address/Data pair to a different write buffer page than the one selected by the starting address during the “write buffer data loading” stage of the operation.
- Writing data other than the Program Buffer to Flash command after loading the specified number of write buffer locations.

Note: The Write-to-Buffer Abort Reset command sequence must be written to the device to return to READ mode.

3 Page Buffer Read Introduction

Whenever the host system changes a “page address” (or toggles CE# during a read), the device performs a “random access”. During this “random access” the read page buffer is loaded in parallel with data within the selected read-page boundaries. Subsequent intra-page accesses are 3 to 4 times faster than random accesses because the data are already available in the buffer.

Therefore, read performance is significantly improved.

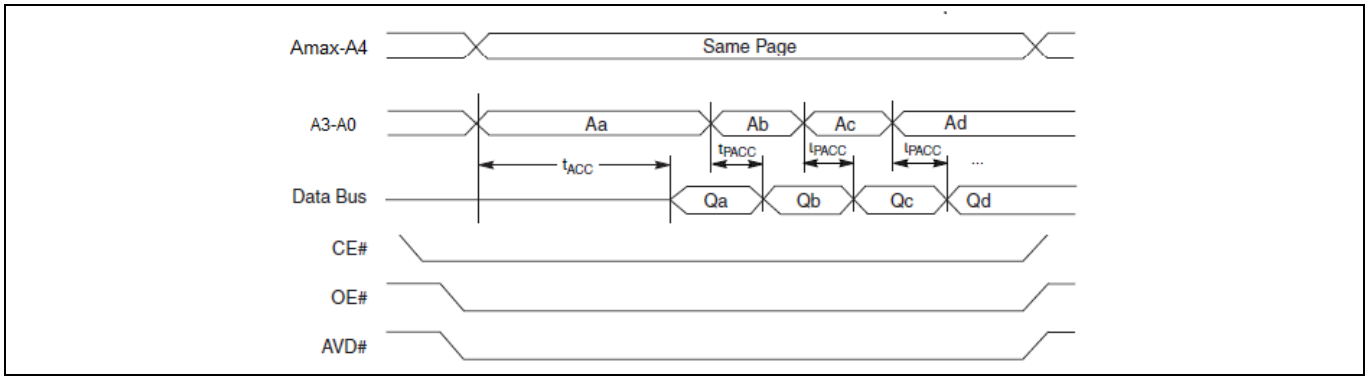


Figure 1 Page Buffer Read Timing Diagram

*Note: **Figure 1** shows device in word mode. Addresses A3–A(-1) are used during byte mode.*

3.1 Read Buffer Operation with a 16-word Page Buffer

Most Infineon page mode flash devices use a 16-word (32-byte) page buffer. For page buffer read operation, the user must issue a read address, or “RA”, for any memory location. During the initial access time (t_{CE}/t_{ACC}) a page of 16 words (32 bytes), starting from a 32-byte boundary, is read into the page buffer. If the device is in word mode, address bits A3 to A0 can then be used to access any of the 16 words within the page with a reduced page access time (t_{PACC}). If the device is in byte mode in a x8/x16 device, A3 through A-1 can be used to access any of the 32 bytes in the page. If the device is a x8-only device, A4 through A0 can be used to access any of the 32 bytes within the page.

The appropriate page is selected by the higher address bits: $A_{(MAX)}$-A_4 for x16-only and x8/x16 devices, and $A_{(MAX)}$-A_5 for x8-only devices. Fast page mode accesses are obtained by keeping the high-order “read page address” bits constant and changing the “intra-read page” address bits: A0 to A3 for x16-only and x8/x16 in word mode; A-1 to A3 for x8/x16 in byte mode; and A0 to A4 for x8-only. This is an asynchronous operation with the host system supplying the specific byte or word location.

Table 2 shows the command sequence definition for read accesses.

Table 2 Read Access

Command Sequence	Interface	Bus Cycles									
		First		Second		Third		Fourth		Fifth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	Both	RA	RD	RA	RD	RA	RD	RA	RD	Note	Note

Note: For reading bytes, eight consecutive memory locations can be read, compared to four memory locations for reading words. “Intra-read page” locations can be accessed in any order.

Legend

- RA = Read Address
- RD = Read Data
- A depiction of the device bus operation for read accesses is shown in **Table 3**.

Table 3 Device Bus Operation for Read Access

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Address	Data
Read	L	L	H	H	X	AIN	DOUT

During page buffer read operations, the CE# pin must be kept at voltage level V_{IL} during all fast page mode accesses. If the CE# pin toggles or changes state during a page buffer read operation, the current data transfer will automatically be aborted and another initial page access is started. This will result in an unnecessary delay in read timings.

3.2 Read Buffer Operation in S29GL-T Devices

The S29GL-T family of devices uses a 16-word (32-byte) page buffer. If the device is in word mode address bits A3–A0 can be used to access any of the 16 words within the page with a reduced page access time (t_{PACC}). Hardware and software that was designed to work with 8-word page buffers will work just as well on devices with a 16-word page buffer without any changes.

4 Write Buffer Programming in S29GL-T Devices

In S29GL-T devices, write buffer programming with program and erase suspend/resume functionality allows the system to write to a maximum of 256 words in one programming operation. This provides increased programming performance up to 64 times faster than word programming. **Table 4** lists the programming steps. Please refer to the appropriate data sheet for a review of the full write buffer operation.

Table 4 Write Buffer Programming Procedure in PL-N Devices

Cycle#	Description	Address	Data	Comment
1	Unlock	Base + 555h	00AAh	
2	Unlock	Base + 2AAh	0055h	
3	Write Buffer Load Command	Program Address	0025h	AMAX to A16 is latched in this command cycle and must not change in subsequent cycles
4	Write Word Count	Program Address	Word Count (N-1)h	
5	Load Buffer Word N	Program Address, Word N	Word N	AMAX to A8 is latched in this command cycle and must not change in subsequent command cycles

Note: For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.

The following is an example of write buffer programming Command:

```
/* Example: Write Buffer Programming Command */
/* NOTES: Write buffer programming limited to 256 words. */
/* All addresses to be written to the flash in */
/* one operation must be within the same flash */
/* page. A flash page begins at addresses */
/* evenly divisible by 0x100. */
UINT16 *src = source_of_data;                    /* address of source data      */
volatile UINT16 *dst = destination_of_data;      /* flash destination address   */
int wc = words_to_program-1;                     /* word count (minus 1)        */
*( (volatile UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1        */
*( (volatile UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2        */
*( (volatile UINT16 *)sector_address ) = 0x0025; /* write buffer load command */
*( (volatile UINT16 *)sector_address ) = wc;     /* write word count (minus 1)  */
while (wc >= 0)    /* ALL dst MUST BE SAME PAGE */
{
  *dst = *src;    /* write source data to destination */
  dst++;          /* increment destination pointer    */
  src++;          /* increment source pointer         */
  wc--;           /* decrement word count             */
}
*( (volatile UINT16 *)sector_address ) = 0x0029; /* write confirm command */
```

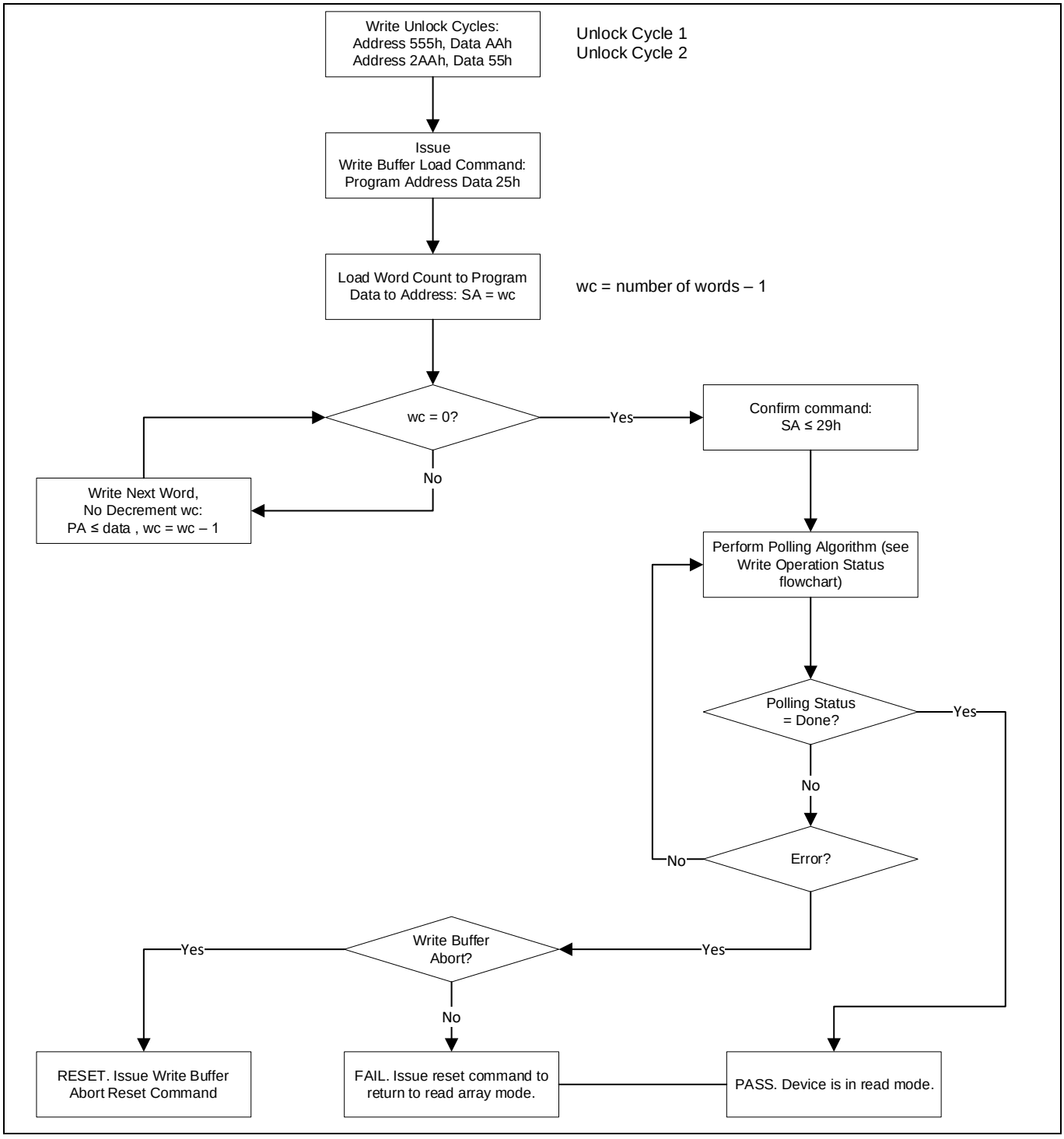
```
/* insert code to poll for completion */

/* Example: Write Buffer Abort Reset */
*( (volatile UINT16 *)addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (volatile UINT16 *)addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (volatile UINT16 *)addr + 0x555 ) = 0x00F0; /* write buffer abort reset */
```

The write buffer page is selected by using the addresses Amax – A8. The write buffer page addresses must be the same for all address/data pairs loaded into the write buffer. Write buffer programming cannot be performed across multiple write buffer pages and sectors. If a write buffer address is loaded multiple times, the address/data pair counter decrements for every data load operation. The software takes care of the ramifications of loading a write buffer location more than once.

Write buffer programming operation can be suspended using the suspend/resume command. If the write buffer command sequence is entered incorrectly the device enters write buffer abort.

Write Buffer Programming in S29GL-T Devices



5 Conclusion

The write buffer programming feature of MirrorBit Flash memory devices can decrease the programming time by over 95%, when compared to single word programming. Write buffer programming is enabled via a simple addition of three commands to the standard embedded algorithm bus command set.

The read page buffer feature of MirrorBit Flash memories can increase performance significantly. Following each random (inter-page) access all locations of the referenced 16-word page are available for fast access. When read accesses can be grouped within a page the average read performance can be increased by 3 to 4 times.

Revision history

Document version	Date of release	Description of changes
**	2006-11-10	New application note
*A	2019-11-21	Updated with the S29GL-T features and removed references to the S29PL-N. Updated to template
*B	2021-03-30	Updated to Infineon template

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