AN98595

Migration from Winbond W25Qxx 3.0-V SPI to Cypress S25FL1-K 3.0-V SPI

AN98595 details the feature set comparisons, package variations, common signal pin/ball assignments, Clock modes, Manufacturers and Device ID's, command set comparisons as well as timing comparisons, migrating from the W25Qxx 3.0V 16-Mb, 32-Mb, and 64-Mb SPI flash to Cypress's S25FL1-K 3.0V 16-Mb, 32-Mb, and 64-Mb SPI flash memory products.

Contents

1 Overview

This application note details the feature set comparisons, package variations, common signal pin/ball assignments, Clock modes, Manufacturers and Device ID's, command set comparisons as well as timing comparisons, migrating from the W25Qxx 3.0V 16-Mb, 32-Mb, and 64-Mb SPI flash to Cypress's S25FL1-K 3.0V 16-Mb, 32-Mb, and 64-Mb SPI flash memory products.

Table 1. Feature Set Comparison v (Sheet 1 of 2)

Parameter	S25FL1-K	W25Q64FV	W25Q32FV	W25Q16CV
Technology Node	90 nm	58 nm	58 nm	90 nm
Architecture	Floating Gate	Floating Gate	Floating Gate	Floating Gate
Density	16 Mbit - 64 Mbit	64 Mbit	32 Mbit	16 Mbit
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V
Normal Read Speed	6 MB/s (50 MHz)	50 MHz (see Table 2)	50 MHz (see Table 2)	50 MHz (see Table 2)
Fast Read Speed	13.5 MB/s (108 MHz)	104 MHz (see Table 2)	104 MHz (see Table 2)	104 MHz (see Table 2)
Dual Read Speed	27 MB/s (108 MHz)	104 MHz (see Table 2)	104 MHz (see Table 2)	104 MHz (see Table 2)
Quad Read Speed	54 MB/s (108 MHz)	104 MHz (see Table 2)	104 MHz (see Table 2)	104 MHz (see Table 2)
Program Buffer Size	256B	256B	256B	256B
Page Program Time (Typ)	700 µs (256B)	700 µs (256B)	700 µs (256B)	700 µs (256B)
Program Suspend/Resume	Yes	Yes	Yes	Yes
Erase Sector Size	4 kB, 64 kB	4 kB, 32 kB, 64 kB	4 kB, 32 kB, 64 kB	4 kB, 32 kB, 64 kB
Parameter Sector Size	N/A	N/A	N/A	N/A
Sector Erase Time (Typ)	70 ms (4 kB) / 350 ms (64 kB)	60 ms (4 kB) / 150 ms (64 kB)	100 ms (4 kB) / 150 ms (64 kB)	30 ms (4 kB) / 150 ms (64 kB)
Erase Suspend/Resume	Yes	Yes	Yes	Yes

Table 1. Feature Set Comparison v (Sheet 2 of 2)

Parameter	S25FL1-K	W25Q64FV	W25Q32FV	W25Q16CV
OTP Size	768B (3 x 256B)	768B (3 x 256B)	768B (3 x 256B)	768B (3 x 256B)
Operating Temperature	-40°C to +85°C / +105°C (1)	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C / +105°C (1)
SPI SCLK Modes Supported	0, 3	0, 3	0, 3	0, 3

Note:

1. *Automotive Temperature Grade.*

2. W25Qxx Operating Clock Frequencies

Table 2. W25Qxx Operating Clock Frequencies

Operating Clock Frequency Conditions and Commands	W25Q64FV	W25Q32FV	W25Q16CV
Read Data Command — 03h 2.7V to 3.0V / 3.0V to 3.6V	33 MHz / 50 MHz (max)	50 MHz (max)	50 MHz (max)
All instructions except Read Data — 03h and Octal Word Read - E3h 3.0V to 3.6V and Commercial Temperature	—	—	104 MHz (max)
Octal Word Read Quad I/O — E3h 3.0V to 3.6V and Industrial Temperature	—	—	50 MHz (max)
All instructions except Read Data — 03h and Octal Word Read — E3h 2.7V to 3.6V and Industrial Temperature	—	—	80 MHz (max)
QPI Read Instructions — 0Bh and Ebh with 2/4/6/8 dummy Clocks	40 / 60 / 80 / 104 MHz	33 MHz to 104 MHz	—
QPI Read Instructions — 0Ch with 2/4/6/8 dummy Clocks	50 / 80 / 104 / 104 MHz	33 MHz to 104 MHz	—
All other SPI/QPI instructions 2.7V to 3.0V / 3.0V to 3.6V	80 MHz / 104 MHz	104 MHz	—

3 Surface Mount Package Variations

Table 3. Cypress SPI Package Offerings

S25FL1-K	64 Mb	32 Mb	16 Mb
6 mm x 5 mm, 8 contact-WSON	√	√	√
8 pin-SOIC (150-mil)	—	√	√
8 pin-SOIC (208-mil)	√	√	√
16 pin-SOIC (300-mil)	√	—	—
8 mm x 6 mm, 24ball-BGA, 5 x 5 config.	√	√	√
8mm x 6mm, 24 ball-BGA, 6 x 4 config.	√	√	√

Table 4 . 2 Winbond SPI Package Offerings

W25Qxx	64 Mb	32 Mb	16 Mb
6 mm x 5 mm, 8 contact-WSON	√	√	√
8 pin-SOIC (150-mil)	—	—	√
8 pin-SOIC (208-mil)	√	√ (1)	√
16 pin-SOIC (300-mil)	√	√	√
8 mm x 6 mm, 24ball-BGA, 5 x 5 config.	√	√	—
8 mm x 6 mm, 24ball-BGA, 6 x 4 config.	√	√	√

Note:

1. *For W25Q32FV, input signal pin#3 is H/W RESET#.*

4 8-Pin and 16-Pin SOIC, and 8-Contact WSON Signal Pin Assignments

Signal pin assignments are identical for both 8-pin SOIC and 16-pin SOIC, as well as the 8-contact WSON package. Therefore, migration from the W25Qxx to the S25FL1-K, in regards to pin assignments is seamless. However, it is important to note, for the S25FL1-K, those pins designated as “DNU” (Do Not Use) for the 16-pin SO package should be left floating and not connected to any V_{IH} or V_{IL} logic level, or GND plane. The S25FL1-K, 16-pin SO package actually has an internal bond-wire connection from the lead-frame to the die, itself. Pins designated as “RFU” or “NC” do not have any internal bond-wire connection from the lead-frame to the die, itself. However, “RFU” pins should not be routed, but rather, reserved for the possibility of future enhanced features.

Table 5. Common Signal Pin Assignments

Signal Pins	W25Qxx	Common Pin # 16-pin SOIC	Common Pin # 8-contact, WSON / 8-pin SOIC	S25FL1-K
Chip Select	/CS	7	1	CS#
Serial Data Out	DO / IO1	8	2	SO / IO1
Write Protect	/WP / IO2	9	3	WP# / IO2
GND / V_{SS}	GND	10	4	V_{SS}
Serial Data In	DI / IO0	15	5	SI / IO0
Serial Clock	CLK	16	6	SCLK
Hold	/Hold / IO3	1	7 (2)	Hold# / IO3
V_{CC}	V_{CC}	2	8	V_{CC}
NC / DNU / RFU	NC	3 (1)	—	DNU
NC / DNU / RFU	NC	4	—	DNU
NC / DNU / RFU	NC	5	—	DNU
NC / DNU / RFU	NC	6	—	DNU
NC / DNU / RFU	NC	11	—	DNU
NC / DNU / RFU	NC	12	—	DNU
NC / DNU / RFU	NC	13	—	DNU
NC / DNU / RFU	NC	14	—	DNU

Notes:

1. *For W25Q32FV (16-pin SOIC), input signal pin#3 is H/W /RESET.*
2. *For W25Q32FV (8-pin/8-contact configuration), when QE=0, the I/O3 can be configured either as a /HOLD input signal pin, or as a / RESET input signal pin depending on status register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin/ 8-contact configuration.*

5 8 mm x 6 mm 24-ball FBGA Ball Array Signal Assignments

Ball signal assignments are identical for both 8-pin SOIC and 16-pin SOIC, as well as the 8-contact WSON package. Therefore, migration from the W25Qxx to the S25FL1-K, in regards to pin assignments is seamless. However, it is important to note, for the S25FL1-K, those pins designated as “DNU” (Do Not Use) for the 16-pin SO package should be left floating and not connected to any V_{IH} or V_{IL} logic level, or GND plane. The S25FL1-K, 16-pin SO package actually have an internal bond-wire connection from the lead-frame to the die, itself. Pins designated as “RFU” or “NC” do not have any internal bond-wire connection from the lead-frame to the die, itself. However, “RFU” pins should be reserved for the possibility of future enhanced features, and not routed.

Table 6. 5x5 Common Ball Array Configuration

Signals	W25Qxx Q64FV / Q32FV	Common Ball Assignment	S25FL1-K
Chip Select	/CS	C2	CS#
Serial Data Out	DO / IO1	D2	SO / IO1
Write Protect	/WP / IO2	C4	WP# / IO2
GND / V_{SS}	GND	B3	V_{SS}
Serial Data In	DI / IO0	D3	SI / IO0

Table 6. 5x5 Common Ball Array Configuration

Signals	W25Qxx Q64FV / Q32FV	Common Ball Assignment	S25FL1-K
Serial Clock	CLK	B2	SCLK
Hold	/Hold / IO3	D4	Hold# / IO3
V_{CC}	V_{CC}	B4	V_{CC}
NC / DNU / RFU	No Ball	A1	No ball
NC / DNU / RFU	NC	A2	NC
NC / DNU / RFU	NC	A3	NC
NC / DNU / RFU	NC	A4	RFU
NC / DNU / RFU	NC	A5	NC
NC / DNU / RFU	NC	B1	DNU
NC / DNU / RFU	NC	B5	NC
NC / DNU / RFU	NC	C1	DNU
NC / DNU / RFU	NC	C3	RFU
NC / DNU / RFU	NC	C5	NC
NC / DNU / RFU	NC	D1	DNU
NC / DNU / RFU	NC	D5	NC
NC / DNU / RFU	NC	E1	NC
NC / DNU / RFU	NC	E2	NC
NC / DNU / RFU	NC	E3	NC
NC / DNU / RFU	NC	E4	RFU
NC / DNU / RFU	NC	E5	NC

Table 7. 6 x 4 Common Ball Array Configuration

Signals	W25Qxx Q64FV / Q32FV / Q16CV	Common Ball Assignments	S25FL1-K
Chip Select	/CS	C2	CS#
Serial Data Out	DO / IO1	D2	SO / IO1
Write Protect	/WP / IO2	C4	WP# / IO2
GND / V_{SS}	GND	B3	V_{SS}
Serial Data In	DI / IO0	D3	SI / IO0
Serial Clock	CLK	B2	SCLK
Hold	/Hold / IO3	D4	Hold# / IO3
V_{CC}	V_{CC}	B4	V_{CC}
NC / DNU / RFU	NC	A1	NC
NC / DNU / RFU	NC	A2	NC
NC / DNU / RFU	NC	A3	NC
NC / DNU / RFU	NC	A4	RFU
NC / DNU / RFU	NC	B1	DNU
NC / DNU / RFU	NC	C1	DNU
NC / DNU / RFU	NC	C3	RFU
NC / DNU / RFU	NC	D1	DNU
NC / DNU / RFU	NC	E1	NC
NC / DNU / RFU	NC	E2	NC
NC / DNU / RFU	NC	E3	NC
NC / DNU / RFU	NC	E4	RFU
NC / DNU / RFU	NC	F1	NC
NC / DNU / RFU	NC	F2	NC
NC / DNU / RFU	NC	F3	NC
NC / DNU / RFU	NC	F4	NC

6 SPI Clock Modes

The S25FL1-K supports SPI Clock Mode 0, as well as Mode 3, identical to that of the W25Qxx family series.

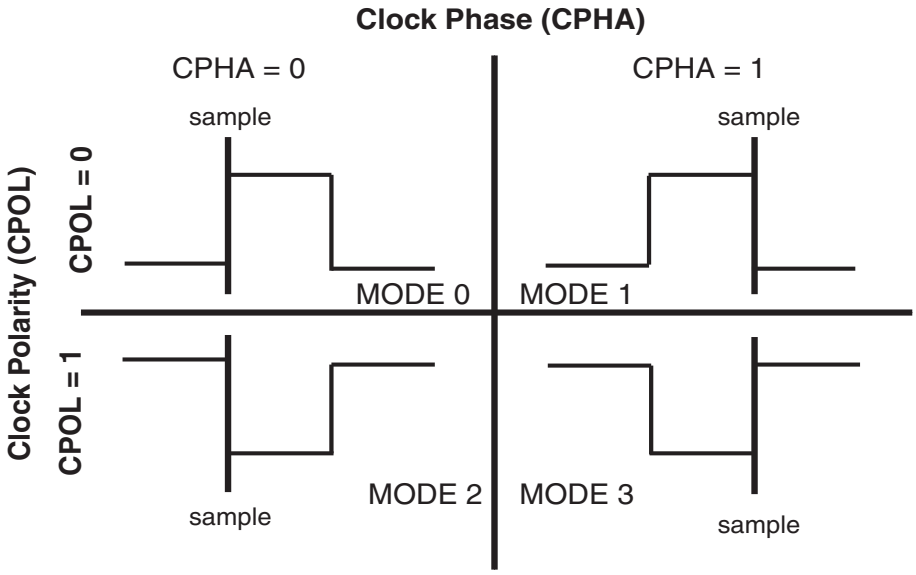
To determine the SPI clock polarity and phase modes, the CLK polarity (CPOL) is the high-order bit and determines the logic level of the CLK signal when the SPI flash is idle or in standby mode. The CLK phase (CPHA) is the low order bit and determines which CLK transition is used to latch data.

- SCLK will stay at logic low state with CPOL = 0, CPHA = 0 (Mode 0)
- SCLK will stay at logic high state with CPOL = 1, CPHA = 1 (Mode 3)

When the CLK polarity is equal to zero (CPOL = 0), and CLK phase is equal to zero (CPHA = 0), input data is latched on the first leading (rising) edge of the CLK; while data is outputted on the next falling edge of the CLK; this is Mode 0.

When the CLK polarity is equal to one (CPOL = 1) and CLK phase is equal to one (CPHA = 1), input data is latched on the first leading (rising) edge of the CLK; while data is outputted on the next falling edge of the CLK; this is Mode 3.

Mode 0 and Mode 3 Clock sampling are detailed directly below.



7 Manufacturer and Device Type Identification

Both S25FL1-K and W25Qxx support identical manufacturer ID, device ID, device type and capacity instructions. However, the S25FL1-K has a simplistic instruction set, regardless of SPI mode.

Table 8. Manufacturer and Device ID — S25FL1-K

Device OPN	Instruction	Data 1	Data 2	Data 3
S25FL116K	ABh 90h 9Fh (JEDEC)	— Manufacturers ID = 01h Manufacturers ID = 01h	Device ID = 14h Device ID = 14h Device Type = 40h	— — Capacity = 15h
S25FL132K (SPI Mode) (SPI Mode)	ABh 90h 9Fh (JEDEC)	— Manufacturers ID = 01h Manufacturers ID = 01h	Device ID = 15h Device ID = 15h Device Type = 40h	— — Capacity = 16h
S25FL164K (SPI Mode) (SPI Mode)	ABh 90h 9Fh (JEDEC)	— Manufacturers ID = 01h Manufacturers ID = 01h	Device ID = 16h Device ID = 16h Device Type = 40h	— — Capacity = 17h

Table 9. Manufacturer and Device ID — W25QxxFV/CV (Sheet 1 of 2)

Device OPN	Instruction	Data 1	Data 2	Data 3
W25Q16CV	ABh 90h 9Fh (JEDEC)	— Manufacturers ID = EFh Manufacturers ID = EFh	Device ID = 14h Device ID = 14h Device Type = 40h	— — Capacity = 15h

Table 9. Manufacturer and Device ID — W25QxxFV/CV (Sheet 2 of 2)

Device OPN	Instruction	Data 1	Data 2	Data 3
W25Q32FV (SPI Mode) (Dual I/O) (Quad I/O) (SPI Mode)	ABh 90H 92h 94h 9Fh (JEDEC)	— Manufacturers ID = EFh Manufacturers ID = EFh Manufacturers ID = EFh Manufacturers ID = EFh	Device ID = 15h Device ID = 15h Device ID = 15h Device ID = 15h Device Type = 40h	— — — — Capacity = 16h
W25Q64FV (SPI Mode) (Dual I/O) (Quad I/O) (SPI Mode)	ABh 90H 92h 94h 9Fh (JEDEC)	— Manufacturers ID = EFh Manufacturers ID = EFh Manufacturers ID = EFh Manufacturers ID = EFh	Device ID = 16h Device ID = 16h Device ID = 16h Device ID = 16h Device Type = 40h	— — — — Capacity = 17h

8 Commands / Instruction Set

Both the S25FL1-K and W25QxxFV/CV support similar command /instruction sets. Refer to the respective data sheets regarding command/instructions specifics.

Table 10. Similar Command/Instruction Set Supported by Both S25FL1-K and W25QxxFV/CV (Sheet 1 of 2)

Command name	Instruction	Opcode
Read Operations		
Read	Read data bytes	03h
Fast Read	Read data bytes at higher speed	0Bh
Fast Read Dual Output	Dual Output Read of data bytes at higher speed	3Bh
Read_ID	Read manufacturer and Device ID	90h
RDID	Read JEDEC ID	9Fh
Fast Read Quad Output	Quad Output Read of data bytes at higher speed	6Bh
Fast Read Dual I/O	Dual I/O Read of data bytes at higher speed	BBh
Fast Read Quad I/O	Quad I/O Read of data bytes at higher speed	EBh
Status and Configuration Register Operations		
RDSR-1	Read Status Register-1	05h
RDSR-2	Read Status Register-2	35h
RDSR-3	Read Status Register-3 (1)	33h (S25FL1-K) / 15h (W25Q32FV only)
WRR	Write (Status and Configuration) Register	01h
Read SFDP	Read Serial FLASH Discovery Parameter Register	5Ah
Program and Erase Operations		
PP	Page Program	02h
P4E	4-kB Sector Erase	20h
BE	Chip, Bulk Erase	C7h, 60h
SE	64-kB Block Erase	D8h
SUSPEND (SUS)	Erase/Program Suspend	75h
RESUME	Erase/Program Resume	7Ah

Table 10. Similar Command/Instruction Set Supported by Both S25FL1-K and W25QxxFV/CV (Sheet 2 of 2)

Command name	Instruction	Opcode
Write Control		
WRDI	Write Disable	04h
WREN	Write Enable	06h
WREN Volatile SR	Write Enable for Volatile Status Register	50h
	Power Saving Mode	
RES	Release from Power-Down and read Device Signature	ABh
DPD	Deep Power-Down	B9h
Security Registers		
Read	Read Security Register	48h
Erase	Erase Security Register	44h
Program	Program Security Register	42h
Burst Wrap Mode		
Burst with Wrap	Set Burst Mode with Wrap	77h

Note:

1. *Read Status Register-3 is available on W25Q32FV only; opcodes are not compatible.*

Table 11. The S25FL1-K — Non-supported W25QxxFV/CV Commands

Command	Instruction	Opcode
Block Erase (32 kB)	Erases 32-kB block	52h
QPI Enable	Enables QPI	38h
Reset Enable	Enables Reset	66h
Reset	Resets SPI flash device	99h
Word Read Quad I/O	—	E7h
Octal Word Read Quad I/O	—	E3h
Manufacturer/Device ID by Dual I/O	—	92h
Manufacturer/Device ID by Quad I/O	—	94h
Global Block Lock (1)	—	7Eh
Global Block Unlock (1)	—	98h
Unique ID Read	Reads Unique Identification	4Bh
Quad Page Program	Page Programming in Quad Mode	32h
Individual Block Lock (1)	Locks Block individually	36h
Individual Block Unlock (1)	Unlocks Block individually	39h
Block Lock Read (1)	Reads status of Block lock	3Dh
Write Status Register-1 (1)	—	01h
Write Status Register-2 (1)	—	31h
Write Status Register-3 (1)	—	11h

Note:

1. *Available on W25Q32FV only.*

9 DC Parameter Differences

Table 12. DC Parameter Differences

Parameter	Range	S25FL1-K	W25Q64FV	W25Q32FV	W25Q16CV	Unit
Standby Current	Typ. / Max.	20	10 / 50	10 / 50	10 / 25	µA
Power-Down Current	Typ. / Max.	2	1 / 25	1 / 20	1 / 5	µA
Read Current Single / Dual / Quad @ 1 MHz	Typ. Max.	4/ 5/ 6 6 / 7.5 / 9	— 15	4 10	4 / 5 / 6 6 / 7.5 / 9	mA
Read Current Single / Dual / Quad @ 50 MHz	Typ. Max.	7 / 8 / 9 10 / 12 / 13.5	— 20	— 15	7 / 8 / 9 10 / 12 / 13.5	mA
Read Current Single / Dual / Quad @ 108 MHz	Typ. Max.	12 / 14 / 16 18 / 22 / 25	—	—	—	mA
Read Current Single / Dual / Quad @ 104 MHz	Max.	—	— 40	— 20	—	mA

10 AC Parameter Differences

Table 13. AC Parameter Differences

Parameter	Range	S25FL1-K	W25Q64FV	W25Q32FV	W25Q16CV	Unit
Input Rise and Fall Times	Max.	2.4	5	5	5	ns
Clock Frequency for all SPI commands, except for command 03h and 0Bh	Max.	108	80 / 104	104	80	MHz
Clock Frequency for Read command 03h	Max.	50	33 / 50	50	50	MHz
Clock Frequency for all Fast Read commands	Max.	108	80 / 104	104	104	mA
Data In Hold Time	Min.	5	3	3	5	ns
Output Hold Time	Min.	2	0	2	0	ns
CS# Deselect Time (for Array Read -> Array Read)	Min.	7	10	10	10	ns
CS# Deselect Time (for Erase or Program -> Read Status Registers); and Volatile Status Register Write Time	Min.	40	50	50	50	ns
CS# high to Standby mode without Electronic Signature Read	Max.	3	30	3	3	µs
CS# high to Standby mode with Electronic Signature Read	Max.	1.8	30	1.8	1.8	µs
Write Status Registers Time	Typ.	10	15	10	10	ms
Byte Program Time (first Byte)	Typ.	10	20	30	30	µs
Additional Byte Programming Time (after first Byte)	Typ. Max.	2.5 12	2.5 10	2.5 12	2.5 12	µs
Sector Erase Time (4 kB)	Typ. / Max.	70 / 450	60 / 400 (1)	100 / 400	30 / 400 (1)	ms
Block Erase Time (64 kB)	Typ. / Max.	350 / 2,000	150 / 2,000	150 / 2,000	150 / 1,000	ms
Chip Erase Time (16 Mb, 32 Mb, 64 Mb)	Typ. Max.	11.2 / 22.4 / 44.8 64 / 128 / 256	20 100	10 50	3 10	s

Note:

1. *Greater than 50K, but less than 100K P/E cycles, Sector Erase is 400 ms.*

11. Serial FLASH Discoverable Parameter (SFDP)

The S25FL1-K and W25QxxFV/CV both feature the 256-byte Serial Flash Discoverable Parameter (SFDP) space. The SFDP space contains information about the device operational capabilities such as available commands, timing, and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables.

Table 14. S25FL1-K Status Registers and Functions

Status Register - 1 (SR-1)	Name	Function	S25FL1-K
Bit - 7	SRP0	Status Register Protect 0	√
Bit - 6	SEC	Sector / Block Protect	√
Bit - 5	TB	Top / Bottom Protect	√
Bit - 4	BP-2	Block Protect Bits	√
Bit - 3	BP-1	Block Protect Bits	√
Bit - 2	BP-0	Block Protect Bits	√
Bit - 1	WEL	Write Enable Latch	√
Bit - 0	BUSY	Embedded Operation Status	√
Status Register - 2 (SR-2)	**Name**	**Function**	**S25FL1-K**
Bit - 7	SUS	Suspend status	√
Bit - 6	CMP	Complement Protect	√
Bit - 5	LB-3	Security Register Lock Bits	√
Bit - 4	LB-2	Security Register Lock Bits	√
Bit - 3	LB-1	Security Register Lock Bits	√
Bit - 2	LB-0	Security Register Lock Bits	√
Bit - 1	QE	Quad Enable	√
Bit - 0	SRP-1	Status Register Protect - 1	√
Status Register - 3 (SR-3)	**Name**	**Function**	**S25FL1-K**
Bit - 7	RFU	Reserved	√
Bit - 6	W6	Burst Wrap Length	√
Bit - 5	W5	Burst Wrap Length	√
Bit - 4	W4	Burst Wrap Enable	√
Bit - 3	LC	Variable Read Latency Control	√
Bit - 2	LC	Variable Read Latency Control	√
Bit - 1	LC	Variable Read Latency Control	√
Bit - 0	LC	Variable Read Latency Control	√

Table 15. W25Qxx Status Registers and Functions (Sheet 1 of 2)

Status Register - 1 (SR-1)	Name	Function	W25Q64FV	W25Q32FV	W25Q16CV
S7	SRP0	Status Register Protect 0	√	√	√
S6	SEC	Sector / Block Protect	√	√	√
S5	TB	Top / Bottom Protect	√	√	√
S4	BP-2	Block Protect Bits	√	√	√
S3	BP-1	Block Protect Bits	√	√	√
S2	BP-0	Block Protect Bits	√	√	√
S1	WEL	Write Enable Latch	√	√	√
S0	BUSY	Embedded Operation Status	√	√	√

Table 15. W25Qxx Status Registers and Functions (Sheet 2 of 2)

Status Register - 2 (SR-2)	Name	Function	W25Q64FV	W25Q32FV	W25Q16CV
S15	SUS	Suspend status	√	√	√
S14	CMP	Complement Protect	√	√	√
S13	LB-3	Security Register Lock Bits	√	√	√
S12	LB-2	Security Register Lock Bits	√	√	√
S11	LB-1	Security Register Lock Bits	√	√	√
S10	(R)	Reserved	Reserved	Reserved	Reserved
S9	QE	Quad Enable	√	√	√
S8	SRP-1	Status Register Protect - 1	√	√	√
Status Register - 3 (SR-3)	**Name**	**Function**	**W25Q64FV**	**W25Q32FV**	**W25Q16CV**
S23	Hold/RST	Hold# / RESET#	—	√	—
S22	DRV-1	Output Driver Strength	—	√	—
S21	DRV-0	Output Driver Strength	—	√	—
S20	(R)	Reserved	—	√	—
S19	(R)	Reserved	—	√	—
S18	WPS	Write Protection Selection	—	√	—
S17	(R)	Reserved	—	√	—
S16	(R)	Reserved	—	√	—

12 Block Protection Bits (BPx)

The S25FL1-K and W25QxxFV/CV both feature Block Protection Bits (BP2, BP1, BP0), located in Status Register-1 (bits 4, 3, 2, respectively). The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write and provide Write Protection control and status. The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

13 Complement Protect (CMP)

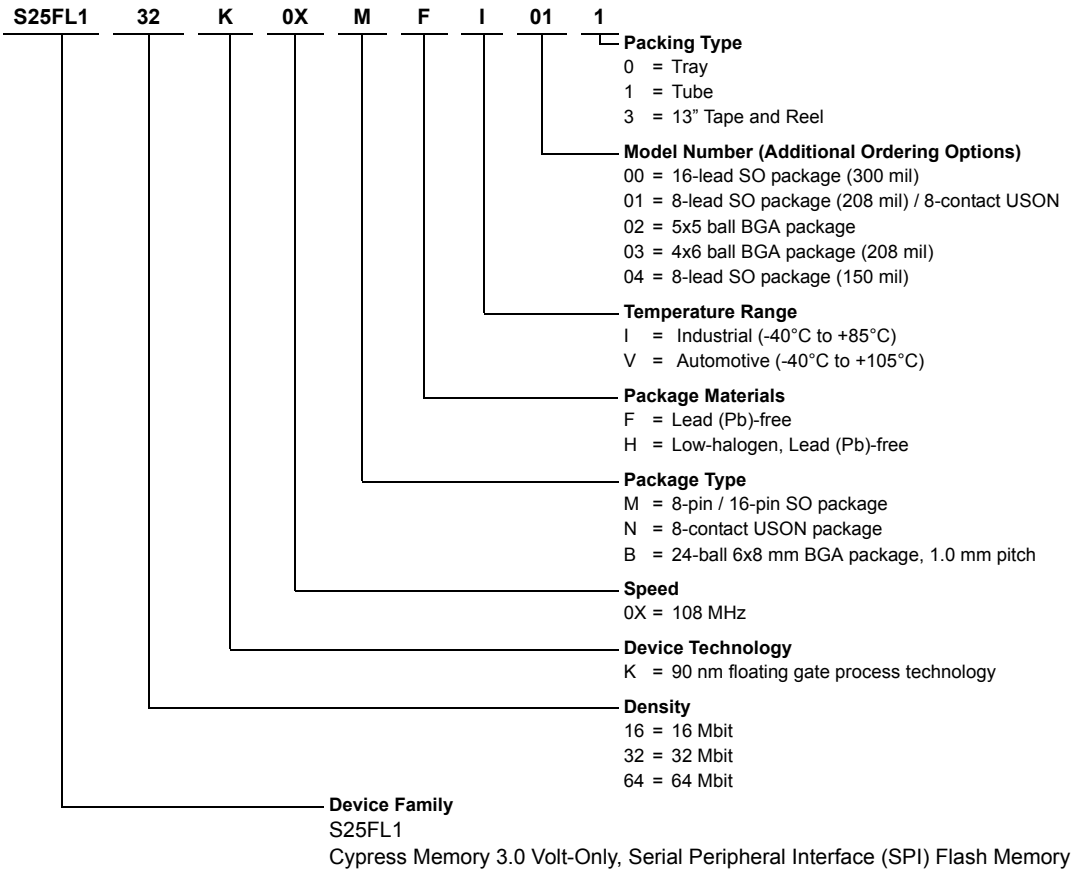
The S25FL1-K and W25QxxFV/CV both feature the Complementary Protect (CMP). The Complement Protect bit is located in SR2, Bit-6 for the FL1-K, and SR2, Bit-14 for the W25Qxx. Bit 6 and Bit 14 are actually the same bits position within SR2. However, the labeling convention is different. The CMP bits are non-volatile read/write bits and are used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection.

14 Security Register Lock Bits

The S25FL1-K and W25QxxFV/CV both feature the Security Register Lock Bits (LB3, LB2, LB1, LB0), located in Status Register-2 (SR2 - bit-5, bit-4, bit-3, bit-2, respectively), and provide the write protect control and status to the Security Registers. Security Register-0 LB0 (SR2[2]) for the S25FL1-K contains the Serial FLASH Discoverable Parameters (SFDP) and is programmed by Cypress. The default state of LB3, LB2, LB1 is 0, Security Registers LB1, LB2, LB3 are unlocked and can be set to 1 individually using the Write Status Registers command. Please note that LB3, LB2, LB1 are One-Time Programmable (OTP), once it is set to 1, the corresponding 256-byte Security Register will become read-only permanently. The W25Q32FV does not support the Security Register-0 Lock Bit feature.

15 S25FL1-K Ordering Information

The ordering part number is formed by a valid combination of the following:



16 Conclusion

The S25FL1-K is featured with automotive temperature grade, streamlined package offering (16-pin and 8-pin SO; 8 mm x 6 mm BGA in 5x5 ball, and 6x4 ball common configuration; as well as 8-lead WSON), Pb-Free and Low halogen package material sets that meet RoHS compliance, and fastest dual and quad read speed of 108 MHz.

The S25FL1-K's feature set comparison, device ID, command/instruction set, status registers, Block Protection Bits, Complement Protect, Security Register Lock Bits, and operating Clock modes are similar, if not identical, to that of the W25Qxx, making the S25FL1-K series an exceptional migration path from the W25Qxx family series.

17 References

- Data Sheet for the W25Q64FVxx, April 13, 2012, Revision D
- Data Sheet for the W25Q32FVxx, April 13, 2012, Revision B (Preliminary)
- Data Sheet for the W25Q16CVxx, April 01, 2011, Revision C
- "Winbond Electronics Enters Automotive FLASH Memory Market" article — February 27, 2012 www.winbond.com
- S25FLK-1 Design Requirement Specification - August 15, 2012, Revision 2

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*A	4928490	MSWI	09/21/2015	Updated in Cypress template
*B	5844184	AESATMP8	08/04/2017	Updated logo and Copyright.

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