AN98590

Migration from Cypress S29NS-R to S29VS-R

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AN98590 discusses the new features of S29VS-R and the considerations the designer should make when migrating from S29NS-R.

1 Introduction

The S29VS-R MirrorBit® Flash family offers a line of 1.8-Volt, burst mode, simultaneous read and write, Address and Data Multiplexed (ADM) products. This guide discusses the new features of S29VS-R and the considerations the designer should make when migrating from S29NS-R. In this migration guide, S29VS-R and VS-R refer to the 128 Mb and 256 Mb densities only. For migration from S29NS-P, please also see the application note, Migrating from S29NS-P to S29VS-R (Migrate_S29NS-P_to_S29VS-R_AN).

2 Feature Comparisons Summary

The following lists the items to consider when migrating from NS-R to VS-R:

- VS-R is an 8-bank device, compared with the 16 banks of the NS-R
- VS-R has different Device ID values than the NS-R
- VS-R has some differences from NS-R in AC and DC parameters

Table 1. Feature Comparisons (Sheet 1 of 2)

Key Features	NS-R	VS-R
Technology	MirrorBit	MirrorBit
Process Node	65 nm	65 nm
Densities	128 to 512 Mb	128 and 256 Mb
Data Bus Width	16-bit (Word)	16-bit (Word)
Bus Interface	ADM	ADM
VCC	1.70V to 1.95V	1.70V to 1.95V
Temperature Range	Wireless (-25°C to +85°C)	Wireless (-25°C to +85°C) Industrial (-40°C to +85°C)
Common Flash Interface (CFI)	Yes	Yes
Burst Frequency Order Options	66 / 83 MHz	83 / 104 / 108 MHz
Burst Length (linear, words)	8 / 16 with wrap-around / continuous	8 / 16 with wrap-around / continuous
Data Transfer Flow Control	Yes (RDY)	Yes (RDY)
Sector Erase Architecture	32 KB small sectors, 128 KB large sectors	32 KB small sectors, 128 KB large sectors
Boot Sector Architecture	NS128R/NS256R : top	VS128/256RxxBHW00 : top
	NS512R/NS01GR : uniform	VS128/256RxxBHW01 : bottom
Banks	16	8
Command Set	Reduced (no unlock cycles)	Reduced (no unlock cycles)
DQ Polling	No	No
Status Register	Yes	Yes
Write Buffer Programming	64-Byte Write Buffer	64-Byte Write Buffer
Single Word Programming	No	No

Table 1. Feature Comparisons (Sheet 2 of 2)

Key Features	NS-R	VS-R
Program Suspend / Resume	Yes	Yes
Erase Suspend / Resume	Yes	Yes
Low VCC Write Inhibit	Yes	Yes
Hardware Sector Protection	VPP pin	VPP pin
Software Sector Protection	Sector Lock Range, Sector Lock/ Unlock	Sector Lock Range, Sector Lock/ Unlock
Secure Silicon Region	256 Bytes factory locked	256 Bytes factory locked
	256 Bytes customer lockable	256 Bytes customer lockable
Program-Erase Endurance	100,000 cycles per sector (typical)	100,000 cycles per sector (typical)
Data Retention	10-year (typical)	10-year (typical)
Discrete Packages	NS128R/NS256R : 44-ball, 0.50 mm pitch FBGA (Low-Halogen, Pb-free)	44-ball, 0.50 mm pitch FBGA (Low-Halogen, Pb-free)
	NS512R : 64-ball, 0.50 mm pitch FBGA (Low-Halogen , Pb-free)	
Discrete Package Sizes (mm)	8.0 x 9.2, 6.2 x 7.7	6.2 x 7.7

3 Flash Memory Array

The VS-R is an 8-bank device, compared with the 16 banks of the NS-R. The sector sizes are the same for both families. The NS512R has uniform sector sizes, while the NS128R and NS256R have top boot sectors. The VS128R and VS256R are both available with top or bottom boot sectors. These differences in bank and sector architecture may require software changes. Refer to the device data sheets for memory address maps.

Table 2. NS256R to VS256R Bank/Sector Example

Format of Flash Image	NS256R			VS256R (Top Boot)		
	Bank	Sector Size	Number of Sectors	Bank	Sector Size	Number of Sectors
OS Image	0	128 KB	16	0	128 KB	32
	1	128 KB	16			
File System Volume	2	128 KB	16	1	128 KB	32
	3	128 KB	16			
	…	128 KB	16	…	128 KB	32
	…	128 KB	16			
	12	128 KB	16	6	128 KB	32
	13	128 KB	16			
	14	128 KB	16	7	128 KB	31
	15	128 KB	15			
Bootloader		32 KB	4		32 KB	4

In the example from Table 2, a product can be populated with either NS256R or VS256R. This Operating System image requires 2 MB of flash space, and fits into bank 0 on NS256R, but on VS256R, it requires a separate bank to enable Simultaneous Read/Write. In order to maintain a single flash image, 4 MB of space is set aside for the OS on both devices.

4 Device Identification

The VS-R has different Device Identification (ID) code values than the NS-R.

Table 3. Device ID Codes

Description	NS256/128R		VS256/128R	
	Word Offset	Data	Word Offset	Data
Manufacturer ID	(BA) + 00h	0001h	(SA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	397Eh (NS256R) 3A7Eh (NS128R)	(SA) + 01h	007Eh (VS256R) 007Eh (VS128R)
Device ID, Word 2	(BA) + 0Eh	3917h (NS256R) 3A35h (NS128R)	(SA) + 0Eh	0064h (VS256R Top) 0066h (VS256R Bottom) 0063h (VS128R Top) 0065h (VS128R Bottom)
Device ID, Word 3	(BA) + 0Fh	3903h (NS256R) 3A03h (NS128R)	(SA) + 0Fh	0001h (VS256R) 0001h (VS128R)
Indicator Bits	(BA) + 07h	**DQ15 - DQ8 = Reserved** **DQ7 - Factory Lock Bit:** 1 = Locked 0 = Not Locked **DQ6 - Customer Lock Bit:** 1 = Locked 0 = Not Locked **DQ5 - DQ0 = Reserved**	(SA) + 07h	**DQ15 - DQ8 = Reserved** **DQ7 - Factory Lock Bit:** 1 = Locked 0 = Not Locked **DQ6 - Customer Lock Bit:** 1 = Locked 0 = Not Locked **DQ5 - DQ0 = Reserved**

5 Electrical Specification Differences

Electrical considerations for porting from NS-R to VS-R are described below. Please refer to the device data sheets for a detailed description of electrical specifications.

Table 4. DC Characteristics

Parameter	Description		Min / Typ / Max	NS-R	VS-R
I_{CCB}	V_{CC} Active Burst Read Current (burst length 8)	83 MHz	Typ	32 mA (1)	35 mA (2)
		104 MHz	Typ	36 mA (1)	39 mA (2)
		83 MHz	Max	36 mA (1)	38 mA (2)
		104 MHz	Max	44 mA (1)	44 mA (2)
	V_{CC} Active Burst Read Current (burst length 16)	83 MHz	Typ	32 mA (1)	28 mA (2)
		104 MHz	Typ	36 mA (1)	32 mA (2)
		83 MHz	Max	38 mA (1)	30 mA (2)
		104 MHz	Max	40 mA (1)	36 mA (2)
	V_{CC} Active Burst Read Current (continuous burst)	83 MHz	Typ	36 mA (1)	28 mA (2)
		104 MHz	Typ	40 mA (1)	32 mA (2)
		83 MHz	Max	42 mA (1)	30 mA (2)
		104 MHz	Max	44 mA (1)	36 mA (2)
I_{CC1}	V_{CC} Active Asynchronous Read Current (tested at 10 MHz)		Max	80 mA (1)	60 mA (2)
I_{CC3}	V_{CC} Standby Current		Typ	20 µA	30 µA
I_{CC5}	Active Current Read While Write (Continuous Burst)	83 MHz	Typ	68 mA (1)	65 mA (2)
		104 MHz	Typ	72 mA (1)	71 mA (2)
		83 MHz	Max	78 mA (1)	70 mA (2)
		104 MHz	Max	78 mA (1)	76 mA (2)

Notes:

1. *This parameter was tested on NS-R with OE# low.*
2. *This parameter was tested on VS-R with OE# high.*

VS-R has a higher typical current draw from V_{CC} while the device is in standby mode, and during active burst read (burst length 8). This change in current should be noted, but the overall system impact is expected to be minimal.

Table 5. AC Characteristics

Parameter	Description	Min or Max	NS-R	VS-R
t_{AVDS}	AVD# Setup Time to CLK	Min	3.5 ns	4 ns (3.38 ns at 108 MHz)
t_{ACS}	Address Setup Time to CLK	Min	3 ns	4 ns (2.89 ns at 108 MHz)
t_{CES}	CE# Setup Time to CLK	Min	3.5 ns	4 ns (3.38 ns at 108 MHz)

5.1 AVD# Setup Time to CLK (t_{AVDS})

For synchronous reads, VS-R requires that AVD# is driven low at least 4 ns before the first rising clock edge. At comparable frequencies (83 MHz and 104 MHz), NS-R only requires 3.5 ns. When moving from NS-R to VS-R, the AVD# timing should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

5.2 Address Setup Time to CLK (t_{ACS})

For synchronous reads, VS-R requires that address lines are stable at least 4 ns before the first rising clock edge. At comparable frequencies (83 MHz and 104 MHz), NS-R only requires 3 ns. When changing from NS-R to VS-R, the address timing should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

5.3 CE# Setup Time to CLK (t_{CES})

For synchronous reads, VS-R requires that CE# is driven low at least 4 ns before the first rising clock edge. At comparable frequencies (83 MHz and 104 MHz), NS-R only requires 3.5 ns. When moving from NS-R to VS-R, the address timing should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

Table 6. Programming Performance

Parameter	Voltage	Typ or Max	NS-R	VS-R
Total 32-word Buffer Programming Time	V_{CC}	Typ	300 µs	450 µs
		Max	3000 µs	3000 µs
	V_{PP}	Typ	154 µs	288 µs
		Max	1540 µs	1540 µs

VS-R could take longer to program in certain cases, as shown in Table 6. Since the maximum times are equivalent, software timeouts should not need any adjustment.

6 Conclusion

The VS-R family offers an easy transition from the NS-R family. Some software changes may be needed to support the different Device ID and number of banks.

7 References

- S29NS-R MirrorBit Flash Family Data Sheet
- S29VS/XS-R MirrorBit Flash Family Data Sheet

Document History Page

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**	–	GJSW	09/03/2010	Initial version
*A	4980944	MSWI	10/30/2015	Updated in Cypress template
*B	5870064	AESATMP8	09/01/2017	Updated logo and Copyright.

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