AN98589

Migration from Cypress S29NS-P to S29VS-R

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AN98589 discusses the new features of S29VS-R MirrorBit® Flash family that offers a line of 1.8-Volt, burst mode, simultaneous read and write, Address and Data Multiplexed (ADM) products, and the considerations the designer should make when migrating from S29NS-P.

Contents

1 Introduction

The S29VS-R MirrorBit® Flash family offers a line of 1.8-Volt, burst mode, simultaneous read and write, Address and Data Multiplexed (ADM) products. This guide discusses the new features of S29VS-R and the considerations the designer should make when migrating from S29NS-P. In this migration guide, S29VS-R and VS-R refer to the 128 Mb and 256 Mb densities only. For migration from S29NS-R, please also see the application note, *Migrating from S29NS-R to S29VS-R* (Migrate_S29NS-R_to_S29VS-R_AN).

2 Feature Comparisons Summary

The following lists the items to consider when migrating from NS-P to VS-R:

- VS-R supports a new software sector protection method, compared with the Advanced Sector Protection features in NS-P
- VS-R features a Status Register, instead of DQ Polling on the NS-P
- Command Set Changes
  - Unlock cycles removed for all commands
  - Separate commands to suspend and resume program vs. erase operations
  - Single word program command removed
- VS-R is an 8-bank device, compared with the 16 banks of the NS-P
- VS-R has different Device ID values than the NS-P
- VS-R has significant changes in synchronous burst read
  - Only supports modes 8 or 16 word with wrap-around or continuous
  - Single Configuration Register, instead of two Configuration Registers in the NS-P
- VS-R has differences in Electrical Specifications

- Hardware Migration Considerations
  - VS-R has no WP# pin
  - Package pin-outs for 128 Mb and 256 Mb densities only differ by WP#

Table 1. Feature Comparisons

Key Features	NS-P	VS-R
Technology	MirrorBit	MirrorBit
Process Node	90 nm	65 nm
Densities	128 to 512 Mb	128 and 256 Mb
Data Bus Width	16-bit (Word)	16-bit (Word)
Bus Interface	ADM	ADM
VCC	1.70V to 1.95V	1.70V to 1.95V
Temperature Range	Wireless (-25°C to +85°C)	Wireless (-25°C to +85°C) Industrial (-40°C to +85°C)
Common Flash Interface (CFI)	Yes	Yes
Burst Frequency Order Options	66 / 83 MHz	83 / 104 / 108 MHz
Burst Length (linear, words)	8 / 16 / 32 with or without wrap-around / continuous	8 / 16 with wrap-around / continuous
Burst mode can be automatically activated	Yes	No
Data Transfer Flow Control	Yes (RDY)	Yes (RDY)
Sector Erase Architecture	32 KB small sectors, 128 KB large sectors	32 KB small sectors, 128 KB large sectors
Boot Sector Architecture	NS128P/NS256P: top	VS128/256RxxBHW00: top
	NS512P: uniform	VS128/256RxxBHW01: bottom
Banks	16	8
Command Set	Unlock cycles	Reduced (no unlock cycles)
DQ Polling	Yes	No
Status Register	No	Yes
Write Buffer Programming	64-Byte Write Buffer	64-Byte Write Buffer
Single Word Programming	Yes	No
Program Suspend / Resume	Yes	Yes
Erase Suspend / Resume	Yes	Yes
Low VCC Write Inhibit	Yes	Yes
Hardware Sector Protection	WP# and VPP pins	VPP pin
Software Sector Protection	Advanced Sector Protection (PPB, DYB, password)	Sector Lock Range, Sector Lock/ Unlock
Secure Silicon Region	256 Bytes factory locked	256 Bytes factory locked
	256 Bytes customer lockable	256 Bytes customer lockable
Program-Erase Endurance	100,000 cycles per sector (typical)	100,000 cycles per sector (typical)
Data Retention	20-year (typical)	10-year (typical)
Discrete Packages	NS128P/NS256P: 44-ball, 0.50 mm pitch FBGA (Pb-free)	44-ball, 0.50 mm pitch FBGA (Low-Halogen, Pb-free)
	NS512P: 64-ball, 0.50 mm pitch FBGA (Pb-free)	
Discrete Package Sizes (mm)	8.0 x 9.2, 6.2 x 7.7	6.2 x 7.7

3 Software Sector Protection

The VS-R family features a new method for software sector protection. The NS-P family supports Advanced Sector Protection (ASP), including Persistent Protection Bits (PPBs), Dynamic Protection Bits (DYBs), and Password Protection. Instead of ASP, VS-R supports new commands Sector Lock, Sector Unlock, and Sector Lock Range.

When the VS-R is first powered up, all sectors are unlocked. Issuing the Sector Lock command will lock all sectors in the device. Until power is cycled, only one sector at a time can be unlocked using the Sector Unlock command. Issuing the Sector Lock Range command will protect the selected sectors from being unlocked with the Sector Unlock command until power is cycled.

Table 2. New VS-R Sector Protection Commands

Command Sequence	Cycles	First		Second		Third		Fourth	
		Word Address	Data	Word Address	Data	Word Address	Data	Word Address	Data
Sector Lock	3	555h	60h	2AAh	60h	SLA (A6 = 0)	60h		
Sector Unlock	3	555h	60h	2AAh	60h	SLA (A6 = 1)	60h		
Sector Lock Range	4	555h	60h	2AAh	60h	SLA	61h	SLA	61h

Legend
SLA = Sector Lock Address

The NS-P Autoselect command can be used to check whether a particular sector is locked. VS-R does not provide this information in the ID / CFI address space. Refer to the VS-R data sheet for a full explanation of this feature.

4 Status Register

The NS-P family supports DQ Polling for software to detect the status of embedded operations. Instead of DQ Polling, VS-R supports a Status Register. The Status Register content overlays the sector selected by the Status Register Read command.

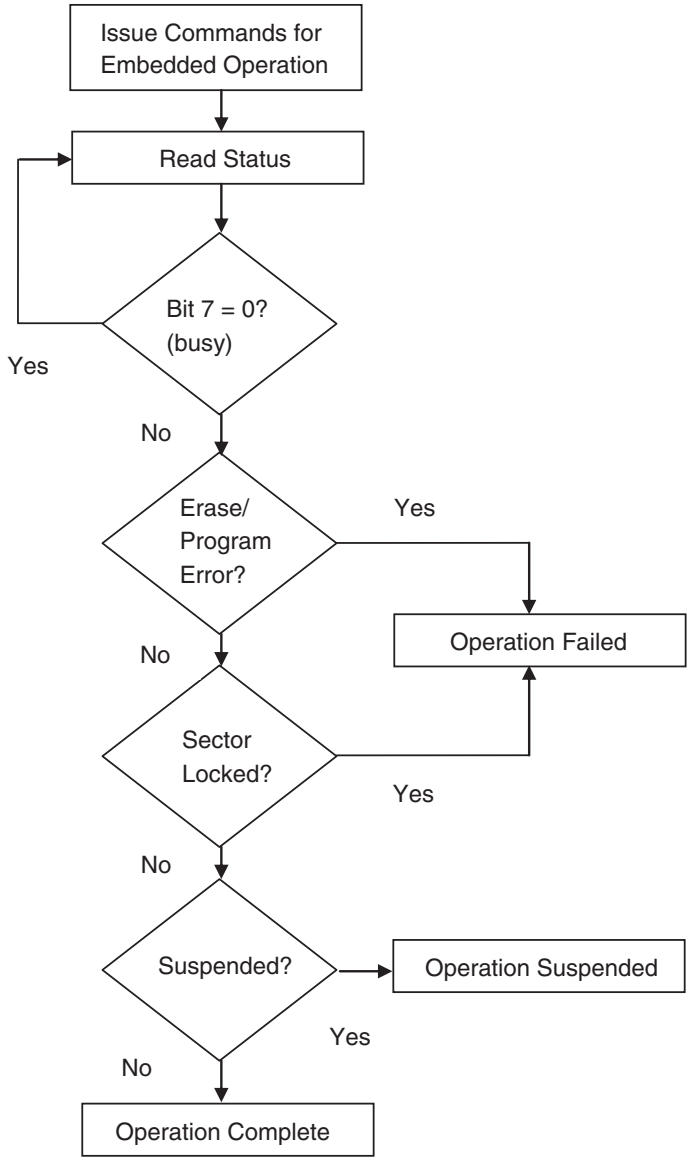
The Status Register contents are available for a single asynchronous read, or a single synchronous burst, after the Status Register Read command is issued. This command must be issued before each read of the status. Refer to the VS-R data sheet for a full explanation of this feature.

The Cypress Low Level Driver (LLD) provides software examples for both DQ Polling and Status Register polling. The LLD can be downloaded from the Cypress web site (www.cypress.com).

Table 3. VS-R Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Overall Device Ready Bit	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	Reserve	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
0 Device Busy	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	0 Op. in addressed bank
0 Device Busy							1 No op. in addressed bank
1 Device Ready	0 No erase in suspend	0 Erase Successful	0 Program Successful	x	0 No program in suspend	0 Sector not locked during op.	0 No active op.
1 Device Ready	1 Erase in Suspend	1 Erase Error	1 Program fail	x	1 Program in suspend	1 Sec locked error	1 Invalid

Figure 1. VS-R Status Register Polling



5 Command Set Changes

The VS-R family has significant command set changes from the NS-P family. Where the NS-P requires unlock cycles for most commands, these are removed from the VS-R commands. The VS-R does not support the Unlock Bypass Mode and the Single Word Program command. The Write Buffer Program command can be used to program individual words, as needed.

The NS-P provides a single Suspend command for both program and erase operations. To avoid confusion about the state of the device, the VS-R provides separate Program Suspend and Erase Suspend commands. Likewise, the Resume command was separated for program and erase. Refer to the VS-R data sheet for a full explanation of the available commands.

The Cypress Low Level Driver (LLD) provides software examples for both command sets. The LLD can be downloaded from the Cypress web site (www.cypress.com).

Table 4. VS-R Suspend/Resume Commands

Command Sequence	Cycles	Address	Data
Program Suspend	1	X	51h
Program Resume	1	SA	50h
Erase Suspend	1	X	B0h
Erase Resume	1	SA	30h

Legend
X = Don't care *SA = Address bits sufficient to select a sector*

6 Flash Memory Array

The VS-R is an 8-bank device, compared with the 16 banks of the NS-P. The sector sizes are the same for both families. The NS512P has uniform sector sizes, while the NS128P and NS256P have top boot sectors. The VS128R and VS256R are both available with top or bottom boot sectors. These differences in bank and sector architecture may require software changes. Refer to the device data sheets for memory address maps.

Table 5. NS256P to VS256R Bank/Sector Example

Format of Flash Image	NS256P			VS256R (Top Boot)		
	Bank	Sector Size	Number of Sectors	Bank	Sector Size	Number of Sectors
OS Image	0	128 KB	16	0	128 KB	32
	1	128 KB	16			
File System Volume	2	128 KB	16	1	128 KB	32
	3	128 KB	16			
	…	128 KB	16	…	128 KB	32
	…	128 KB	16			
	12	128 KB	16	6	128 KB	32
	13	128 KB	16			
	14	128 KB	16	7	128 KB	31
	15	128 KB	15			
Bootloader		32 KB	4		32 KB	4

In the example from Table 5, a product can be populated with either NS256P or VS256R. This Operating System image requires 2 MB of flash space, and fits into bank 0 on NS256P, but on VS256R, it requires a separate bank to enable Simultaneous Read/Write. In order to maintain a single flash image, 4 MB of space is set aside for the OS on both devices.

7 Device ID

The VS-R has a combined ID and Common Flash Interface (CFI) memory map. Access to Autoselect ID values and CFI information is enabled by two different commands:

- CFI Query (command 98h)
- Autoselect (command 90h)

Commands 90h and 98h are both called ID/CFI Entry in the VS-R data sheet since they enable a combined memory space. Just like NS-P, the VS-R requires the ID/CFI Exit command (F0h) to exit this memory space and access the Flash memory array. Autoselect with unlock cycles can be used with VS-R to check the Device ID, but it is not backwards compatible. The NS-P Autoselect command can be used to check whether a particular sector is locked. VS-R does not provide this information in the ID / CFI address space.

Table 6. Autoselect Entry with Unlock Cycles

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle1	Write	BA+AAAh	BA+555h	AAh
Unlock Cycle2	Write	BA+555h	BA+2AAh	55h
Autoselect Command	Write	BA+AAAh	BA+555h	90h

Legend
BA = Address bits sufficient to select a bank

Table 7. VS-R ID/CFI Entry Command

Cycle	Operation	Byte Address	Word Address	Data
ID/CFI Entry Command	Write	SA+XAAh	SA+X55h	90h or 98h

Legend
X = Don't care
SA = Address bits sufficient to select a sector

Table 8. Autoselect ID Codes

Description	NS256/128P		VS256/128R	
	Word Offset	Data	Word Offset	Data
Manufacturer ID	(BA) + 00h	0001h	(SA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	317Eh (NS256P) 327Eh (NS128P)	(SA) + 01h	007Eh (VS256R) 007Eh (VS128R)
Device ID, Word 2	BA + 0Eh	3141h (NS256P) 3243h (NS128P)	SA + 0Eh	0064h (VS256R Top) 0066h (VS256R Bottom) 0063h (VS128R Top) 0065h (VS128R Bottom)
Device ID, Word 3	BA + 0Fh	3100h (NS256P) 3200h (NS128P)	SA + 0Fh	0001h (VS256R) 0001h (VS128R)
Indicator Bits	BA + 07h	**DQ15 - DQ8 = Reserved** **DQ7 - Factory Lock Bit:** 1 = Locked, 0 = Not Locked **DQ6 - Customer Lock Bit:** 1 = Locked, 0 = Not Locked **DQ5 - Handshake Bit:** 1 = Reserved, 0 = Std Handshake **DQ4 & DQ3 - WP# Protection Boot Code:** 01 = WP# protects the top boot sectors **DQ2 - DQ0 = Reserved**	SA + 07h	**DQ15 - DQ8 = Reserved** **DQ7 - Factory Lock Bit:** 1 = Locked, 0 = Not Locked **DQ6 - Customer Lock Bit:** 1 = Locked, 0 = Not Locked **DQ5 - DQ0 = Reserved**

8 Synchronous Burst Read

The VS-R supports synchronous burst read, but it does not support as many burst read modes as the NS-P. Table 9 highlights the modes supported. Refer to the VS-R data sheet for a full explanation of the synchronous burst read mode.

Table 9. Synchronous Burst Read Mode

Burst Read Mode	Supported in NS-P?	Supported in VS-R?
Continuous	Yes	Yes
8-word with wrap-around	Yes	Yes
16-word with wrap-around	Yes	Yes
32-word with wrap-around	Yes	No
8-word without wrap-around	Yes	No
16-word without wrap-around	Yes	No
32-word without wrap-around	Yes	No
Burst mode can be automatically activated	Yes	No

The VS-R has a single 16-bit Configuration Register. The NS-P has two 16-bit Configuration Registers. The VS-R Configuration Register must be programmed with the Write Buffer Program command, while the NS-P Configuration Register must be programmed with the Set Configuration Register Command. Refer to the VS-R data sheet for a full explanation of the Configuration Register.

Table 10. Program NS-P Configuration Register

Address	Data	Description
SA+555h	AAh	Unlock Cycle 1
SA+2AAh	55h	Unlock Cycle 2
SA+555h	D0h	Configuration Register Entry
SA+X00h	CR	Set CR0
SA+X01h	CR	Set CR1
X	F0h	Configuration Register Exit

Legend
X = Don't care *CR = Configuration Register Data*
SA = Address bits sufficient to select a sector

Table 11. Program VS-R Configuration Register

Address	Data	Description
SA+555h	D0h	Configuration Register Entry
SA+555h	25h	Write Buffer Load
SA+2AAh	0	One Word
SA	CR	Configuration Register Data
SA+555h	29h	Buffer to Flash
X	F0h	Configuration Register Exit

Legend
X = Don't care *CR = Configuration Register Data*
SA = Address bits sufficient to select a sector

Table 12. Configuration Register Differences Between NS-P and VS-R

CR Bit	Function		Setting	
	NS-P	VS-R	NS-P	VS-R
CR1.15 - CR1.5	Reserved	N/A	1 = Default	N/A
CR1.4	Output Drive Strength	N/A	0 = Full Drive (Default) 1 = Half Drive	N/A
CR1.3 - CR1.1	Reserved	N/A	1 = Default	N/A
CR1.0	Wait State (with CR0.13-11)	N/A	Detail see data sheet	N/A
CR0.15	Reserved	Device Read Mode	0 = Reserved (Default) 1 = Reserved	0 = Synchronous Read Mode 1 = Asynchronous Read Mode (Default)
CR0.14	Reserved	Wait State	0 = Reserved (Default) 1 = Reserved	Detail see data sheet
CR0.13 - CR0.11	Wait State (with CR1.0)	Wait State	Detail see data sheet	Detail see data sheet
CR0.7	Reserved	Output Drive Strength	0 = Reserved 1 = Reserved (Default)	0 = Full Drive (Default) 1 = Half Drive
CR0.4	RDY Function	Reserved	0 = RDY (Default) 1 = Reserved	0 = Reserved (Default) 1 = Reserved
CR0.3	Burst Wrap Around	Reserved	0 = No Wrap Around Burst 1 = Wrap Around Burst (Default)	0 = Reserved 1 = Reserved (Default)
CR0.2-CR0.0	Burst Length	Burst Length	000 = Continuous (Default) 010 = 8-Word Linear burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst All other bit settings are reserved	000 = Continuous (Default) 010 = 8-Word Linear Burst Wrap Around 011 = 16-Word Linear Burst Wrap Around All other bit settings are reserved

9 Hardware Sector Protection

The VS-R does not have a WP# pin, which can be used to lock specific sectors for the NS-P. The VS-R can lock all sectors with the VPP pin, similar to NS-P. Refer to device data sheets for a full explanation of the hardware data protection methods.

10 Electrical Specification Differences

Electrical considerations for porting from NS-P to VS-R are described below. Since there are several differences between burst read on the NS-P and the VS-R, burst read current and timings are not discussed here. Please refer to the device data sheets for a detailed description of electrical specifications.

Table 13. DC Characteristics

Parameter	Description	Source	Min / Typ / Max	NS-P	VS-R
I_{CC1}	V_{CC} Active Asynchronous Read Current (tested at 10 MHz)	V_{CC}	Max	80 mA	60 mA
I_{CC2}	V_{CC} Active Write Current	V_{CC}	Typ	<20 mA	30 mA
I_{CC3}	V_{CC} Standby Current	V_{CC}	Typ	20 µA	30 µA
			Max	70 µA	40 µA
I_{CC6}	V_{CC} Sleep Current	V_{CC}	Typ	5 µA	20 µA
I_{PP}	Accelerated Program Current	V_{CC}	Typ	<15 mA	25 mA
			Max	20 mA	28 mA
V_{LKO}	Low V_{CC} Lock-out Voltage	–	Min	–	1.0V
			Max	1.4V	1.1V

VS-R has a higher current draw from V_{CC} in some situations. This change in current should be noted, but the overall system impact is expected to be minimal.

VS-R has a slightly lower lockout voltage than NS-P. Since systems should be designed for a minimum operating V_{CC} of 1.7V with either flash family, this change in lockout voltage should have no negative impact.

Table 14. Capacitance, Single Die and Package

Parameter	Description	Min or Max	NS-P	VS-R
C_{IN}	Input Capacitance	Min	1.05 pF	2.0 pF
		Max	1.75 pF	6.0 pF
C_{OUT}	Output Capacitance	Min	1.50 pF	2.0 pF
		Max	2.50 pF	6.0 pF

VS-R has higher capacitance values than the NS-P. This increased capacitance can affect the slope of signals for read and write cycles, as well as V_{CC} ramp to the device. When changing from NS-P to VS-R devices, these waveforms should be checked to ensure the timing specifications are satisfied. Signal integrity simulations can be run with IBIS models, which are available at www.cypress.com.

Table 15. V_{CC} Power-up

Parameter	Description	Min or Max	NS-P	VS-R
t_{VCS}	V_{CC} Setup Time	Min	30 µs	300 µs
t_{VIOS}	V_{IO} Setup Time	Min	–	300 µs

The VS-R requires that RESET# is held low significantly longer after V_{CC} ramps up. When moving from NS-P to VS-R, the power-up waveforms should be checked. If the RESET# pin is not held low for at least 300 µs after V_{CC} ramps up, circuit changes may be needed to accommodate the new specification.

Table 16. AC Characteristics

Parameter	Description	Min or Max	NS-P	VS-R
t_{RC}	Read Cycle Time	Min	–	80 ns
t_{OE}	Output Enable to Output Valid	Max	9 ns	15 ns
t_{AVDO}	AVD# High to OE# Low	Min	–	4 ns
t_{WEA}	WE# Disable to AVD# Enable	Min	–	9.6 ns
t_{OEH} (data reads)	WE# Disable to OE# Enable	Min	0 ns	4 ns
t_{VLWH}	AVD# Disable to WE# Disable	Min	–	23.5 ns
t_{CR}	CE# Low to RDY Valid	Max	–	10 ns
t_{WEH}	OE# Disable to WE# Enable	Min	–	4 ns
t_{ESL}	Erase Suspend Latency	Min	20 µs	30 µs
t_{PSL}	Program Suspend Latency	Min	20 µs	30 µs

10.1 Read Cycle Time (t_{RC})

VS-R requires a minimum asynchronous read cycle of 80 ns. NS-P does not specify this requirement. When moving from NS-P to VS-R, the timing of back to back cycles should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

10.2 Output Enable to Output Valid (t_{OE})

VS-R provides read cycle output within 15 ns of OE# going low. NS-P provides valid output within 9 ns. When changing from NS-P to VS-R, devices and components reading from flash must now wait at least 15 ns before latching the data.

10.3 AVD# High to OE# Low (t_{AVDO})

For asynchronous reads, VS-R requires AVD# is driven high at least 4 ns before OE# goes low. Since NS-P does not have this requirement, it must be checked when moving to VS-R. The memory controller may need adjustment.

10.4 WE# Disable to AVD# Enable (t_{WEA})

VS-R requires AVD# is driven low at least 9.6 ns after a write cycle. NS-P does not specify this requirement. When moving from NS-P to VS-R, the timing of back to back cycles should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

10.5 WE# Disable to OE# Enable (t_{OEH})

For asynchronous data reads, VS-R requires OE# is driven low at least 4 ns after a write cycle. NS-P specifies 0ns for this parameter. When changing from NS-P to VS-R, the timing of back to back cycles should be checked to ensure this new requirement is satisfied. The memory controller may need adjustment.

10.6 AVD# Disable to WE# Disable (t_{VLWH})

For flash write cycles, VS-R requires WE# is driven high at least 23.5 ns after AVD# goes high. NS-P does not specify this requirement. When moving from NS-P to VS-R, the timing of write cycles should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

10.7 CE# Low to RDY Valid (t_{CR})

When the flash device is not chip selected, the RDY pin is tri-stated to High-Z. Once the device is selected for read or write, VS-R provides valid output on RDY within 10 ns of CE# going low. NS-P does not specify this parameter. When using VS-R, devices and components reading from the flash RDY pin must wait at least 10 ns before latching the value.

10.8 OE# Disable to WE# Enable (t_{WEH})

For flash write cycles, VS-R requires WE# is driven low at least 4 ns after OE# goes high. NS-P does not specify this requirement. When moving from NS-P to VS-R, the timing of back to back cycles should be checked to ensure this requirement is satisfied. The memory controller may need adjustment.

10.9 Erase Suspend Latency (t_{ESL})

After issuing an Erase Suspend Command, system software can read the device status to check if the erase operation was suspended or completed. VS-R requires a delay of at least 30us before reading the Status Register. NS-P requires a delay of only 20 µs before checking device status. When moving from NS-P to VS-R, a longer delay must be implemented.

10.10 Program Suspend Latency (t_{PSL})

After issuing an Program Suspend Command, system software can read the device status to check if the erase operation was suspended or completed. VS-R requires a delay of at least 30 µs before reading the Status Register. NS-P requires a delay of only 20 µs before checking device status. When moving from NS-P to VS-R, a longer delay must be implemented.

Table 17. Erase and Programming Performance (Sheet 1 of 2)

Parameter	Voltage	Typ or Max	NS-P	VS-R
128 KB Sector Erase Time With Pre-programming Included	V_{CC}	Typ	0.9s	1.3s
		Max	5.0s	5.5s
	V_{PP}	Typ	0.7s	1.3s
		Max	3.75s	5.5s
128 KB Sector Erase Time With Pre-programming Excluded	V_{CC}	Typ	0.8s	0.8s
		Max	3.5s	3.5s
	V_{PP}	Typ	0.8s	0.8s
		Max	3.5s	3.5s
32 KB Sector Erase Time With Pre-programming Included	V_{CC}	Typ	0.45s	0.6s
		Max	1.85s	3.5s
	V_{PP}	Typ	0.35s	0.6s
		Max	1.4s	3.5s

Table 17. Erase and Programming Performance (Sheet 2 of 2)

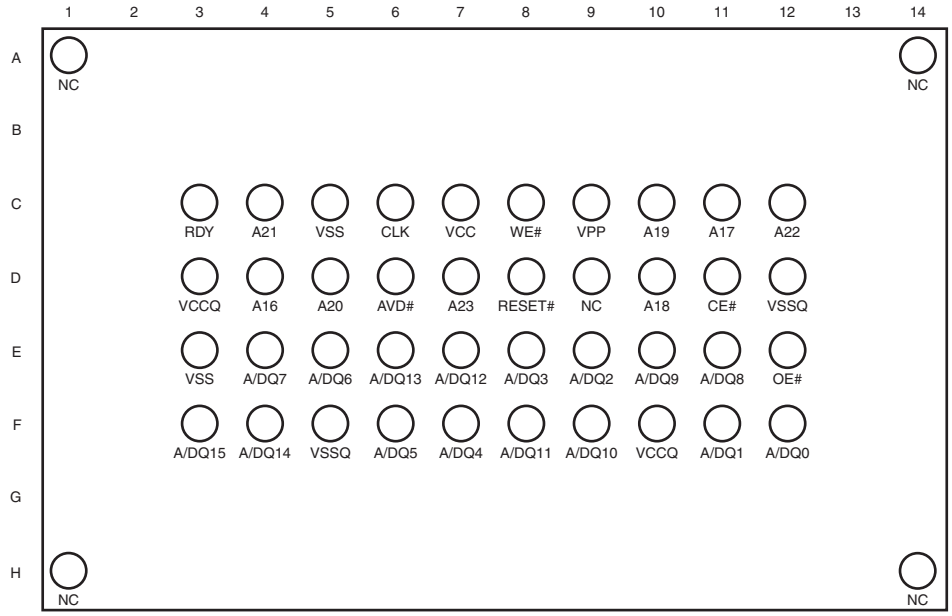
Parameter	Voltage	Typ or Max	NS-P	VS-R
32 KB Sector Erase Time With Pre-programming Excluded	V_{CC}	Typ	0.15s	0.35s
		Max	2.0s	2.0s
	V_{PP}	Typ	0.15s	0.35s
		Max	2.0s	2.0s
Total 32-word Buffer Programming Time	V_{CC}	Typ	300 µs	450 µs
		Max	3000 µs	3000 µs
	V_{PP}	Typ	192 µs	288 µs
		Max	1920 µs	1540 µs

VS-R could take longer to program and erase in certain cases, as shown in Table 17. Software time outs should be checked to ensure they allow the applicable maximum time.

11 Packaging

The VS-R and NS-P (128 Mb and 256 Mb densities) are available in 44-ball, 0.50 mm pitch FBGA packages. The difference is that the VS-R package has NC instead of WP# for ball D9.

Figure 2. VS-R Ball Out



12 Conclusion

The VS-R family offers several improvements over the NS-P family, specifically targeting customer usage.

- Simplified operation status
- Simplified command set
- Simplified sector protection

13 References

- S29NS-P MirrorBit Flash Family Data Sheet
- S29VS/XS-R MirrorBit Flash Family Data Sheet

Document History Page

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**	–	GJSW	09/14/2010	Initial version
*A	4980574	MSWI	10/30/2015	Updated in Cypress template
*B	5870084	AESATMP8	09/01/2017	Updated logo and Copyright.

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