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Spec Title: AN98582 - MIGRATION FROM MICRON(R) M25P/PE/PX AND N25Q TO CYPRESS S25FL1-K SPI FLASH FAMILY

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AN98582

Migration from Micron® M25P/PE/PX and N25Q to Cypress S25FL1-K SPI Flash Family

This application note provides conversion guidelines for migrating from the Micron M25P, M25PE, M25PX, and N25Q SPI series to the Cypress S25FL1-K SPI Flash Family. The document discusses the specification differences when migrating from M25P, M25PE, M25PX, and N25Q to S25FL1-K.

1 Introduction

This application note provides conversion guidelines for migrating from the Micron M25P, M25PE, M25PX, and N25Q SPI series to the Cypress S25FL1-K SPI Flash Family.

This application note is based on information available to date from data sheets and other applications notes publicly available from Cypress and Micron. Please refer also to the latest relevant specifications. The document discusses the specification differences when migrating from M25P, M25PE, M25PX, and N25Q to S25FL1-K.

2 Feature Comparison

Micron M25P, M25PE, M25PX, and N25Q products are well suited for migration to Cypress FL1-K products. Some of the reasons are compatible pinouts, packages, command set, and 4/64-kB block/sector structure. Cypress products support Dual I/O and Quad I/O modes, while Micron only has Dual I/O mode on the newer M25PX Family and Dual/Quad on the N25Q family.

The major differences are the Micron block protection scheme and different OTP handling, which requires some software changes when features are in use. Another difference in M25PE devices is the Page erase feature, which makes a software change necessary when it is used.

Table 1. Feature Comparison between Cypress S25FL1-K and Micron M25P/PE/PX and N25Q

	Micron M25P	Micron M25PE	Micron M25PX	Micron N25Q	Cypress S29FL1-K
Standard Pinout	X	X	X	X	X
Standard Packages	X	X	X	X	X
Standard Command Set	X	X	X	X	X
4/64-kB Block/Sector	Only 64 kB	X	X	X	X
Multi I/O	—	—	Dual I/O	Dual I/O - Quad I/O	Dual I/O - Quad I/O
Block Protection	BP (1)	BP / LR (1)	BP / LR (1)	BP / LR (1)	BP (1)
OTP	—	—	64 bytes	64 bytes	4 x 256-byte security registers
Page Erase	—	X	—	—	—

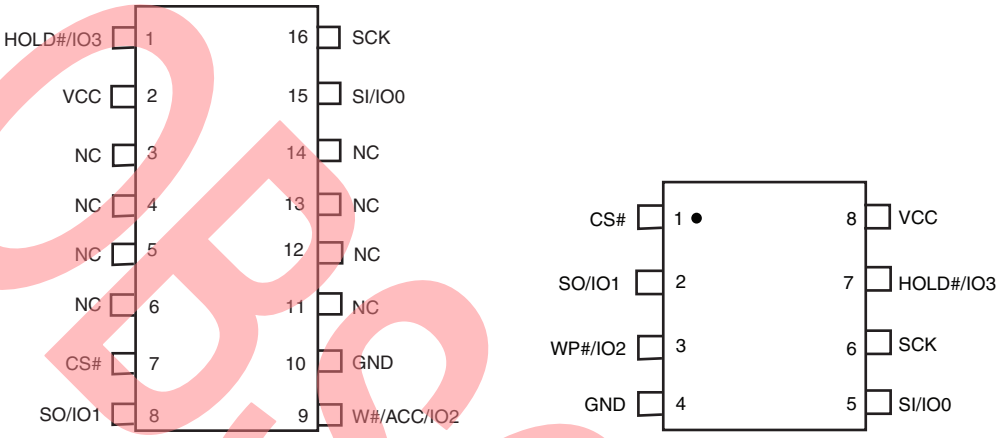
Notes:

1. *BP: Block protection bits, LR: Lock register.*
2. *—: Feature is not supported; X: Feature is supported.*

2.1 Packaging — All Densities

The most common packages for Micron and Cypress are the SOIC packages. The pinout is identical on the M25P, M25PX, and N25Q families, while the PE Series has Reset functionality instead of a HOLD function. FL1-K devices are not impacted in functionality when the system Reset# pin will be connected to the device HOLD# pin. Thus, this will allow a direct replacement without PCB redesign. Figure 1 shows those SOIC packages and pinouts. Please refer to the data sheets for detailed package information.

Figure 1. SOIC 150/208/300 mil Package and Pinout (16-pin and 8-pin Versions)



Note:

1. *On M25PE, Reset# replaces HOLD#.*

Table 2 and Table 3 summarize the available packages from Cypress and Micron.

Table 2. Cypress's Available Packages

	Cypress S25FL1-K		
	FL116K	**FL132K**	**FL164K**
SOIC8 150 mil	X	X	
SOIC8 208 mil	X	X	X
SOIC16 300 mil			X
USON 5x6	X	X	X
BGA 6x8	X	X	X

Note:

1. *X: Package is available.*

Table 3. Micron's Available Packages

	Micron M25P			Micron M25PE	Micron M25PX			Micron N25Q
	P16	**P32**	**P64**	**PE16**	**PX16**	**PX32**	**PX64**	**Q064**
SOIC8 150 mil	X				X			
SOIC8 208 mil	X	X		X	X	X		X
SOIC16 300 mil	X	X	X			X	X	X
USON 5x6	X	X		X	X	X		X
BGA 6x8					X	X	X	X

Note:

1. *X: Package is available.*

2.2 Sector Architecture

The sector architecture between Micron (M25P, M25PE, M25PX, and N25Q) and Cypress S25FL1-K can be considered almost identical. For those families, Micron states 64-kB sectors while offering sub-sectors of 4 kB (except M25P, which has only 64-kB sectors). However, both Micron and Cypress support the same flexible erase architecture of 4 kB, 64 kB, and chip erase operations (see Table 9, . *Command Set of S25FL1-K and M25P / M25PX / M25PE / N25Q* on page 6). M25PE devices have additionally Page Erase function. Page programming size of 256 byte is also identical. Table 4 shows a summary of the erase and programming granularity.

Table 4. Erase and Programming Granularity

	Micron M25P	Micron M25PE	Micron M25PX, N25Q	Cypress S29FL1-K
Sector Size	64 kB	4 kB, 64 kB	4 kB, 64 kB	4 kB, 64 kB
Erase Size	64 kB, chip erase	256 byte, 4 kB, 64 kB, chip erase	4 kB, 64 kB, chip erase	4 kB, 64 kB, chip erase
Page Prog. Size	256 bytes	256 bytes	256 bytes	256 bytes

2.3 Sector Protection

Both Cypress's FL1-K and Micron's M25P / M25PE / M25PX / N25Q offer very similar Sector Protection based on Block Protect Bits (BP2, BP1, BP0). Therefore, there is no software change required when migrating to the FL1-K. Using BP bits, all, none, or a portion of the memory array can be protected from Program and Erase instructions. The BP Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register SR1 (SR1[4], SR1[3], SR1[2]) that provide Write Protection control and status.

The factory default setting for the Block Protect Bits is 0 (none of the array is protected). BP bits can be set using the Write Status Register Instruction. The non-volatile Top/Bottom bit (TB) controls if the BP Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array. The non-volatile Sector/Block Protect bit (SEC) on S25FL1-K devices controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array.

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register SR2 (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed.

The TB, SEC, and CMP Bits functionality is not available on M25P and M25PE series devices. M25PX supports only TB. N25Q supports TB and SEC but no CMP. Please refer to the Cypress data sheet for the valid combinations. Table 5 shows the Cypress sector protection. Please refer also to the status register handling.

Additionally, Micron devices M25PE / M25PX / N25Q offer a sector based Protection which makes software changes necessary when used.

For those devices, every physical 64-kB sector of the device has a corresponding two-bit Sector Protection Register, “Write lock bit” and “Lock down bit” that is used to control the software protection of a sector.

Table 5. Status Register Memory Protection (CMP = 0)

Status Register (1)					Migration from Micron® M25P/PE/PX and N25Q to Cypress S25FL1-K SPI Flash Family (16-Mbit) Block Protection (CMP=0) (2)			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	31	1F0000h – 1FFFFFh	64 kB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128 kB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h – 1FFFFFh	256 kB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h – 1FFFFFh	512 kB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h – 1FFFFFh	1 MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2 MB	All
1	0	0	0	1	31	1FF000h – 1FFFFFh	4 kB	Upper 1/512
1	0	0	1	0	31	1FE000h – 1FFFFFh	8 kB	Upper 1/256
1	0	0	1	1	31	1FC000h – 1FFFFFh	16 kB	Upper 1/128
1	0	1	0	X	31	1F8000h – 1FFFFFh	32 kB	Upper 1/64
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/512
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/256
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/128
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/64

Notes:

1. *X = don't care.*
2. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*
3. *The Complement Protect bit (CMP SR2[6]) is a non-volatile read/write bit in the status register (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed. For instance, when CMP=0, a top 4-kB sector can be protected while the rest of the array is not; when CMP=1, the top 4-kB sector will become unprotected while the rest of the array become read-only.*

2.4 Status Register

The Status Register can be read to determine the device's ready/busy status as well as the status of many other functions such as Hardware Locking and Software Protection.

Cypress's Status Register 1 provides the same information as Micron's Status Register. The Status Register bits for functions that are not available on Micron Devices read 0, e.g: Bit 6 for setting of Sector protection granularity and Bit 5 for the Top / Bottom selector on PE devices. Default settings of Bits 5 and 6 result in same device behavior as Micron Devices.

Cypress FL1-K devices have two additional Status Registers (SR2 and SR3), which can be used to provide status on additional device features and to configure the burst wrap feature. The Write Status Register instruction allows the three Status Registers to be written in one command sequence. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 through 2 of Status Register-1), CMP, LB3, LB2, LB1, LB0, QE, SRP1 (bits 6 through 0 of Status Register-2) and W6, W5, W4 and LC (bits 6 through 0 of Status Register-3) can be written. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

Table 6, Table 7, and Table 8 show the Cypress status registers SR1, SR2 and SR3 respectively.

Table 6. Cypress FL1-K Status Register 1 (SR1)

Bits	Field Name	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors
5	TB	Top / Bottom Protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits		0	000b = No protection
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 7. Cypress FL1-K Status Register 2 (SR2)

Bits	Field Name	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	Non-volatile and volatile versions	0	0 = Normal Protection Map 1 = Inverted Protection Map
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected Security register 0 contains the Serial Flash Discoverable Parameters and is always programmed and locked by Cypress.
4	LB2			0	
3	LB1			0	
2	LB0			1	
1	QE	Quad Enable	Non-volatile and volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled
0	SRP1	Status Register Protect 1		0	0 = SRP0 selects whether WP# input has effect on protection of the status register 1 = SRP0 selects Power Supply Lock Down or OTP Lock Down mode.

Table 8. Cypress FL1-K Status Register 3 (SR3)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved		0	Reserved for Future Use
6	W6	Burst Wrap Length	Volatile	1	00 = 8-byte wrap. Data read starts at the initial address and wraps within an aligned 8-byte boundary 01 = 16-byte wrap. Data read starts at the initial address and wraps within an aligned 16-byte boundary. 10 = 32-byte wrap. Data read starts at the initial address and wraps within an aligned 32-byte boundary. 11 = 64-byte wrap. Data read starts at the initial address and wraps within an aligned 64-byte boundary.
5	W5			1	
4	W4	Burst Wrap Enable		1	0 = Wrap Enabled 1 = Wrap Disabled
3	Latency Control (LC)	Variable Read Latency Control		0	Defines the number of read latency cycles in Fast Read, Dual Out, Quad Out, Dual IO, and Quad IO commands. Binary values for 1 to 15 latency cycles. A value of zero disables the variable latency mode.
2				0	
1				0	
0				0	

3 Software Considerations

3.1 Micron M25P / M25PE / M25PX / N25Q versus S25FL1-K Command Set Comparison

M25P / M25PE / M25PX / N25Q and S25FL1-K have a wide range of common instructions (op-codes) in their command set.

While Cypress FL1-K devices have numerous additional commands that are related to Dual and Quad IO functionality and Erase/Program Suspend/Resume, Micron Devices have additional commands for the Sector based Protection (WRLR, RDLR). A further difference is the “Dual Input fast program” command which is available only on M25PX and N25Q devices and the “Page Write” and “Page Erase” command of M25PE devices.

Regarding status register handling, there is no need for a software change because SR1 of FL1-K can be written alone without including SR2 and SR3. CMP, QE and SPR1 bits will be cleared to 0, which results in same device behavior as Micron Devices.

Table 9 shows a comparison summary of the command set of a Cypress S25FL1-K device with the corresponding M25P / M25PE / M25PX / N25Q device families.

Table 9. Command Set of S25FL1-K and M25P / M25PX / M25PE / N25Q (Sheet 1 of 2)

Name	Description	S25FL1-K	M25P16	M25PE16	M25PX16	N25Q064
READ	Read Data (Single output)	03H	03H	03H	03H	03H
FAST_READ	Fast Read (Single output)	0BH	0BH	0BH	0BH	0BH
DOR	Dual Output Fast Read	3BH	—	—	3BH	3BH
QOR	Quad Output Fast Read	6BH	—	—	—	6BH
DIOR	Dual I/O Fast read	BBH	—	—	—	BBH
QIOR	Quad I/O Fast read	EBH	—	—	—	EBH
RDID	Read Identification (JEDEC)	9FH	9FH	9FH	9FH	9FH
	Read Mfg. ID and device ID	90H	—	—	—	—
	Set Burst with Wrap	77H	—	—	—	—
	Continuous Read Mode Reset	FFH	—	—	—	—
WREN	Write Enable	06H	06H	06H	06H	06H

Table 9. Command Set of S25FL1-K and M25P / M25PX / M25PE / N25Q (Sheet 2 of 2)

Name	Description	S25FL1-K	M25P16	M25PE16	M25PX16	N25Q064
WRDI	Write Disable	04H	04H	04H	04H	04H
	Write Enable for volatile status Reg.	50H	—	—	—	—
WRLR	Write Lock Register	—	—	E5H	E5H	E5H
RDLR	Read Lock Register	—	—	E8H	E8H	E8H
	4-kB Sector Erase	20H	—	20H	20H	20H
SE	64-kB Block Erase	D8H	D8H	D8H	D8H	D8H
BE	Bulk Erase	C7H, 60H	C7H	C7H	C7H	C7H
	Erase/Program Suspend	75H	—	—	—	75H
	Erase/Program Resume	7AH	—	—	—	7AH
PP	Page Program	02H	02H	02H	02H	02H
	Page Write	—	—	0AH	—	—
	Page Erase	—	—	DBH	—	—
DIFP	Dual Input fast program	—	—	—	A2H	A2H
QPP	Quad Page Programming	—	—	—	—	32H
DP	Deep Power Down	B9H	—	B9H	B9H	—
	Release from Deep Power Down	ABH	—	ABH	ABH	—
	Release from Deep Power Down / Read Electronic Signature	ABH	—	—	—	—
RDSR	Read Status Register 1	05H	05H	05H	05H	05H
	Read Status Register 2	35H	—	—	—	—
	Read Status Register 3	33H	—	—	—	—
WRR	Write Status Register	01H	01H	01H	01H	01H
	Read SFDP Register	5AH	—	—	—	5AH
	Read Security Registers	48H	—	—	—	—
	Erase Security Registers	44H	—	—	—	—
	Program Security Registers	42H	—	—	—	—
ROTP	Read OTP	—	—	—	4BH	4BH
POTP	Program OTP	—	—	—	42H	42H

3.2 OTP Related Commands

The OTP (One Time Programmable) area is a specific region that can be used to store a serial number or a security-oriented key. The M25PX and N25Q series have a 64-bytes OTP area that can be programmed by the user. The M25P and M25PE series do not offer an OTP region at all.

The S25FL1-K family provides four 256-byte Security Registers. Each register can be used to store information that can be permanently protected by programming One Time Programmable (OTP) lock bits in Status Register 2 (LB3, LB2, and LB1). Security register 0 is used by Cypress to store and protect the Serial Flash Discoverable Parameters (SFDP) information that is also accessed by the Read SFDP command.

The three additional Security Registers can be erased, programmed, and protected individually. These registers may be used by system manufacturers to store and permanently protect security or other important information separate from the main memory array.

Micron devices have two commands to manage the OTP area, as locking down is done with an additional byte during programming. For M25PX, to lock the OTP area, bits 0…3 of the additional 65th byte need to be programmed to logic 0. For N25Q, to lock the OTP area, only bit 0 of the additional 65th byte needs to be programmed to logic 0.

Table 10. OTP Commands

Name	Description	S25FL1-K	M25P16	M25PE16	M25PX16	N25Q064
	Read Security Registers	48H	—	—	—	—
	Erase Security Registers	44H	—	—	—	—
	Program Security Registers	42H	—	—	—	—
ROTP	Read OTP	—	—	—	4BH	4BH
POTP	Program OTP	—	—	—	42H	42H

4 Timing Considerations

4.1 Power-Up Timing

One of the most sensitive electrical specifications is the power-up timing needed to correctly initialize the device. Figure 2 and Table 11 show the power-up characteristics of both S25FL1-K and Micron devices.

Figure 2. Power-Up Timing Diagram

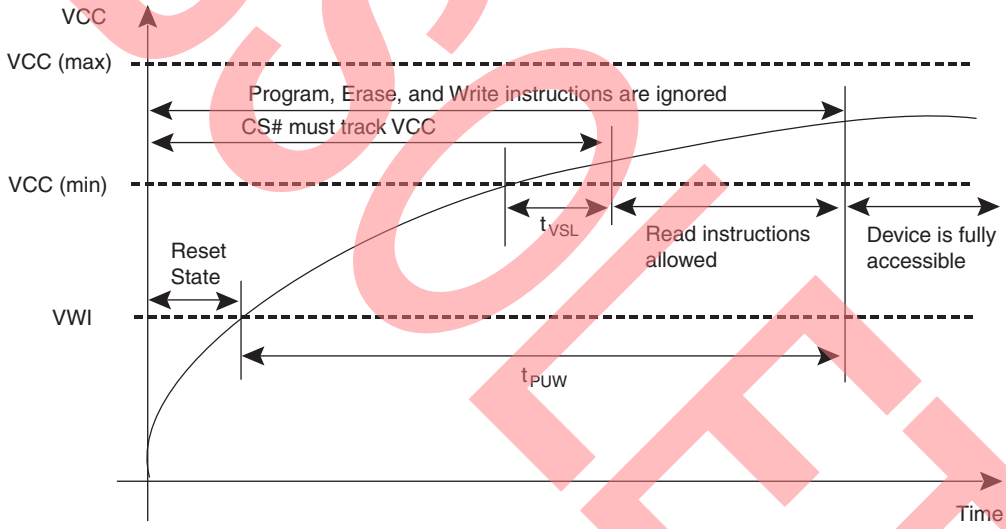


Table 11. S25FL1-K Power-Up Timing Requirements

Parameter	Symbol	M25P		M25PE		M25PX		N25Q		FL1-K		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	30	—	30	—	30	—	— (1)	— (1)	10	—	µs
Delay before Program or Erase	t_{PUW}	1	10	1	10	1	10	— (1)	— (1)	1	10	ms
Write Inhibit Threshold Voltage	t_{WI}	1.0	2.1	1.5	2.5	1.5	2.1	1.5	2.5	1.0	2.0	V

Notes:

1. *Those parameters are not described in the corresponding data sheets.*

It is important to note that the power-up parameters of the M25 family members are more restrictive. In particular, the delay before the system issues the first access (t_{VSL}) needs to be three times longer. Additionally, writes are inhibited already at 2.5V or 2.1V (N25Q and M25PX), while FL1-K allows writing down to 2.0V.

4.2 Data in Setup/Hold Time

Two AC timing parameters that are critical in SPI designs are Data In Setup Time and Data In Hold Time. They specify how long data needs to be valid before and after the rising edge of the clock signal, respectively. Almost all devices have the same timing. The minor different requirement should not be an issue in the design but may just need to be verified. Table 12 shows the Data in Setup/Hold timing characteristics for both S25FL1-K and Micron devices.

Table 12. Data in Setup/Hold Timing Characteristics

Parameter	Symbol	S25FL1-K	M25P	M25PE	M25PX	N25Q	Units
Data In Setup Time (Min)	t_{DVCH}/t_{DS}	2	5	2	2	2	ns
Data In Hold Time (Min)	t_{CHDX}/t_{DH}	5	5	5	5	3	ns

4.3 Further Timing Comparison

In general, the timing characteristics of both Micron and Cypress flash families are almost identical with just a little deviation.

One difference is that the Cypress FL1-K family has a much faster CS# deselect time. Given the 100 ns of M25P / M25PE devices or 80 ns of M25PX, FL1-K needs only 7 ns between Reads (vs 20 ns for N25Q) and 40 ns for Read after Writes (vs 50 ns for N25Q). There is no need to do any changes but it's important to note that the performance of the application can be increased easily here. Table 13 shows a comparison between S25FL1-K and Micron devices with regards to the various CS# deselect times.

Table 13. CS# deselect Time Characteristics

Parameter	Symbol	S25FL1-K	M25P	M25PE	M25PX	N25Q	Units
CS# deselect time between Reads (Min)	t_{SHSL1}/T_{CS1}	7	100	100	80	20	ns
CS# deselect time for Read after Writes (Min)	t_{SHSL2}/T_{CS2}	40	100	100	80	50	ns

5 Conclusion

Migrating from Micron M25P / M25PE / M25PX / N25Q families to the Cypress S25FL1-K is straightforward and requires minimal accommodation in regards to either system software or hardware. Similar pinout, packages, command set, and sector architecture makes this migration path really easy.

Additionally, once accommodations are made, if required, FL1-K flash will enable access to a wider range of SPI flash features and superior read throughput up to 54 Mbytes/s using Quad bit data path.

The major differences are the Micron block protection scheme and different OTP handling, which requires some SW changes when those features are in use.

Document History Page

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**	–	–	10/19/2012	Initial version.
*A	4928522	MSWI	09/21/2015	Updated to Cypress template.
*B	5798822	AESATMP8	07/05/2017	Updated logo and Copyright.
*C	6299527	BACD	09/04/2018	Obsolete document. Completing Sunset Review.

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