# Migration from Am29LV-D to S29JL-J/S29PL-J (64 Mb)

## About this document

### Scope and purpose

This application note discusses migration concerns when moving to S29JL064J or S29PL064J from AM29LV065D or AM29LV64xD flash.

## Table of contents

# 1 Introduction

The Am29LV065D and Am29LV64xD (Am29LV640D/Am29LV641D) flash devices manufactured with the 230-nm floating-gate technology are being migrated to next generation process technologies. The S29GL064N manufactured in 110 nm MirrorBit® process technology is the recommended default migration path from these legacy 64 Mbit AM29LV flash devices; however, certain applications may require faster access times, increased word or byte programming performance, or greater program/erase cycle endurance. If these characteristics are important, S29JL064J manufactured in 110 nm floating-gate technology offers an alternative migration path option. This application note discusses migration concerns when moving to S29JL064J or S29PL064J from AM29LV065D or AM29LV64xD flash.

While S29JL064J and S29PL064J maintain floating-gate technology compatibility, pin-to-pin backward compatibility is not maintained with the x8 only Am29LV065D or the x16 only Am29LV64xD and the Versatile I/O (VIO) pin feature is not supported. S29JL064J supports migration to a 48-pin TSOP and a 48-ball Fine-Pitch BGA package, and S29PL064J supports migration to a 48-ball Fine-Pitch BGA.

S29JL064J and S29PL064J are multi-bank devices that support Simultaneous Read/Write operations and top and bottom boot sectors for efficient parameter storage. S29PL064J also adds fast page mode read within an 8 Word page and a software command based sector protection method.

# 2 Architectural/feature comparison

Table 1 lists a feature comparison summary of the Am29LV065D and Am29LV64xD devices versus S29JL064J and S29PL064J is provided.

**Table 1 Feature comparison**

| Feature | Am29LV065D, Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|
| Technology | 230 nm floating gate technology | 110 nm floating gate technology | 110 nm MirrorBit technology |
| Sector architecture | 128 uniform sectors of 64 kbyte | 8 small boot sectors of 8 kB located at Top and Bottom.<br><br>126 uniform sectors of 64 kB<br><br>Organized in four Banks to enable simultaneous operation:<br><br>Bank 1 - 8 Mbit, 8 x 8 kB, 15 x 64 kB<br>Bank 2 - 24 Mbit, 48 x 64 kB<br>Bank 3 - 24 Mbit, 48 x 64 kB<br>Bank 4 - 8 Mbit, 15 x 64 kB, 8 x 8 kB | Same as JL064J except Banks 1, 2, 3, 4 called Banks A, B, C, D. |
| Access time, supply and I/O voltage range | 90 ns $V_{CC}$ 3.0V to 3.6V $V_{IO}$ 3.0V to 5.0V<br>120 ns $V_{CC}$ 3.0V to 3.6V $V_{IO}$ 3.0V to 5.0V<br>120 ns $V_{CC}$ 3.0V to 3.6V $V_{IO}$ 1.8V to 2.9V (LV065D)<br>100 ns $V_{CC}$ 3.0V to 3.6V $V_{IO}$ 1.8V to 2.9V | 55 ns, 60 ns, 70 ns, 90 ns<br>Full $V_{CC}$ 2.7V to 3.6V.<br>**No $V_{IO}$ support.** | 55 ns, 60 ns, 70 ns<br>Full $V_{CC}$ 2.7V to 3.6V.<br>**No $V_{IO}$ support.** |
| Bus architecture | (LV065D) x8<br>(LV64xD) x16 | x8 / x16 | x16 |
| Device ID | (LV065D) 93h<br>(LV64xD) 22D7h | (x8) 7Eh, 02h, 01h<br>(x16) 227Eh, 2202h, 2201h | 227Eh, 2202h, 2201h |
| Program operation | (LV065D) Single Byte programming<br>(LV64xD) Single Word programming | Single Byte or Word programming | Single Word programming |

## Architectural/feature comparison

| Feature | Am29LV065D, Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|
| Sector protection/ unprotection | HW Sector Group Protection<br>$V_{ID}$ on RESET# pin<br>Autoselect $V_{ID}$ on A9 pin | Same but first and last Sector Groups are subdivided into 8 x 8 kB and 3 x 64 kB (9 Sector Groups)<br>Addresses for balance of the 4 x 64 kB Sector Groups are unchanged | Same as JL064J and adds a software command based sector protection method not requiring RESET#=$V_{ID}$ |
| Temporary sector unprotection | $V_{ID}$ on RESET# pin | Same as Am29LV065D / Am29LV64xD except for first and last Sector Group sub Addresses | Same as JL064J |
| 256 bytes secure silicon sector region | Available | Same | Same |
| Data polling | Software detection of write/erase embedded algorithms completion | Same | Same |
| Ready/Busy# pin | Hardware detection of write/erase embedded algorithms completion<br>(LV641D TS048, SSO056: Not available) | Available with TS048 and VBK048 | Available with VBK048 |
| Erase suspend/resume | Command to suspend erase to program/read | Same. Also, simultaneous Read/Write operations possible in different banks | Same as JL064J |
| Command interface | Set of commands to perform various device operations | Fully backward compatible except Device ID | Same as JL064J |
| WP# pin | Available with LV64xD TS048 and SSO056. Protects top or bottom 64 kB sector | WP# pin to protect the two bottom and two top sectors (SA0, SA1, SA140, SA141) | Same as JL064J |
| Package summary | (LV065D) TS048, FBE063<br>(LV64xD) TS048, FBE063, SSO056, LAA064 | TS048, VBK048<br><br>TS048 pinout significantly different from x8 LV065D and does not support $V_{IO}$ while adding WP# to ACC pin<br><br>TS048 differs on 6 pins from LV641D and does not support $V_{IO}$ and adds WP# to ACC pin | VBK048 only<br><br>VBK048 ballout does not support x8 operation unlike the LV065D<br><br>VBK048 does not support $V_{IO}$ and adds WP# to ACC ball versus the LV640DU FBE063 |

**Architectural/feature comparison**

| Feature | Am29LV065D, Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|
| | | VBK048 ballout significantly different from x8 LV065D and does not support $V_{IO}$ while adding WP# to ACC ball<br><br>VBK048 does not support $V_{IO}$ and adds WP# to ACC ball versus the LV640DU FBE063 | |

## 2.1 DC and AC specification differences

**Table 2** lists the minor differences in the Absolute Maximum Ratings between the Am29LV065D and Am29LV64xD devices versus S29JL064J and S29PL064J.

**Table 2 Absolute maximum ratings comparison**

| Parameter | Description | Am29LV065D/ Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|---|
| WP#/ACC | Voltage with respect to ground | (ACC)<br>–0.5 V to +12.5 V | –0.5 V to +10.5 V | –0.5 V to +10.5 V |
| A9, OE#, RESET# | Voltage with respect to ground | –0.5 V to +12.5 V | (A9, RESET#)<br>–0.5 V to +12.5 V | –0.5 V to +13.0 V |

**Table 3** lists the minor differences in the DC characteristics between the Am29LV065D and Am29LV64xD devices versus S29JL064J and S29PL064J. The S29PL064J requires almost twice the VCC Active Read Current as the Am29LV065D, Am29LV64xD, or S29JL064J. Note the ranges for VHH and VID have been tightened for the S29JL064J and S29PL064J.

**Table 3 DC characteristics comparison**

| Parameter | Description | Am29LV065D/ Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|---|
| $I_{LR}$ | Reset leakage current | – | 35 µA | 35 µA |
| $I_{CC1}$ | $V_{CC}$ active read current @ 5 MHz | (Byte)<br>Typ: 9 mA<br>Max: 16 mA | (Byte / Word)<br>Typ: 10 mA<br>Max: 16 mA | (Word)<br>Typ: 20 mA<br>Max: 30 mA |
| $I_{CC2}$ | $V_{CC}$ active write current | Typ: 26 mA<br>Max: 30 mA | Typ: 15 mA<br>Max: 30 mA | Typ: 15 mA<br>Max: 25 mA |
| $V_{IH}$ | Input high voltage | Min: 0.7 x $V_{CC}$ | Min: 0.7 x $V_{CC}$ | Min: 2.0 V |
| $V_{HH}$ | Voltage for ACC program acceleration | Min: 11.5 V<br>Max: 12.5 V | Min: 8.5 V<br>Max: 9.5 V | Min: 8.5 V<br>Max: 9.5 V |
| $V_{ID}$ | Voltage for autoselect and temporary sector unprotect | Min: 8.5 V<br>Max: 12.5 V | Min: 11.5 V<br>Max: 12.5 V | Min: 11.5 V<br>Max: 12.5 V |
| $V_{OL}$ | Output low voltage | Max: 0.45 V | Max: 0.45 V | Max: 0.4 V |

### Architectural/feature comparison

| Parameter | Description | Am29LV065D/ Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|---|
| $V_{OH1}$ | Output high voltage | Min: 0.8 x $V_{IO}$ | Min: 0.85 x $V_{CC}$ | |
| $V_{OH2}$ | Output high voltage | | | Min: $V_{CC}$ – 0.2 V |
| $V_{LKO}$ | Low $V_{CC}$ lock-out voltage | Min: 2.3 V<br>Max: 2.5 V | Min: 1.8 V<br>Typ: 2.0 V<br>Max: 2.5 V | Min: 2.3 V<br>Max: 2.5 V |

Table 4 lists the minor differences in the AC characteristics between the Am29LV065D and Am29LV64xD devices versus S29JL064J and S29PL064J. The S29JL064J and S29PL064J have the same or better program and erase performance versus the Am29LV065D and Am29LV64xD devices.

**Table 4 AC characteristics comparison**

| Parameter | Description | Am29LV065D/ Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|---|
| $t_{DF}$ | Chip enable to output high-Z | Max: 30 ns | Max: 16 ns | Max: 16 ns |
| $t_{DF}$ | Output enable to output high-Z | Max: 30 ns | Max: 16 ns | Max: 16 ns |
| $t_{OH}$ | Output hold time from addresses, CE# or OE#, whichever occurs first | Min: 0 ns | Min: 0 ns | Min: 5 ns |
| $t_{READY}$ | RESET# low during embedded algorithm to read mode (CE# low) | Max: 20 µs | Max: 35 µs | Max: 20 µs |
| $t_{RPD}$ | RESET# low to standby mode | Min: 20 µs | Min: 35 µs | Min: 20 µs |
| $t_{WHWH1}$ | Programming operation | (LV065D)<br>Byte Typ: 5 µs<br>Byte Max: 150 µs<br><br>(LV64xD)<br>Word Typ: 11 µs<br>Word Max: 300 µs | Byte Typ: 6 µs<br>Byte Max: 150 µs<br><br>Word Typ: 6 µs<br>Word Max: 210 µs | Word Typ: 6 µs<br>Word Max: 100 µs |
| $t_{WHWH1}$ | Accelerated programming operation | (LV065D)<br>Byte Typ: 4 µs<br>Byte Max: 120 µs<br>(LV64xD)<br>Word Typ: 7 µs<br>Word Max: 210 µs | Typ: 4 µs<br>Max: 210 µs | Word Typ: 4 µs<br>Word Max: 60 µs |
| | Chip program time | (LV065D)<br>Byte Typ: 42 sec<br>Byte Max: 126 sec<br><br>(LV64xD)<br>Word Typ: 48 sec<br>Word Max: 144 sec | Byte Typ: 42 sec<br>Byte Max: 126 sec<br><br>Word Typ: 28 sec<br>Word Max: 84 sec | Word Typ: 25.2 sec<br>Word Max: 50.4 sec |

**Architectural/feature comparison**

| Parameter | Description | Am29LV065D/ Am29LV64xD | S29JL064J | S29PL064J |
|---|---|---|---|---|
| $t_{WHWH2}$ | Sector erase operation | Typ: 0.9 sec<br>Max: 15 sec | Typ: 0.5 sec<br>Max: 5 sec | Typ: 0.5 sec<br>Max: 2 sec |
| $t_{ESL}$ | Erase suspend latency | – | Max: 35 µs | Max: 35 µs |
| | Chip erase time | Typ: 115 sec | Typ: 71 sec | Typ: 71 sec<br>Max: 113.6 sec |

## 2.2 Command set

The S29JL064J and S29PL064J Command Sequences are fully software backward compatible with the Am29LV065D and Am29LV64xD except when reading the Device ID.

### 2.2.1 Device ID

S29JL064J (x8: 7Eh, 02h, 01h; x16:227Eh, 2202h, 2201h) and S29PL064J (227Eh, 2202h, 2201h) have three Read Cycle Device ID command sequences unlike the Am29LV065D (93h) and Am29LV64xD (22D7h) which have single Read Cycle Device ID command sequences.

## 2.3 CFI register differences

**Table 5** Lists the Common Flash Interface (CFI) register space differences between the Am29LV065D and Am29LV64xD devices versus S29JL064J and S29PL064J.

**Table 5 AC CFI differences**

| Address | Description | Am29LV640D/ AM29LV641D | Am29LV065D | S29JL064J | S29PL064J |
|---|---|---|---|---|---|
| 1Fh | Typical timeout per single word write $2^N$ µs | 0004h | 04h | 0003h | 0003h |
| 21h | Typical timeout per individual block erase $2^N$ ms | 000Ah | 0Ah | 0009h | 0009h |
| 22h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) | 0000h | 00h | 000Fh | 0000h |
| 23h | Max. timeout for word write $2^N$ times typical | 0005h | 05h | 0004h | 0004h |
| 28h | Flash device interface description (refer to CFI publication 100) | 0001h | 00h | 0002h | 0001h |
| 2Ch | Number of erase block regions within device | 0001h | 01h | 0003h | 0003h |
| 2Dh | Erase block region 1 information | 007Fh | 7Fh | 0007h | 0007h |
| 2Fh | Erase block region 1 information | 0000h | 00h | 0020h | 0020h |
| 30h | Erase block region 1 information | 0001h | 01h | 0000h | 0000h |

### Architectural/feature comparison

| Address | Description | Am29LV640D/ AM29LV641D | Am29LV065D | S29JL064J | S29PL064J |
|---|---|---|---|---|---|
| 31h | Erase block region 2 information | 0000h | 00h | 007Dh | 007Dh |
| 34h | Erase block region 2 information | 0000h | 00h | 0001h | 0001h |
| 35h | Erase block region 3 information | 0000h | 00h | 0007h | 0007h |
| 37h | Erase block region 3 information | 0000h | 00h | 0020h | 0020h |
| 44h | Minor version number, ASCII | 0033h | 31h | 0033h | 0033h |
| 45h | Address sensitive unlock | 0000h | 01h | 000Ch | TBD |
| 47h | Sector protect 00 = Not supported, X = Number of sectors per group | 0004h | 04h | 0001h | 0001h |
| 49h | Sector protect/unprotect scheme 04 = 29LV800A mode | 0004h | 04h | 0004h | 0007h |
| 4Ah | Simultaneous operation 00 = not supported, XX = Number of Sectors in bank | 0000h | 00h | 0077h | 0077h |
| 4Ch | Page mode type 00 = not supported, 01 = 4 word page, 02 = 8 word page | 0000h | 00h | 0000h | 0002h |
| 4Dh | ACC (Acceleration) supply Minimum bits 7–4 = Hex value in Volts, Bits 0–3 = BCD value in 100 mV | 00B5h | B5h | 0085h | 0085h |
| 4Eh | ACC (Acceleration) Supply Maximum | 00C5h | C5h | 0095h | 0095h |
| 4Fh | Top/bottom boot sector flag 00h = Uniform sector, no WP# control 04h = Uniform sector, WP# protects bottom sector 05h = Uniform sector, WP# protects top sector | 0000h | 00h | 0001h | 0001h |

# 3 Package migration and pinout differences

Am29LV065D and Am29LV64xD designs requiring or selecting a 48-pin TSOP package should migrate to the S29JL064J. Am29LV065D designs requiring a 48-pin Fine-Pitch BGA package should migrate to the S29JL064J. Am29LV64xD designs requiring a 48-pin Fine-Pitch BGA package can migrate to S29JL064J or S29PL064J.

Am29LV64xD designs using the 56-pin SSOP (SSO056) or 64-ball Fortified BGA (LAA064) will need to change the physical package by migrating to either the S29JL064J 48-pin TSOP or to S29JL064J or S29PL064J 48-pin Fine-Pitch BGA.

## 3.1 $V_{IO}$, versatileIO not supported

S29JL064J and S29PL064J do not support the $V_{IO}$ pin function for interfacing to devices with different voltage levels unlike the Am29LV065D and Am29LV64xD.

## 3.2 RD/BY#, ready/busy

S29JL064J and S29PL064J support the RD/BY# Ready/Busy pin function indicating whether an Embedded Algorithm is in progress or complete like the Am29LV065D and Am29LV640D 63-ball Fine-Pitch BGA but unlike the Am29LV641D 48-pin TSOP.

## 3.3 WP#, write protect

S29JL064J and S29PL064J support the WP# Write Protect pin function like the Am29LV065D and Am29LV641D but unlike the Am29LV640DU which lacks the WP# signal.

When WP#=$V_{IL}$ with S29JL064J and S29PL064J, the two bottom and two top 8 kB sectors are protected unlike WP#=$V_{IL}$ protecting the top or bottom 64 kB sector of the Am29LV065D and Am29LV641D.

## 3.4 Am29LV065D package migration pinout differences

The Am29LV065D is offered in x8 Byte optimized 48-pin TSOP and 63-ball Fine-Pitch BGA packages. Both the migration of the Am29LV065D 48-pin TSOP to the S29JL064J 48-pin TSOP and Am29LV065D 63-ball Fine-Pitch BGA to the S29JL064J 48-pin Fine-Pitch BGA require the majority of PCB footprint signals to be rerouted.

The S29JL064J 48-Ball Fine-pitch Ball Grid Array 8.15 x 6.15 mm package (VBK048) is smaller in physical size than the Am29LV065D 63-Ball Fine-Pitch BGA 11 x 12 mm package (FBE063) since the die is smaller and the corner balls are not required for package stability.

## 3.5 Am29LV64xD package migration pinout differences

### 3.5.1 Am29LV64xD 48-pin TSOP pinout differences

As shown in **Figure 1**, six signal pins on the Am29LV64xD 48-pin TSOP differ from the S29JL064J 48-pin TSOP. At a minimum, A19 and A21 will need to be rerouted.

Example:

For a x16 Word design, if pin 47 $V_{IO}$ is already connected to $V_{CC}$, no change is required and DQ15 should already be routed to pin 45. By electing to not support ACC and RD/BY#, the PCB rerouting changes are limited to A19 and A21.

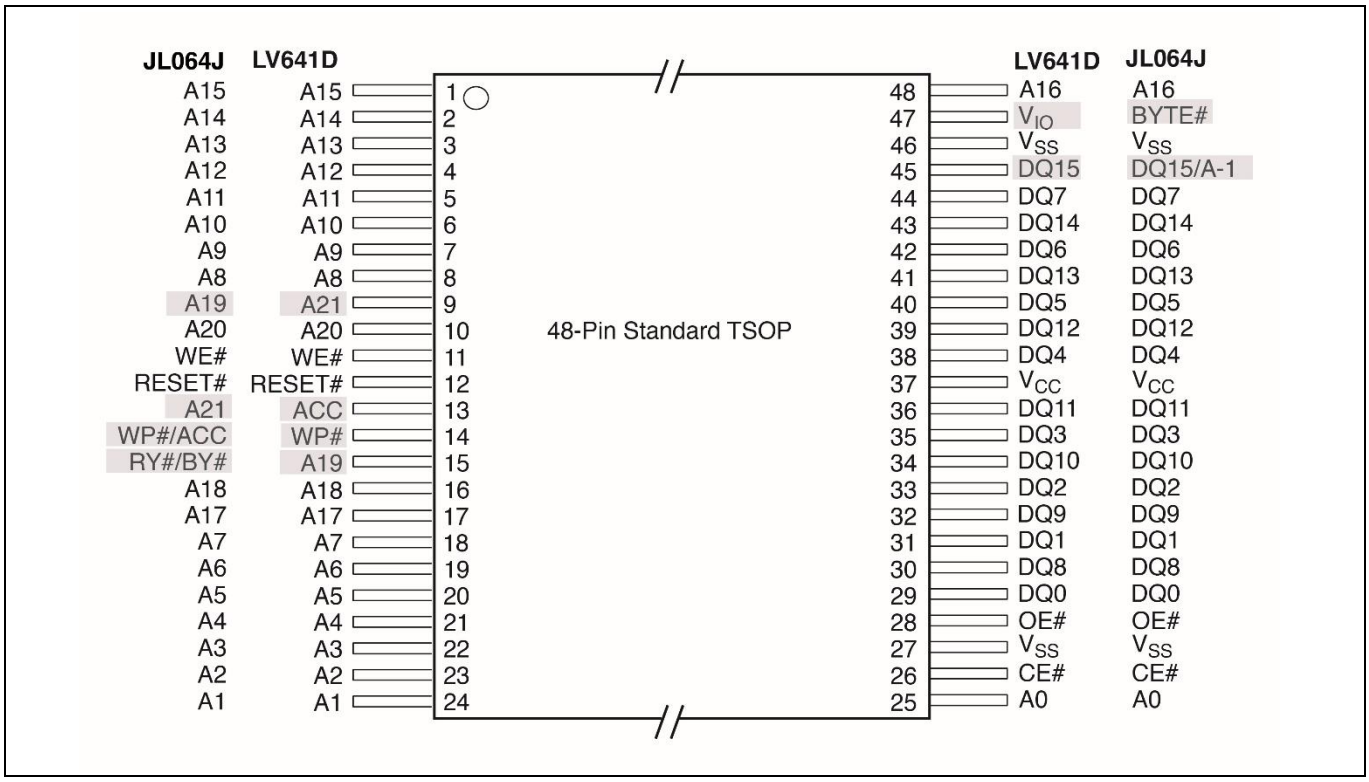


**Figure 1 PSoC Creator features**

### 3.5.2 Am29LV640DU 63-ball fine-pitch BGA ballout differences

The core 48 balls of the Am29LV640DU 63-ball Fine-Pitch BGA package have significant compatibility with the S29JL064J or S29PL064J 48-pin Fine-Pitch BGA. Since both the S29JL064J and S29PL064J die are smaller, the 15 corner balls of the Am29LV640DU 63-ball Fine-Pitch BGA 11 x 12 mm package (FBE063) are no longer required for package stability, and the S29JL064J and S29PL064J 48-pin Fine-Pitch BGA package (VBK048) size has been reduced to 8.15 x 6.15 mm.

As shown in **Figure 2**, signals on the Am29LV640DU Fine-Pitch BGA core 48 balls differ from both the S29JL064J and S29PL064J 48-pin Fine-Pitch BGA package. Am29LV640DU ball H7 is VIO unlike S29JL064J ball F6, BYTE#, or S29PL064J ball F6, NC (No Connect), since the S29JL064J and S29PL064J do not support VIO. Am29LV640DU ball D4 is ACC unlike both S29JL064J and S29PL064J ball B3 which multiplex WP# Write Protect with ACC.

## Package migration and pinout differences

Example:

No PCB changes will be required to drop the S29PL064J 48-pin Fine-Pitch BGA package onto an existing Am29LV640DU 63-ball Fine-Pitch BGA design if the $V_{IO}$ VersatileIO feature is not required and Am29LV640DU ball D4, ACC, is tied to $V_{CC}$.

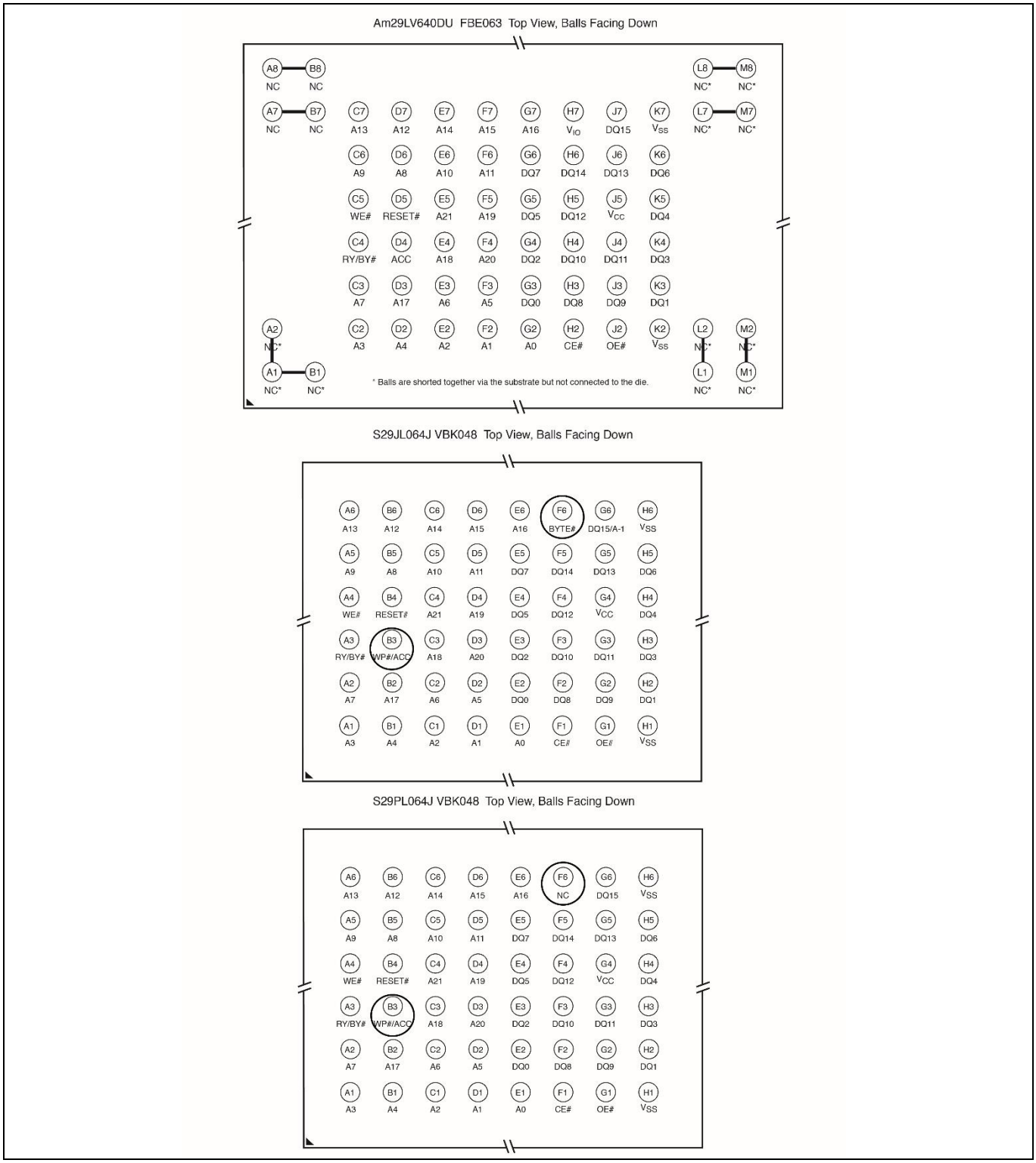


**Figure 2 Am29LV640DU FBE063 versus S29PL064J VBK048 package ballouts**

# 4 Design considerations

## 4.1 Sector architecture

S29JL064J and S29PL064J have eight 8 kB boot sectors located at both the top and bottom with one hundred twenty-six (126) 64 kB uniform sectors in between unlike the Am29LV065D and Am29LV64xD that have one hundred twenty-eight (128) 64 kB uniform sectors.

## 4.2 Bank architecture

S29JL064J and S29PL064J are organized in four Banks to enable simultaneous operation unlike the Am29LV065D and Am29LV64xD which have a single Bank. The S29JL064J and S29PL064J Bank Architecture is not a migration concern unless the software design is upgraded to leverage the ability to erase or program in one bank while reading from a different bank.

## 4.3 Hardware sector protection

### 4.3.1 Sector group protection

Both the S29JL064J and S29PL064J devices support hardware Sector Group Protection like the Am29LV065D and Am29LV64xD. However, the S29JL064J and S29PL064J devices permit independent Sector Protection control of the eight 8 kB boot sectors located at both the top and bottom using addresses A21–A12 along with the contiguous top and bottom three (3) 64 kB Sector Blocks using addresses A21–A15. The 30 Sector Groups in between the S29JL064J and S29PL064J top and bottom boot sectors and Sector Blocks use addresses A21-A17 for Sector Protection control like the Am29LV065D and Am29LV64xD.

### 4.3.2 Sector group unprotection

S29JL064J and S29PL064J support Sector Group Unprotection like the Am29LV065D and Am29LV64xD except for the independent control of top and bottom boot sectors and Sector Blocks as discussed in the **4.1 Sector architecture** section.

### 4.3.3 Temporary sector group unprotect

S29JL064J and S29PL064J support Temporary Sector Group Unprotection like the Am29LV065D and Am29LV64xD although the WP# pin can be used to protect the two bottom and two top 8 kB sectors versus the top or bottom 64 kB sector of the Am29LV065D and Am29LV641D during the Temporary Sector Group Unprotection mode.

## 4.4 RoHS

S29JL064J products are only offered in RoHS compliant Pb-free packages while the S29PL064J products are offered in RoHS compliant Pb-free packages as well as Standard packages like the Am29LV065D and Am29LV64xD.

## 4.5 First read after power reset

For the S29JL064J and S29PL064J devices, during the power up sequence, CE# should rise with VCC and must only be driven low after RESET# has gone high. CE# falling edge after RESET# is necessary to initiate the first read operation. If CE# is low through power up and the first read, the Host may latch erroneous data for the first read. In applications that do not control CE# adequately for the S29JL064J or S29PL064J, a weak pull-up resistor should be used to tie CE# to VCC.

# 5 References

- Am29LV065D Data Sheet (23544_C3)
- Am29LV640D/Am29LV641D Data Sheet (22366_C7)
- S29JL064J Data Sheet (S29JL064J_00)
- S29PL064J Data Sheet (S29PL-J_00)

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2011-03-30 | Initial release. |
| *A | 2018-04-17 | Updated to Cypress template.<br>Completing Sunset Review. |
| *B | 2021-06-30 | Updated to Infineon template. |

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