AN98567

Understanding Load Capacitance and Access Time

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AN98567 examines how capacitive load added by placing multiple devices on the same trace affects read access time.

1 Introduction

Sometimes a design engineer can be tempted to place multiple devices on the same trace. This is especially true if there is no defined bus standard and reducing costs is critical. However, each of these devices will add its input capacitance to the trace which can cause problems. This paper examines how this added capacitive load effects read access time.

2 Total Capacitive Load

The total capacitive load is defined as the sum of the input capacitance of all the other devices sharing the trace. Note that the capacitance of the device driving the trace is not included. If the total load capacitance on a trace exceeds the output capacitance specification of the driving device then this total load capacitance is defined as 'excessive'. Typically a device input is specified with about 10 [pf] of capacitive load.

3 Non-Excessive Output Delay

If the total capacitive load is not excessive then the device's data sheet AC parameters should be used to determine the output delay of the device.

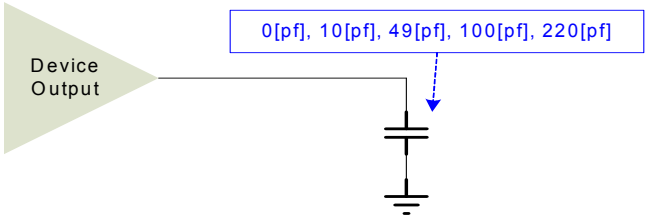
4 ‘Excessive’ Output Delay

If the total load capacitance is excessive there is no guarantee for the operation of the device. However, usually the effect of the excessive load capacitance will be to slow the voltage transitions on the trace. This delay will roughly increase with the capacitance. Note that signal integrity problems could also arise from the addition of the devices to the trace.

5 Measurement of Voltage Transition Time verses Load Capacitance

Measurements of voltage transition time were taken for various load capacitances. The voltage transition time is defined as the time from the initial output voltage change to the opposite logical voltage threshold. In Figure 1 a popular CPLD device drives a 2.5 [mm] (~ 1 inch) trace. The trace has no stubs. The following load capacitance values were used: 0 [pf], 10 [pf], 49 [pf], 100 [pf], and 220 [pf].

Figure 1. Test Setup



The following figures show a rising voltage observed at the end of the trace. These figures show that as load capacitance increases the rise time slows. Figure 2 shows that it takes about 0.5 [ns] to transition from 0.0 [V] to +2.4 [V] (logic level high).

Figure 2. Signal Transition with No Load

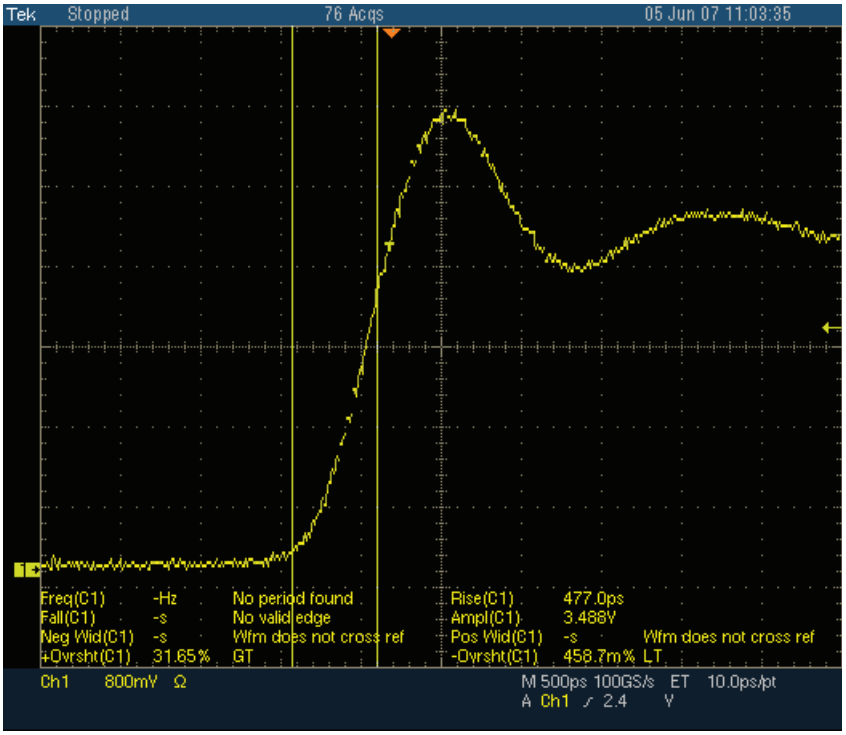


Figure 3 shows that with a 10 [pf] load capacitor 1.2 [ns] is needed to transition from 0.0 [V] to logic level high.

Figure 3. Signal Transition with 10 [pf] Load

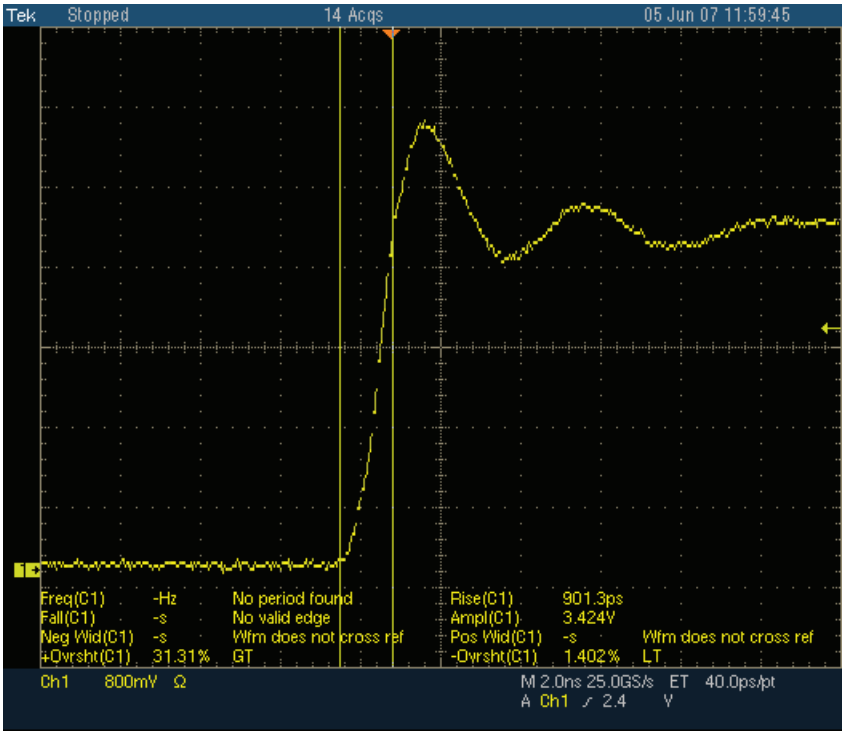
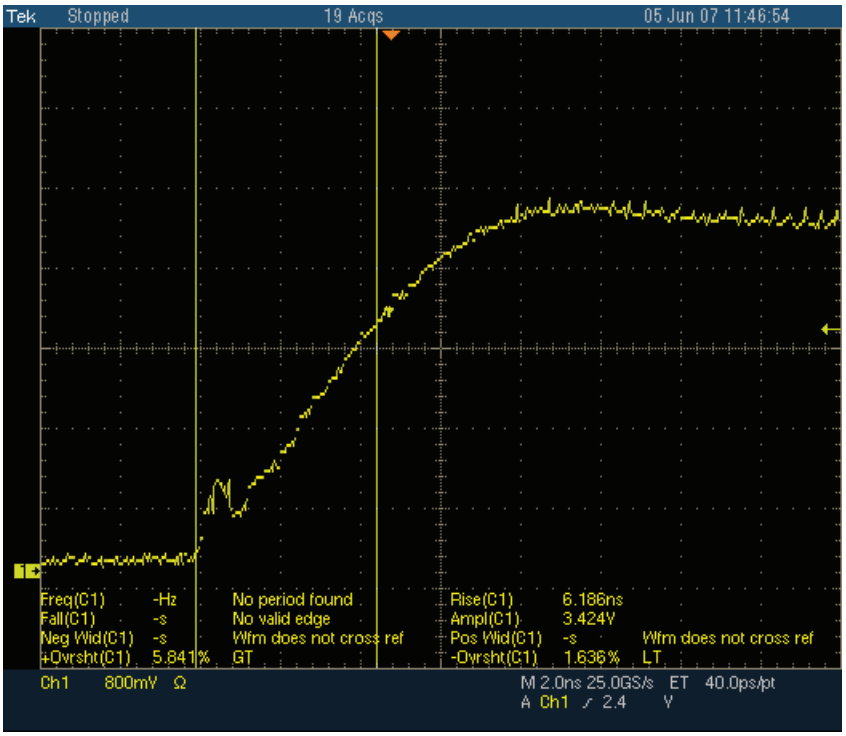


Figure 4 shows that with a 100 [pf] load capacitor 4.4 [ns] is needed to transition from 0.0 [V] to logic high.

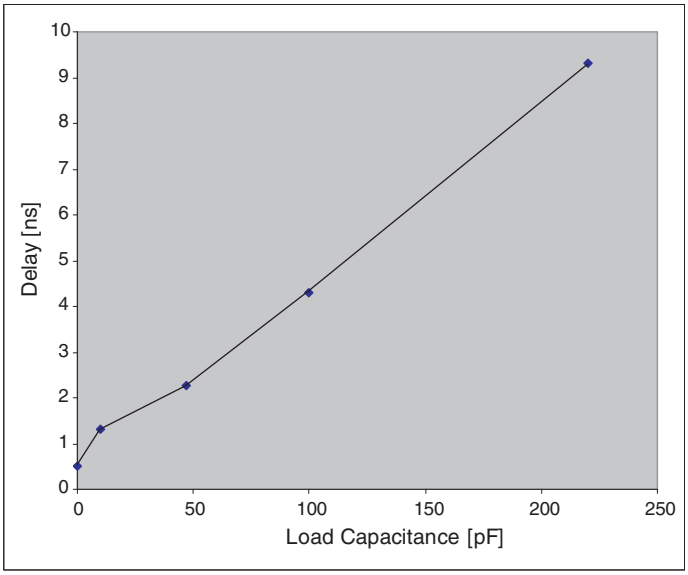
Figure 4. Signal Transition with 100 [pf] Load



6 Transition Time verses Load Capacitance

Figure 5 shows the transition time for these various load capacitors. The Y-axis is in nanoseconds [ns] the X-axis is in picofarads [pf].

Figure 5. Voltage Transition Time verse Load Capacitance



It can be seen from Figure 5 that the time is proportional to load capacitance. In this particular case it is about 1 [ns] for every additional 25 [pf] of load capacitance over the range from 10 [pf] to 220 [pf]. This ratio will be different for different designs.

7 Read Bus Cycle Timing

Excessive load capacitance increases read access time. The following examples show how the increase in voltage transition time increases asynchronous read bus cycle time.

7.1 No Extra Load Capacitance

Figure 6 shows a simplified connection between the CPU and the FLASH. There is no excessive load capacitance.

Figure 6. CPU and FLASH Block Diagram

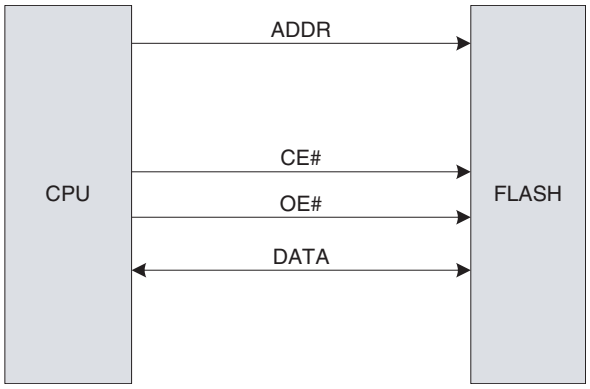
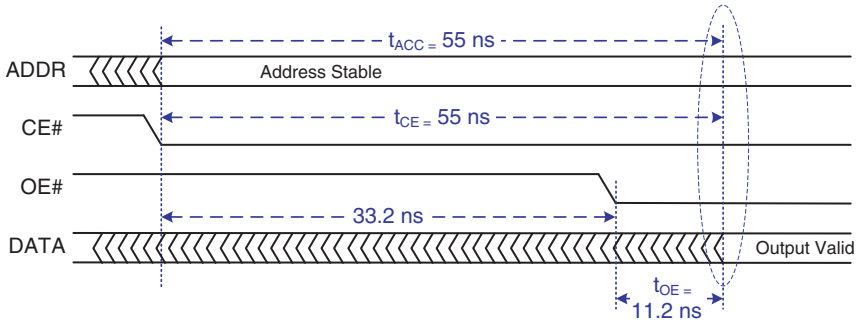


Figure 7 shows a simplified asynchronous read bus cycle. There is no excessive load capacitance. In this example output data is assured to be valid 55 [ns] after the address is first stable.

Figure 7. Simplified Asynchronous Read Bus Cycle

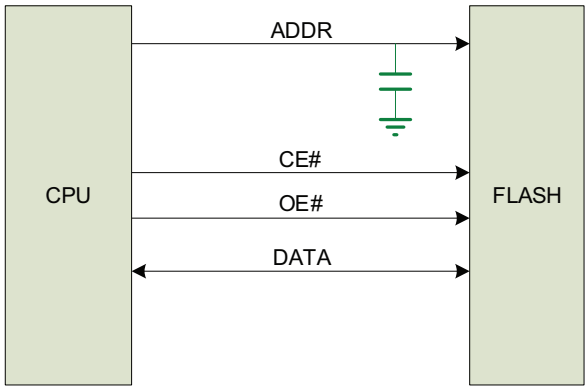
During an asynchronous read bus cycle all the AC parameters must be satisfied. In this case only t_{ACC}, t_{OE}, and t_{CE} are shown. The vertical bar (within the oval) emphasizes that all of the parameters must be met before valid output data can be expected. The signals are shown at the FLASH pins.



7.2 Address Bus with Excessive Load Capacitance

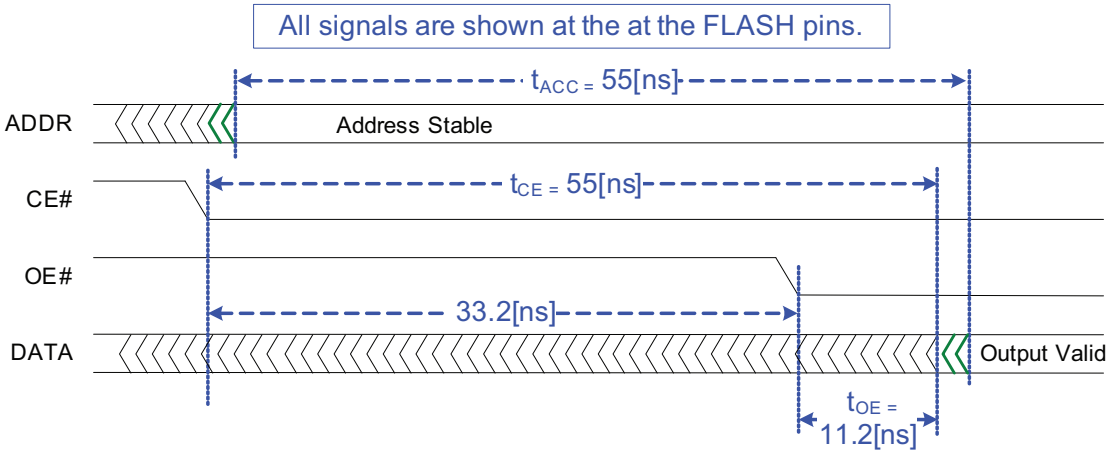
In Figure 8 a green capacitor is used to represent an excessive total load capacitance on the traces of the address bus.

Figure 8. CPU and FLASH with Excessive ADDR Bus Load



This excessive load results in slowed transitions on the ADDR bus and a delay in the arrival of stable address at the FLASH. This delay causes a delay in the output of valid data by the FLASH. This effect is shown by the shifting to the right of Address Stable and Output Valid (See the two green << delays in Figure 9).

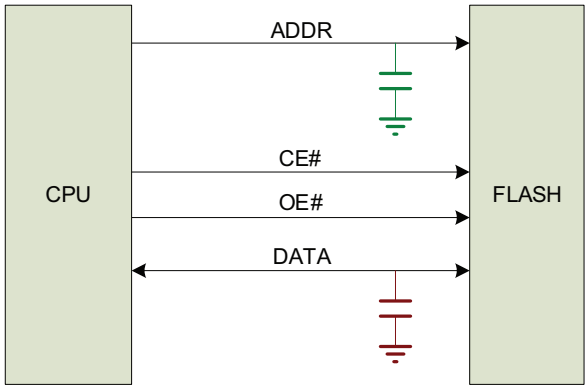
Figure 9. Asynchronous Read Bus Cycle with Excessive ADDR Bus Load



7.3 ADDR and DATA Bus with Excessive Load Capacitance

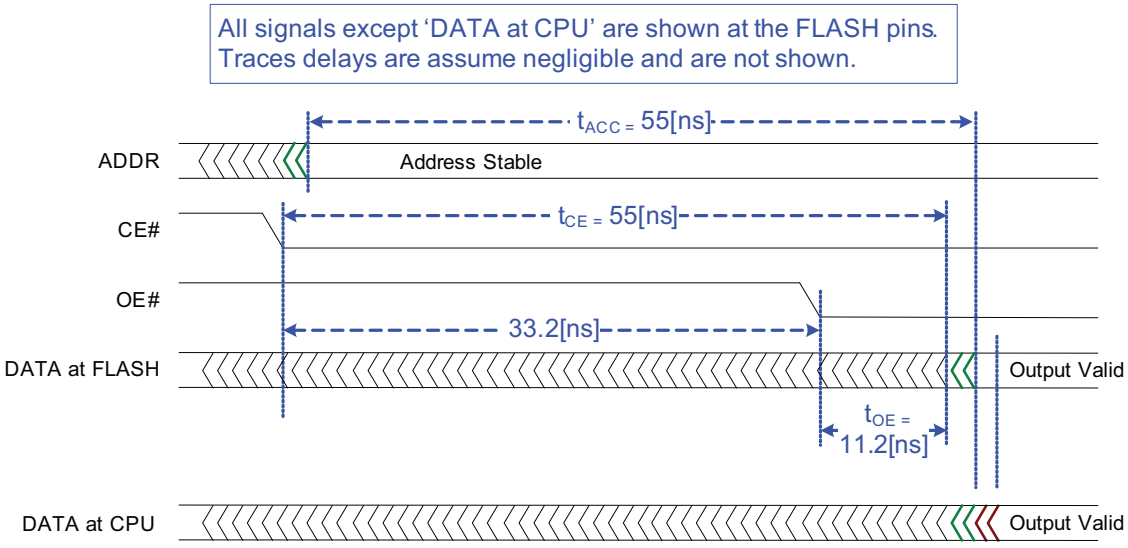
In Figure 10 both the address bus and data bus have excessive load capacitance. The load on the address bus is represented by the green capacitor. The load on the data bus is represented by the brown capacitor.

Figure 10. CPU and FLASH with Excessive ADDR and DATA Bus Load



This results in a further delay in the arrival of valid output data at the CPU. This is shown by the added delay (See the one brown << delay in Figure 11) between Output Valid in 'DATA at FLASH' and Output Valid in 'DATA at CPU'.

Figure 11. Asynchronous Read Bus Cycle with Excessive ADDR and Data Bus Load



Synchronous Bus Cycles and Write Bus Cycles will be affected in a similar manner. The design engineer must provide enough time for the increased transition times to assure reliable operation. Note that for simplicity trace propagation delays were not shown in the prior waveforms.

8 Signal Integrity

In general adding devices to a trace tends to result in a reduction of signal integrity. Some factors that contribute to this are as follows:

- Added trace stubs
- Longer trace length
- Vias (especially through-hole) for a thick PCB
- Additional devices (including connectors) with different load and drive characteristics
- Optional board assemblies in which some devices might not be present

These variables provide more opportunities for signal integrity problems to arise so it is not recommended to have many devices sharing the same trace. Signal integrity simulation tools are often used to reduce this design risk. The use of such tools is beyond the scope of this application note.

9 Strict Interface Standards

Some buses like DDR have very restrictive rules which must be carefully followed. In such cases the adding of capacitive load and trace length is limited or forbidden.

10 Things to Remember

Having excessive capacitive loads on traces is not recommended.

Device performance is not guaranteed for excessive capacitive load, but generally it can be expected that there will be a linearly proportional delay in voltage transitions to the amount of added load capacitance. The ratio for the amount of added delay to the amount of capacitive load will vary by design. Adding load capacitance to traces could cause signal integrity problems. Using a signal integrity tool and simulating with Cypress provided IBIS models on an accurately modelled PCB can reduce this design risk.

11 References

Resonance in Short Transmission Line', HIGH-SPEED DIGITAL DESIGN - online newsletter - Vol. 6 Issue 06

Document History Page

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**	–	–	10/25/2007	Initial version
*A	4958589	MSWI	10/16/2015	Updated in Cypress template
*B	5843220	AESATMP8	08/03/2017	Updated logo and Copyright.

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