Interfacing Infineon S29CD016J Flash to NXP MPC56x Microcontroller

About this document

Scope and purpose

NXP's MPC56X Applications processors and Infineon S29CD016J flash memory are utilized extensively in today's automotive and other embedded applications. Products like Infineon S29CD016J high performance Burst Mode flash enable full flexibility to optimize a processor's read bandwidth and provide better overall system performance levels. This application note provides a brief highlight of some of the devices key product features while illustrating the hardware and configuration considerations when interfacing an MPC56x to S29CD016J.

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1 Interface/Configuration Requirements

The MPC56x Power Architecture processors are designed for high performance embedded requirements like automotive and other control-intensive applications. This MPC56x product family supports extended operating temperature range, 2.6 volt power supply, and supports asynchronous and burst read/write operations to provide high performance capabilities. The S29CD016J is a high performance flash device supporting extended operating temperature range, 2.6V V_{CC}, V_{IO} option for 1.65V to 2.75V, asynchronous/burst mode accesses, Simultaneous Read/Write Operations for 16 Mb and 32 Mb densities. The following will address some of the basic interface and configuration requirements for the MPC56x family to perform 5-1-1-1 synchronous accesses to retrieve data from a S29CD016J flash.

1.1 Power Supply Requirements

The MPC56x internal logic of the processor requires a nominal 2.6 volt supply like the S29CD016J V_{CC} range (2.5V and 2.75V) while supporting a V_{IO} option for 1.65V to 2.75V. A 2.6-volt power supply can be connected to VDD and routed to the processor power pins (VDDF, QVDDL, NVDLL and KAPWR). The V_{CC} and V_{IO} pins of the flash memory can interface directly to the VDD pin of the microprocessor as long as the supply is regulated within flash V_{CC} operating range. The ground pins V_{SS} and V_{SSF} pins on the microprocessor can be connected directly to V_{SS} of the flash memory.

1.2 Hardware Reset

The HRESET# pin of the MPC56X should be connected to the RESET# pin of the S29CD016J flash memory to enable both devices to be reset during unexpected power down situations and to ensure that the flash is ready to be accessed following any system reset. Note during power down once the flash V_{CC} drops below V_{LKO} the flash V_{CC} should be completely powered down prior to reinitiating power up sequence.

1.3 Address, Data Bus, and Control Signal Interface

The MPC56x will need to access the S29CD016J in 32 bit mode which requires 19 address lines to access the 2 Mbyte cell array (512 kB by 32-bit). The MPC56x processor typically has its data order configured as most significant bit to least significant bit and the S29CD016J is setup least significant bit to most significant bit; under these conditions the address and data pins connections must be bit number reversed. Flash address lines A0–A18 are connected to A29–A11 of the microprocessor while the flash data lines D0–D31 are connected to D31–D0 of the processor. The CLK, CE#, OE#, WE#, and ADV# control signals from the flash memory must be connected to CLK, CSx#, OE#, WE#, and TS# of the microprocessor. **Table 1** lists the hardware interface between the MPC56x and the S29CD016J, while **Figure 1** provides a high level interconnect diagram.

Note: The MPC56x can access the flash using any of its chip selects CSx# but CS0# is required when booting from flash.

Table 1 MPC56x and S29CD016J Interface

Power Connection / Device	CPU	Flash
V_{CC} Power Supply	VDD, VDDF, QVDDL, NVDLL, KAPWR	V_{CC}, V_{IO}
Clock	CLK	CLK
Chip Select	CSx#	CE#
Output Enable	OE#	OE#
Write Enable	WE#	WE#
Address Valid	TS#	ADV#
Address Bus	A29 - A11	A0 - A18
Data Bus	D0-D31	D31 - D0

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Power Connection / Device	CPU	Flash
Reset	HRESET#	Reset#
Ground	VSS, VSSF	V_{SS}

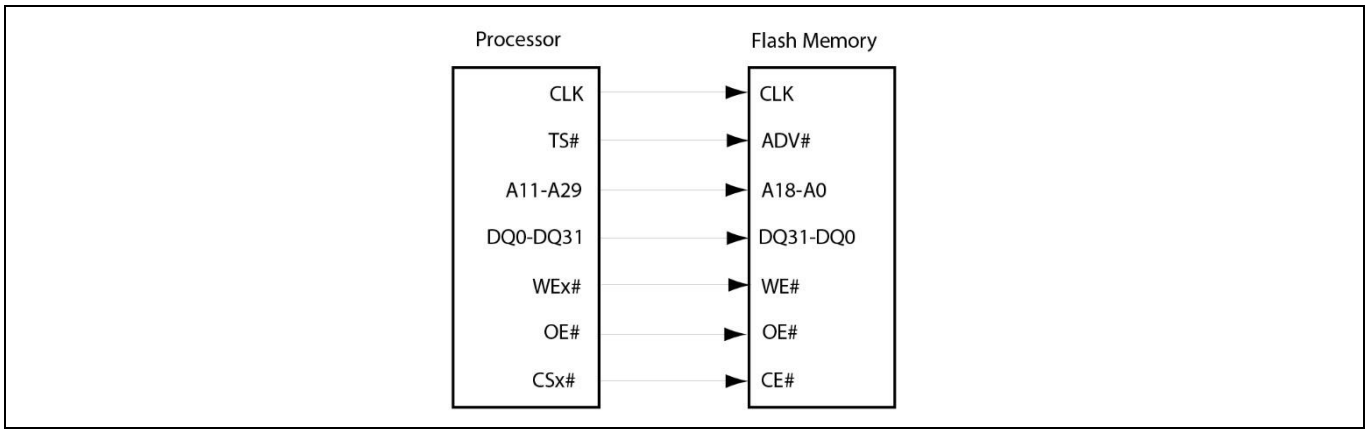

Figure 1 Interface Between MPC56x and S29CD016J

1.4 Bus Operations, Timings, and Device Configuration

1.4.1 Boot-up From Flash

The signal timings of the flash memory and the processor are compatible over a range of frequencies. The standard S29CD016J offering includes 40 MHz to 66 MHz operation. Upon boot-up the flash default access mode is asynchronous read. The MPC56x microprocessors come out of reset in sequential mode with its default setting of 15 wait states, which meets the S29CD016J asynchronous access timing requirements.

1.4.2 Synchronous Burst Mode Accesses

There are a number of steps to enable synchronous accesses after completing the initial boot code process; the following provides a high level description of the steps required to configure the MPC56x and S29CD016J for 5-1-1-1 synchronous access:

1. Boot the system; copying the basic initialization information from flash to the MPC56x internal SRAM
2. Exit MPC56x Serialized Mode by modifying the ISCT_SER field in the ICTRL Register to 10b
3. Branch to the mode changing code copied in the SRAM
4. Program S29CD016J Configuration Register (Support for 5-1-1-1 synchronous accesses)
5. Program MPC56x BR0, OR0, BBCMCR and SIUMCR Registers: (Support for 5-1-1-1 synchronous accesses)
6. Once the above steps are successfully completed then the flash can be accessed synchronous accesses.

The next sections will highlight Processor and flash configuration setting considerations to support a 5-1-1-1 synchronous access.

1.4.3 Programming S29CD016J Configuration Register

Table 2 provides the basic command sequence to write to the S29CD016J Configuration Register.

Table 2 S29CD016J Configuration Register Write Definition

Clock	Cycle 1	Cycle 2	Cycle 3	Cycle 4
Addr	555h	2AAh	555h	XX
Data	AAh	55h	D0h	WD

Note: The MPC56x uses byte addresses whereas the Infineon flash uses 32-bit word addresses. Pins A30:A31 are not connected. Therefore, address CPU A29 is attached to flash A0, instead of CPU A31. This results in an address shift left by 2 bits. The 32 bit word mode representation of address 2AAh would be AA8h in byte mode. The data WD represents the 16-bit flash Configuration Register settings.

The S29CD016J default access mode after boot up is asynchronous; Table 3 highlights all the default bit settings for the flash Configuration Register after boot-up. Reference the S29CD-J and S29CL-J Flash Family data sheet for functions of each group of bit settings.

Table 3 S29CD016J Flash Configuration Register Default Setting

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	Reserve	IAD3	IAD2	IAD1	IAD0	DOC	Reserve
1	0	0	1	1	1	0	0

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
BS	CC	Reserve	Reserve	Reserve	BL2	BL1	BL0
1	1	0	0	0	1	0	0

1.4.4 Initial Access Timing Settings

The MPC56x and the S29CD016J default configuration settings do not provide optimal access timing. The MPC56x default setting is 15 wait states for either a random access read or the initial read of a burst access. Similarly, the S29CD016J's default Burst Initial Access Delay is 9 clock cycles. This means that both the MPC56x Memory Controller Option Register (ORx[24-27]) and the S29CD016J Configuration Register (IAD[3:0]) must be modified to enable more optimal access operations.

The timing of a 4 beat burst mode access is generally stated using a shorthand convention like: x-y-y-y. The first number (x) represents the number of clock cycles to access the 1st word. The other numbers are how many clock cycles to access the second, third and fourth accesses. An example would be 5-1-1-1, requires eight clock cycles to complete the four beat burst while a 6-1-1-1 would require nine clock cycles to complete the same four beat access.

It is important to understand the convention used to determine the MPC56x wait states compared to the number of clock cycles comprising the S29CD016J Burst Initial Access delay is not exactly the same. The first wait state (clock cycle) for the MPC56x is the CLK cycle that puts the address on the bus with the falling edge of both the CLK and ADV# while flash initial access or clock counts is started after the later occurrence of the falling edge of ADV# or by valid address. The 5-1-1-1 access timing provides the number of clock cycles the flash requires once the flash initial access has been started which means the processor timing can include one or more additional clock cycles.

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The S29CD016J supports a wide range of initial access delays as shown in **Table 4** highlighting the 5-1-1-1 access timing while **Table 5** and **Table 6** highlight the MPC56x ORx and BR0 Register settings for the same 5-1-1-1 access.

Table 4 S29CD-J Burst Initial Access Delay Nomenclature and Configuration Register Settings

Initial Access Delay	Configuration Register (IAD3-IAD0) CR13-CR10	Initial Burst Access Clock Cycles
4-1-1-1	0010	4 CLK cycle initial burst access delay **(1)**
5-1-1-1	0011	5 CLK cycle initial burst access delay
6-1-1-1	0100	6 CLK cycle initial burst access delay
7-1-1-1	0101	7 CLK cycle initial burst access delay
8-1-1-1	0110	8 CLK cycle initial burst access delay
9-1-1-1	0111	9 CLK cycle initial burst access delay

Note:

1. *S29CD-J can support 4-1-1-1 access up to 40 MHz clock frequency.*

Table 5 MPC56x ORx Configuration Register

Bit	Name	Value	Comment
0-15	Address Mask	0xFFC0	0xFFC0 for mask in 32 bit setup
16	Address Mask	0	Bit 16 must be on always
17-19	Address Type Mask	User Defined	
20	CNST	0	
21-22	ACS	00b	No delay required
23	ETHR	0	Not required
24-27	SCY	100b	6 clock cycles
28-30	BSCY	000b	Initialize 1 clock period per beat
31	TRLX	0	Not Required

Table 6 MPC56x BR0 Configuration Register

Bit	Name	Value	Comment
0-16	Base Address	User defined	Flash Base Address
17-19	Address Type	User Defined	User assign Flash to address type
20-21	Port Size	00b	00 - 32 bit Port Size 10 - 16 bit Port Size
22	Reserved		
23	Write Protect	Ussr defined	0 - for flash programming 1 - for flash reading only
24	Reserved		
25	Burst Length	0	0 - Burst Access up to 4 words 1 - Burst Access up to 8 words

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Bit	Name	Value	Comment
26	WEBS	0	
27	TBDIP	0	Do not toggle BDIP
28	LBDIP	0	No late BDIP
29	TA	0	No external TA
30	Burst Inhibit	0	0 - Enable burst access 1 - Disable burst access
31	Valid	1	Activate current bank

Figure 2 shows a timing diagram for a 5-1-1-1 burst mode access again the S29CD016J's initial access is started by the later occurrence of the falling edge of ADV# or by address valid during the first clock cycle. The flash outputs the initial data during the fifth clock cycle and the processor captures the data on the rising edge of sixth clock cycle. New data is output on subsequent rising clock edges until the burst read is completed.

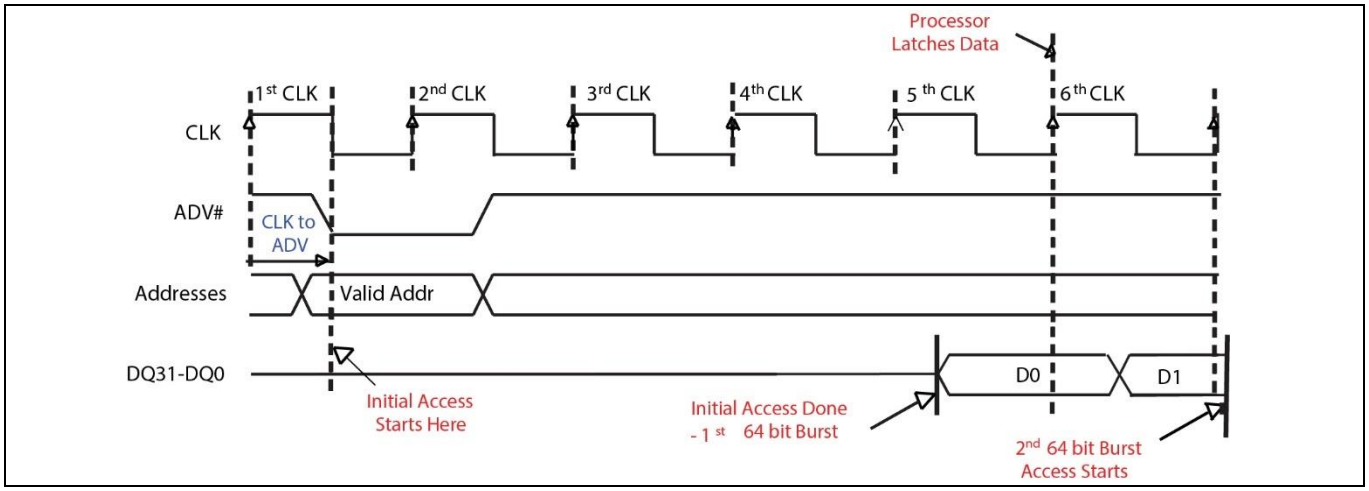

Figure 2 5-1-1-1 Burst Read Access

1.4.5 S29CD016J Configuration Register Settings

There are several parameters including RM, IAD, and BL which need to be set modified in the Configuration Register to support 5-1-1-1 synchronous accesses. The initial access delay (IAD) options have already been discussed in detail. The RM and BL selections are straight forward:

- RM =1 Enables Synchronous Access
- BL = 010 Enables 4 beat double word access

Bit definitions that need to be modified to support a 4 beat 5-1-1-1 burst access are as follows and shown in **Table 7**. Note the Configuration register cannot be programmed while another Embedded Operation (program or erase) is active.

Interface/Configuration Requirements

Table 7 S29CD016J Flash Configuration Register Setting for 5-1-1-1 Access

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	Reserve	IAD3	IAD2	IAD1	IAD0	DOC	Reserve
1	0	0	1	1	1	0	0

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
BS	CC	Reserve	Reserve	Reserve	BL2	BL1	BL0
1	1	0	0	0	1	0	0

2 Summary

NXP's Power Architecture products like MPC56X continue as a world leading solution for automotive and other embedded applications. Products like Infineon S29CD016J high performance Burst Mode flash offer substantial flexibility and high performance enabling optimization of the processor’s read bandwidth and provide better overall system performance levels. This application noted provides a brief highlight of some of the devices key product features while illustrating the hardware and configuration considerations when interfacing an MPC56x to S29CD016J. Both these product families continue providing cost effective innovative high performance solutions while maintaining product reliability and long term support strategies.

References

[1] **Infineon S29CD016J Datasheet**

[2] NXP MPC56X Datasheet

Revision history

Document version	Date of release	Description of changes
**	2010-12-15	Initial version.
*A	2019-01-18	Updated to template Completing Sunset Review
*B	2021-03-26	Updated to Infineon template

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