Interfacing i.MX6x to S29GL-S MirrorBit™ Flash

About this document

Scope and purpose

AN98562 highlights key i.MX6x processor / S29GL-S flash device features and outlines an example case illustrating the hardware and configuration consideration when interfacing an i.MX6x to the S29GL-S.

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1 Overview and Background

1.1 Introduction

The initial discussion provides a very brief overview of the NXP i.MX6x single, dual, and quad-core multimedia processor and the S29GL MirrorBit Eclipse™ flash family. These initial comments will be followed with additional information concerning the seamless interface between i.MX6x and the S29GL-S flash and a simple case study of the i.MX6 / S29GL-S read performance capabilities.

1.2 NXP i.MX6x Multimedia Processor

NXP highlights the iMX family as a versatile platform for multimedia and display applications, which uses an ARM®-based processor offering both performance and integration to enable next-generation smart devices. The i.MX6x provides scalable multi-core platform solutions ranging from single, dual, and quad-core families based on the ARM Cortex®-A9. The i.MX6x feature set enables next-generation consumer, industrial, and automotive applications by combining the powerful processing capabilities of the ARM Cortex-A9 with enhanced 2D / 3D graphics, as well as high-definition video. The i.MX6x provides a new level of multimedia performance and is enabling the next generation user experience. **Figure 1** shows the i.MX6x high level block diagram. The i.MX6x external memory controller provides the ability to connect to a wide variety of memory devices. The external memory controller includes multi-mode DDR controller, Raw NAND flash controller, and the WEIM-PSRAM / NOR-flash interfaces.

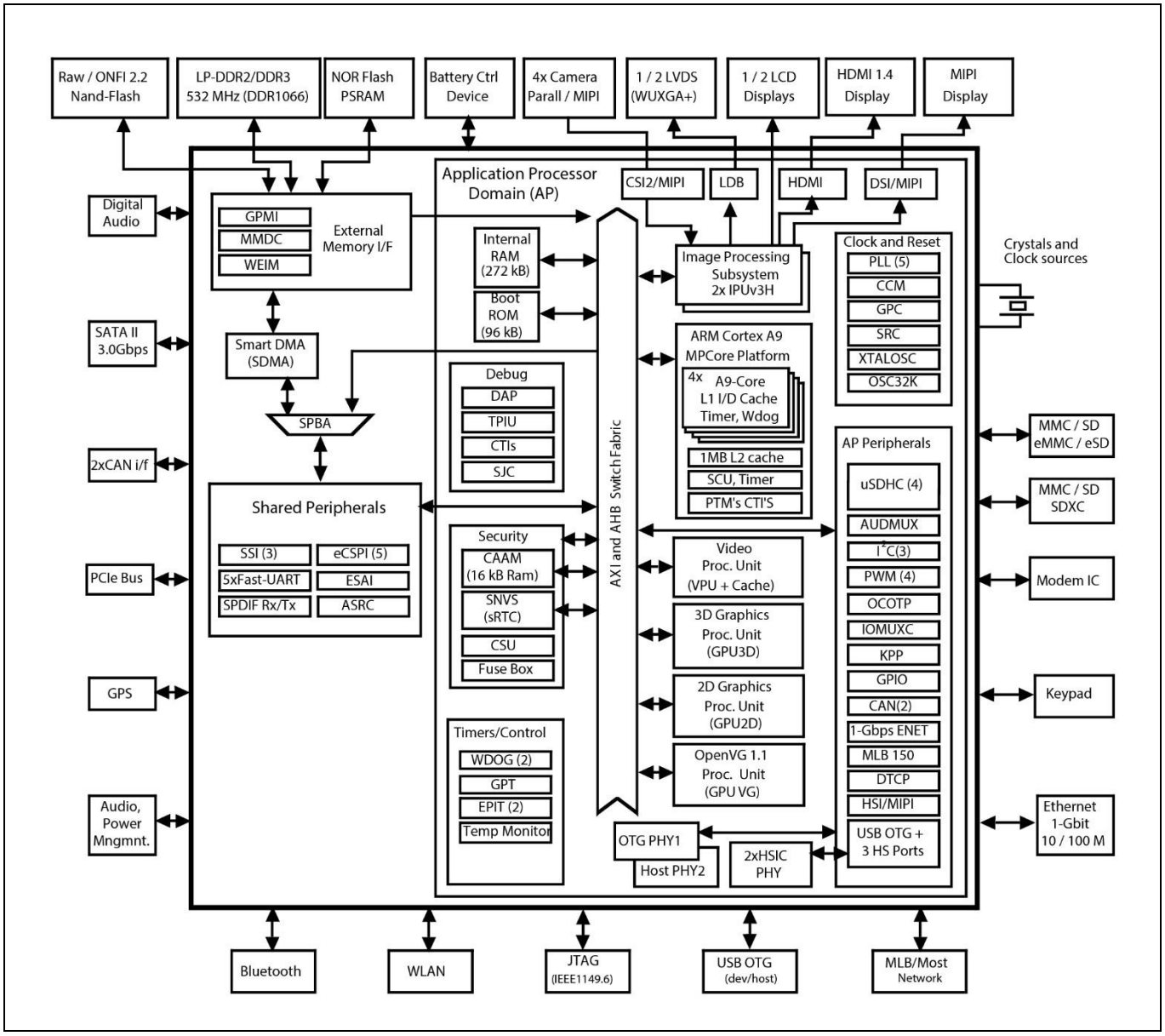

Figure 1 i.MX6x Block Diagram

This application note focuses on the i.MX6x External Interface Module (EIM), which provides flexible asynchronous and synchronous access to a wide range of external peripherals such as SRAM, PSRAM and parallel NOR flash. The i.MX6x uses a similar EIM configuration as offered on the previous generation i.MX53. Note the i.MX6x system bus is faster (2x 64-bit at 532 MHz) compared to the i.MX53, which uses a 64-bit at 200 MHz. It should be noted the EIM and the NAND flash controller share data bus pins in order to reduce the total number of EXTMC I/O.

1.3 External Interface Module Features

- Up to six chip selects for external devices
- Programmable Data Port Size (x8, x16, and x32)
- Programmable Wait-State Generator: read and write accesses
- Configurable Chip Select 0 base address
- 28-bit address bus: 256 Mbyte (2 Gigabit)

Overview and Background

- Access Modes: asynchronous, page, burst, multiplexed /non-multiplexed
- Page size options: 2, 4, 8, 16, or 32 words
- EIM Main Clock: maximum frequency 133 MHz
- Supports Boot from external device using CS0

A high level block diagram for the i.MX6x EIM is shown in **Figure 2**.

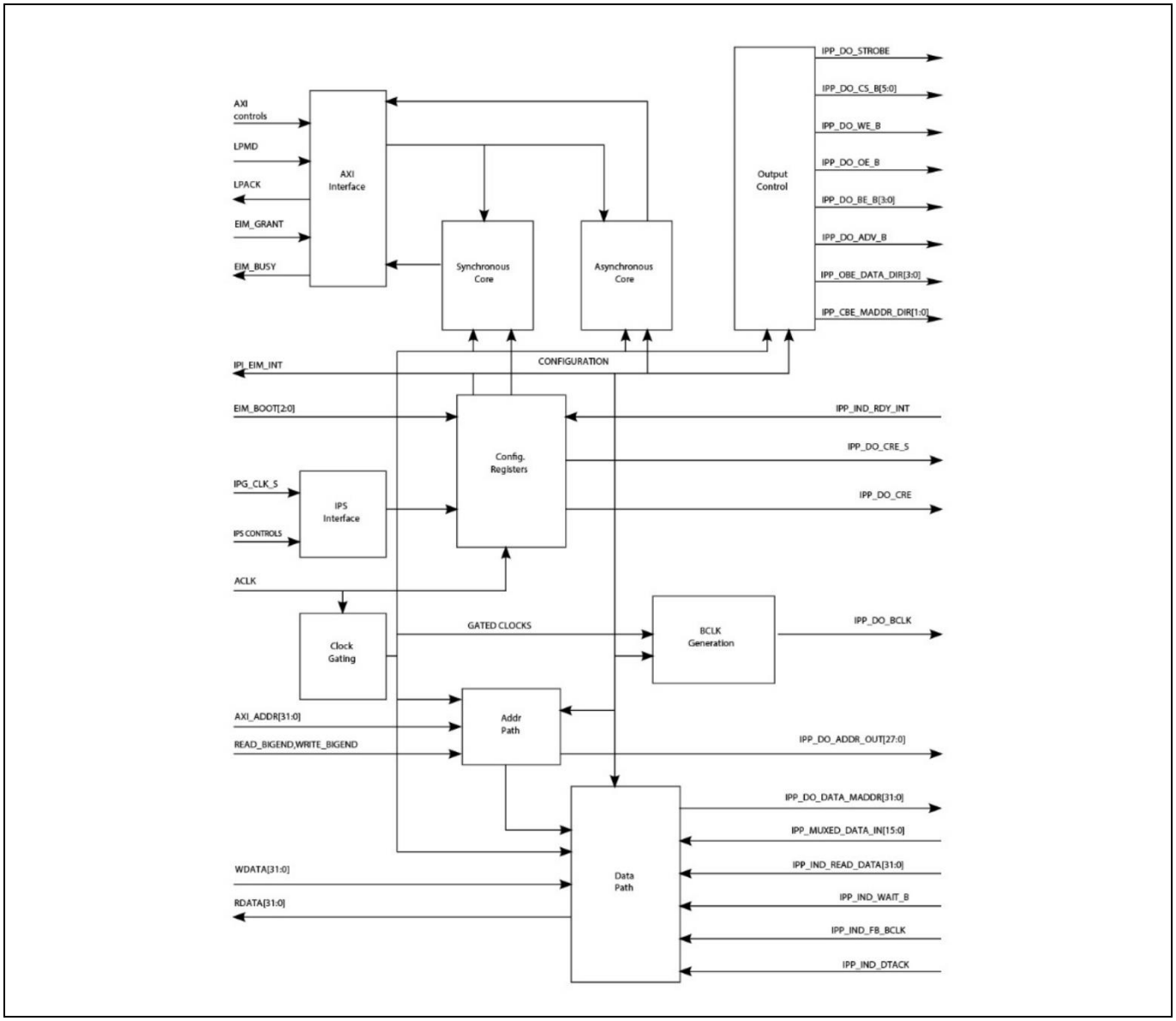

Figure 2 i.MX6x EIM Block Diagram

1.4 S29GL MirrorBit NOR Flash Family

The S29GL MirrorBit flash family is the industry's leading price-performance NOR flash memory technology for embedded applications. The S29GL MirrorBit technology enables designers to create innovative, state of the art, cost-effective solutions. This product family offers densities from 32 Mb (4 MB) to 2 Gb (256 MB), supporting 3.3V or 1.8V interface voltages, long term reliable data integrity, high performance Page Read / Write Buffer programming, and long term product support. The S29GL also features a universal package footprint across device densities for both BGA and TSOP packages. These features can be leveraged to use varying flash densities across a customer's product line to minimize NRE development cost and time-to-market.

Overview and Background

The latest S29GL-S family integrates MirrorBit Eclipse architecture. The Eclipse architecture enables high bandwidth programming up to 1.5 MB/s. This programming BW is more than 10x faster compared to the previous generation. The S29GL-S MirrorBit Eclipse also further enhances the Page Read access times, enabling read BW up to 96 MB/s. These features along with sustaining expected NOR reliability and continuing cost reductions trends make these devices ideal for today's embedded applications solutions requiring state of the art read / program performance.

Figure 3 shows a typical block diagram for an S29GL Asynchronous / Page MirrorBit flash.

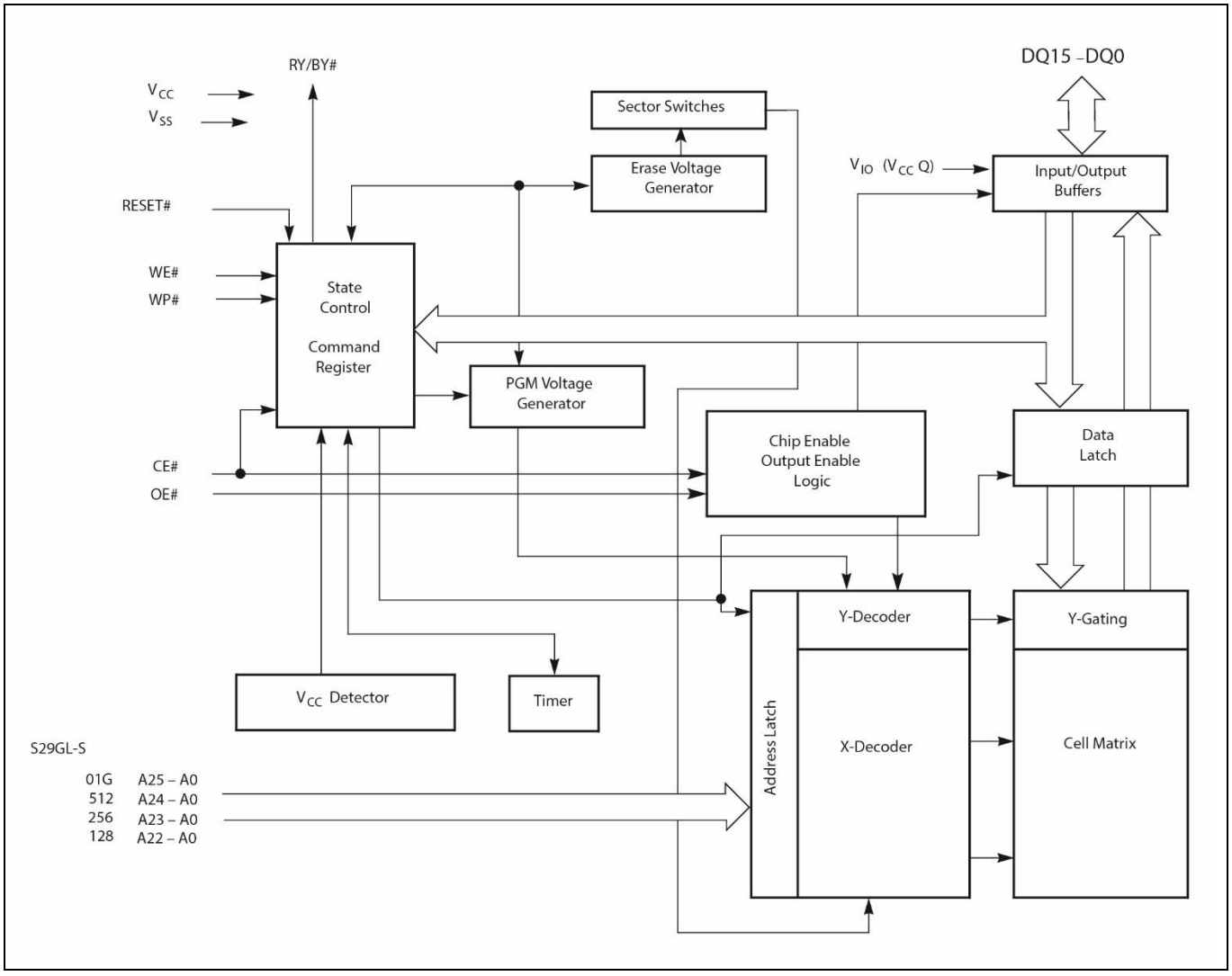

Figure 3 S29GL Asynchronous / Page Mode Block Diagram

2 i.MX6x and S29GL Interface Considerations

This section considers the interface requirements for an i.MX6x and S29GL128S. Reference the i.MX6x and S29GL technical documentation to determine the best interface/setup options for specific application requirements.

2.1 Hardware Interface

As stated earlier, the i.MX6x offers non-multiplexed and multiplex options to support asynchronous and page read accesses to external peripherals. This section highlights options for interfacing the i.MX6x and S29GL128S to support asynchronous and page read accesses.

2.1.1 High Level i.MX6x / S29GL-S Interface

Figure 4 shows the signal interface from the i.MX6x to an S29GL-S NOR flash.

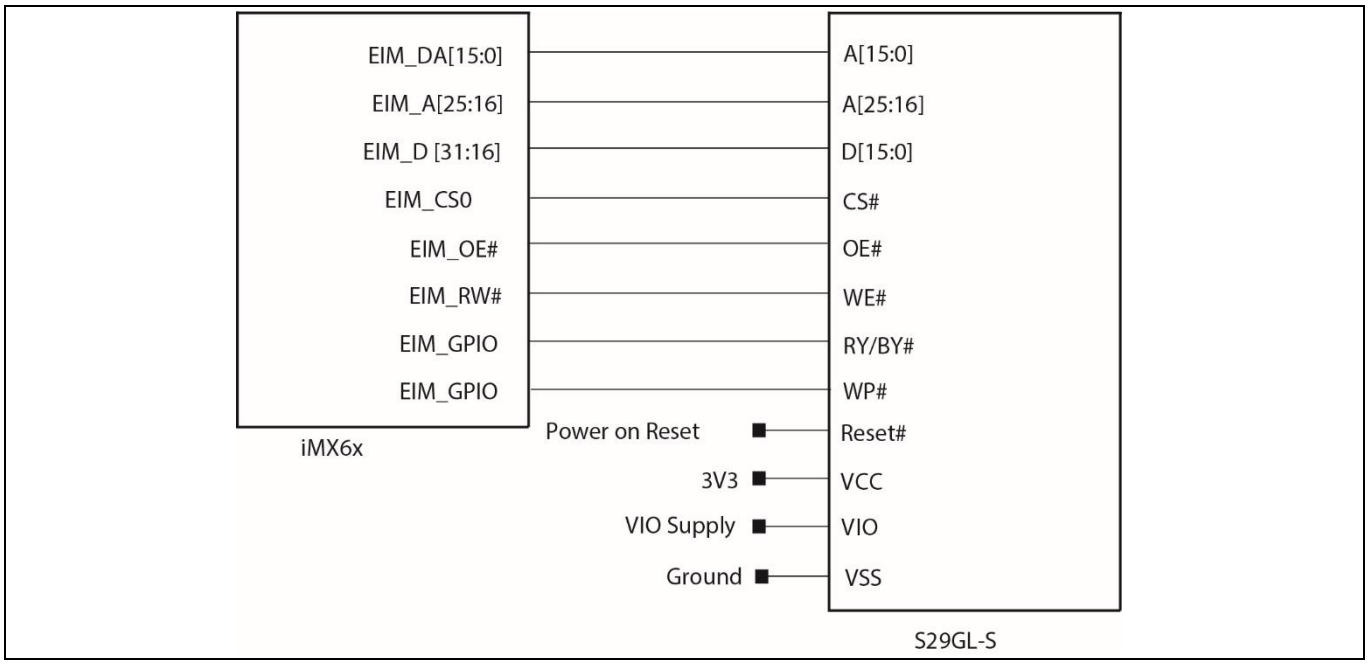

Figure 4 Interface Diagram for i.MX6x to S29GL-S

Note:

1. *CS0 required for boot.*
2. *RESET should be connected to same system reset driving the i.MX6x.*

2.1.2 Interface Diagram for i.MX6x to S29GL-S

The i.MX6x EMI I/O interface power supply should be set up according to external memory requirements. Reference the i.MX6x data sheet for additional details.

2.2 i.MX6x / S29GL-S Read Performance Considerations

Embedded applications require fast read performance to enable high speed data transfers from flash to support fast start-up requirements or transfers of data from NVM to DRAM. The following highlights a case study of the read performance that can be obtained when interfacing the i.MX6 to a S29GL-S flash.

3 Example: i.M6 EIM / S29GL-S Functionality

After the power is turned on a system can:

1. Start execution from S29GL-S / Initialize the i.MX6x
2. Copies the flash code to main memory (DDRx)
3. i.MX6 initiates execution from DDR

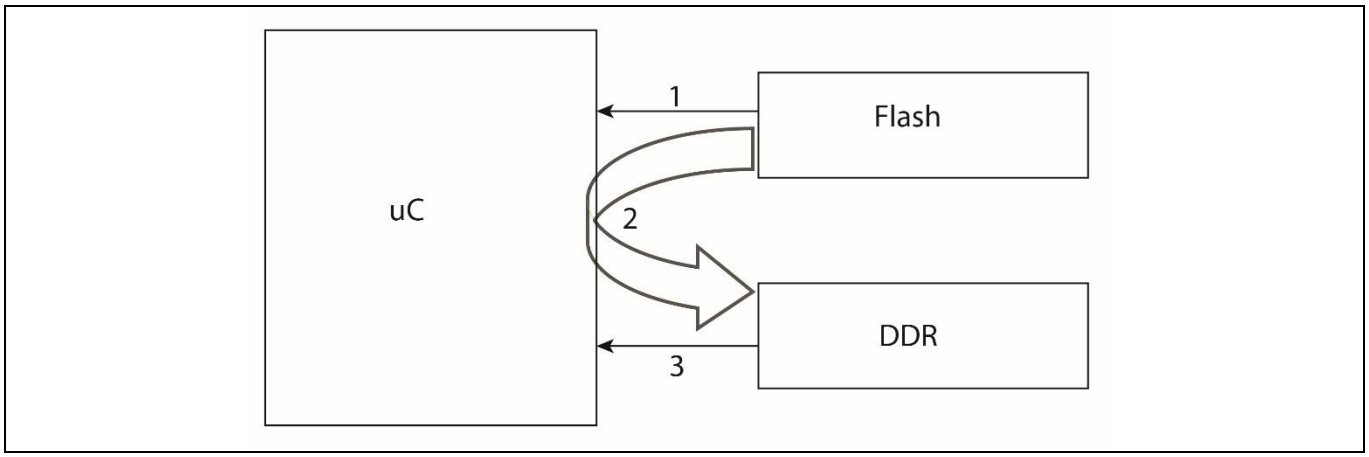

Figure 5 Example Boot-Up Process

3.1 i.MX6x and S29GL-S Access Highlights

- i.MX6x provides a seamless non-multiplexed address data bus interface to the S29GL-S flash
- i.MX6x and S29GL-S support asynchronous or page mode read access capability

The cache line size should match the flash page size.

3.2 i.MX6x Read Access

- Asynchronous Access: single word
- Read Page Access: 2, 4, 8, 16, or 32 words
- EIM Main Clock: default frequency 133 MHz
- Flexible read and write access timing

3.3 i.MX6 Clocking

- EIM (NOR flash memory controller) clock is 133 MHz by default
  - Clock adjustable for individual memory timing requirements
- Two examples clock setting to access S29GL-S (90 ns model):
  - Configuration 1: Optimal Read Performance / Reduced Timing Margins

    EMI clock frequency: 120 MHz (8.3 ns per clock tick)

    EMI settings for t_{ACC}: 91.7 ns (11 clock ticks of 8.3 ns)

    EMI settings for t_{PACC}: 16.7 ns (2 clock ticks of 8.3 ns)
  - Configuration 2: Good Read Performance / Improved Timing Margins

    EMI clock frequency: 133 MHz (7.5 ns per clock tick)

Example: i.M6 EIM / S29GL-S Functionality

EMI settings for t_{ACC}: 97.5 ns (13 clock ticks of 7.5 ns)

EMI settings for t_{PACC}: 22.5 ns (3 clock ticks of 7.5 ns)

Note: These register settings are not guaranteed by Infineon.

Table 1 i.MX6 Configuration Register Settings

Register Name	Configuration 1	Configuration 2
EIM_CS0GCR1	0x10020281	0x10020281
EIM_CS0GCR2	0x00000001	0x00000001
EIM_CS0RCR1	0x0b020000	0x0d020000
EIM_CS0RCR2	0x00008000	0x00009000

3.4 S29GL-S Read Access

- Initial Access: t_{IACC} options from 90 ns to 120 ns page
- Read Access
- Page Size: 16 words and t_{PACC} options from 15 ns to 30 ns

Figure 6 and **Table 2** illustrate the general S29GL128S with 90 ns initial access and 15 ns page read access characteristics.

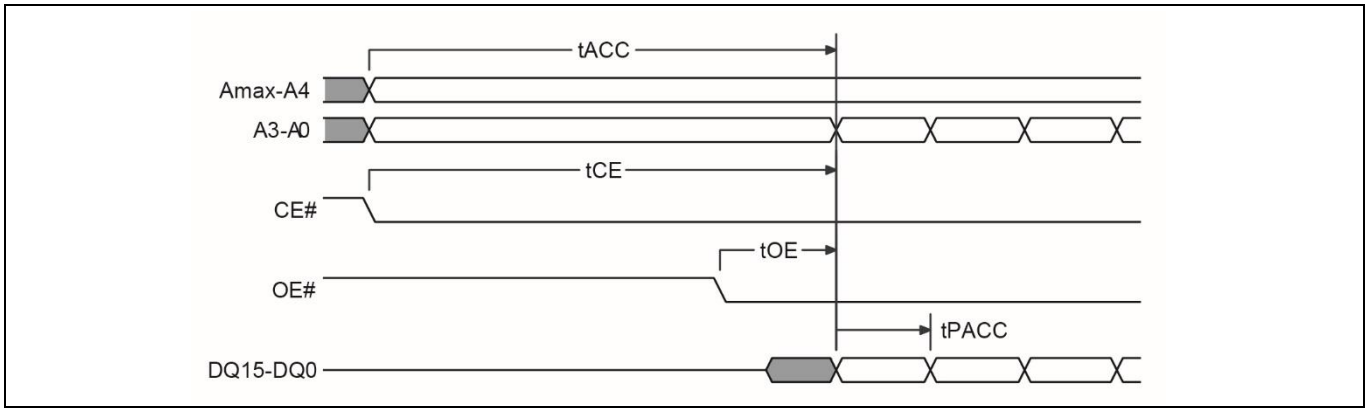

Figure 6 S29GL-S Asynchronous / Page Read Access

Note:

1. *Word Configuration: Toggle A0, A1, A2, and A3.*

Table 2 S29GL128S90 Access Characteristics

Parameter Description	Value
Asynchronous Access: (t_{ACC})	90 ns
Page Access (t_{PACC})	15 ns
Read Page Size	16 words (32 bytes)

3.5 Read Access Algorithms / Performance Results

- Access algorithms options: optimize flash data transfer to DRAM
  - Simple load/store instructions: non-optimal performance
  - Memcpy() OS / DMA routines: provides better performance
  - Cached access typical provides better performance than uncached
  - Data Cache benefits read-only situations: i.e. boot loaders and other read only requirements

Table 3 Performance Results: i.MX6 / S29GL-S SABRE Solo Platform

Software Algorithm	Configuration 1	Configuration 2
memcpy() cached	80.4 MB/s	65.5 MB/s
memcpy() uncached	59.9 MB/s	53.1 MB/s
DMA with Polling	36.6 MB/s	33.0 MB/s
DMA with Interrupts	35.9 MB/s	32.0 MB/s

Key take away: Memcpy() outperforms DMA.

4 Conclusion

This document highlights key i.MX6x and S29GL-S device features and outlines an example case illustrating the hardware and configuration consideration when interfacing these devices in your next design. The examples show cases how both NXP's and Infineon product optimizations enable embedded system solutions supporting faster read and programming capabilities. NXP's new i.MX6x and Infineon latest S29GL-S flash continue to enable state of the art embedded design innovations and solutions.

References

Infineon and NXP each offer extensive support for their product portfolios.

[1] Infinoen has substantial development collateral including data sheets, application notes, software drivers, simulation models, hardware development tools, and other support items. They can be found at:

http://www.cypress.com/products/parallel-nor-flash-memory

An example software tool offering is the FFS™. The Flash File System enables faster read and write system performance for flash memory. This is another case of how Infineon is providing solutions to our customers to optimize system performance. By using FFS, software engineers can extract the full value of NOR flash memory and tune products to offer a better user experience and ensure very high levels of performance and reliability.

[2] NXP offers i.MX6x product documentation and product reference designs that provide a functional hardware platform and software solution for engineers to develop with the i.MX6x processor family.

http://www.freescale.com/webapp/sps/site/overview.jsp?code=IMX6X_SERIES

Revision history

Document version	Date of release	Description of changes
**	2013-07-09	Initial version
*A	2015-10-13	Updated in template
*B	2017-08-02	Updated logo and Copyright
*C	2018-07-18	Updated template Fixed Figure 4
*D	2021-03-26	Updated to Infineon template

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