Infineon, Micron, and Winbond High Density 3.0 Volt SPI Flash Core Command Sets

About this document

Scope and purpose

AN98554 discusses the differences of the core command sets Infineon high-density, 3.0-V SPI flash devices with 128 Mbit or higher densities with devices from Micron and Winbond.

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1 Introduction

Based on de facto standards, Serial Peripheral Interface (SPI) flash memory has evolved with faster interface speeds and wider data paths, higher densities, and new features while maintaining backward compatibility with the earliest single bit Serial input and output (SIO) SPI flash memories.

New feature support for Dual I/O (DIO), Quad I/O (QIO, Double Data Rate (DDR), extended 32-bit or 4-byte addressing, and flexible individual sector protection schemes, SPI command sets have grown in size and diverged based on manufacturer implementations. This will continue until “de facto” standard commands emerge or all competitive methods are adopted in a multifunction tool (“Swiss Army knife”) approach.

1.1 32-Bit or 4-Byte Addressing

Previous generation (legacy) SPI flash devices supported only 24-bit or 3-byte addressing to access 16 Mbytes or 128 Mbits of address space. With 32-bit or 4-byte Extended addressing, SPI flash devices can support densities of 256 Mbit and higher, up to a theoretical 4 Gbytes or 32 Gbits of address space.

The Infineon S25FL-S 3.0V SPI flash family supports 4-byte extended addressing across densities, from 128 Mbit to 1 Gbit for software portability across designs with different memory requirements. By contrast, Micron® and Winbond® have only added 4-byte extended addressing support to SPI flash with densities of 256 Mbit or higher.

Infineon S25FL-S SPI flash supports extended addressing three ways:

- Bank address register — a software (command) loadable internal register that supplies the high-order bits of address when legacy 24-bit or 3-byte addresses are in use.
- Extended address mode — a bank address register bit that changes all legacy commands to expect 32-bit or 4-byte addresses supplied from the host system.
- New commands — that perform both legacy and new functions, which expect a 32-bit or 4-byte address.

Micron and Winbond support similar extended addressing schemes, though the implementation details differ, as discussed in **Write and Register Access**. In addition, Micron and Winbond support a common SPI command based approach to Enter 4-Byte Address Mode and Exit 4-Byte Address Mode.

2 Core 3.0 Volt SPI Commands

Command sets from Infineon, Micron, and Winbond high density 3.0 volt SPI flash devices of 128 Megabit (Mbit) or higher densities are compared in this application note. Core commands supported by at least two manufacturers or critical SPI commands from a single manufacturer are distilled into tabular formats for comparison and reference.

Designs requiring or preferring SPI flash memories with second sources can leverage these tables to implement portable firmware or driver software in order to minimize considerations for each manufacturer's proprietary implementations.

The following manufacturer device data sheets were compared to develop the 3.0 volt SPI Core Command tables:

Table 1 3.0 Volt SPI Flash Devices Compared by Manufacturer

Manufacturer	Density			
	128 Mbit	256 Mbit	512 Mbit	1 Gbit
Infineon	S25FL127S S25FL128S	S25FL256S	S25FL512S	S70FL01GS
Micron	N25Q128A	N25Q256A	N25Q512A	N25Q00AA
Winbond	W25Q128BV W25Q128FV	W25Q256FV W25Q257FV		

Note:

1. *The Winbond W25Q128JV, W25Q256JV, and W25M512JV data sheets have not yet been released and were not included in the comparison.*

2.1 Read Device ID

When supported, the Read JEDEC Serial Flash Discoverable Parameters 5Ah command should be used to read device identification, feature, and configuration information in accordance with the JEDEC JESD216 standard. Otherwise, the Read ID (RDID) 9Fh command should be used to access manufacturer identification, device identification, and Common Flash Interface (CFI) information.

Table 2 Read Identification Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
Read ID	9Fh	9Fh	9Fh
Read JEDEC Serial Flash Discoverable Parameters	5Ah **(1)**	5Ah	5Ah
Read Electronic Signature	ABh	—	ABh **(2)**

Note:

1. *Infineon S25FL127, S2FL512S, and S70FL01GS support the Read Serial Flash Discoverable Parameters command.*
2. *Winbond also uses the ABh command code for the Release from Deep Power-Down Mode command.*

2.2 Read Flash Array

All of the manufacturers support the standard Read Flash Array commands for Single I/O, Dual I/O, and Quad I/O: Read 03h, Fast Read 0Bh, Read Dual Out 3Bh, Read Quad Out 6Bh, Dual I/O Read BBH, and Quad I/O Read EBh.

On devices supporting DDR read, the DDR Fast Read 0Dh, DDR Dual I/O Read BDh, and DDR Quad I/O Read EDh commands are common across Infineon and Micron. None of the Winbond devices listed in **Table 1** support DDR read.

Infineon supports 4-byte address Read 13h, Fast Read 0Ch, Read Dual Out 3Ch, Read Quad Out 6Ch, Dual I/O Read BCh, and Quad I/O Read ECh commands on all densities, while Micron and Winbond do not support them on 128 Mbit 3.0 V SPI devices that only require 24-bit or 3-byte addresses.

Table 3 Read Flash Array Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
Read	03h	03h	03h
Fast Read	0Bh	0Bh	0Bh
Read Dual Out	3Bh	3Bh	3Bh
Read Quad Out	6Bh	6Bh	6Bh
Dual I/O Read	BBh	BBh	BBh
Quad I/O Read	EBh	EBh	EBh
DDR Fast Read	0Dh **(1)**	0Dh **(2)**	—
DDR Dual I/O Read	BDh **(1)**	BDh **(2)**	—
DDR Quad I/O Read	EDh **(1)**	EDh **(2)**	—
Read (4-byte address)	13h	13h **(2)**	13h **(3)**
Fast Read (4-byte address)	0Ch	0Ch **(2)**	0Ch **(3)**
Read Dual Out (4-byte address)	3Ch	3Ch **(2)**	3Ch **(3)**
Read Quad Out (4-byte address)	6Ch	6Ch **(2)**	6Ch **(3)**
Dual I/O Read (4-byte address)	BCh	BCh **(2)**	BCh **(3)**
Quad I/O Read (4-byte address)	ECh	ECh **(2)**	ECh **(3)**

Note:

1. *Infineon S25FL127S does not support DDR.*
2. *Micron N25Q128A does not support DDR or 4-byte address read commands.*
3. *Winbond W25Q128BV and W25Q128FV do not support 4-byte address read commands.*

2.3 Program Flash Array

Page Program 02h and Quad Page Program 32h commands are common to all manufacturers for programming the flash array.

Infineon and Micron also support the 4-byte address Page Program 12h and Quad Page Program 34h commands.

Table 4 Program Flash Array Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
Page Program	02h	02h	02h
Page Program (4-byte address)	12h	12h	-
Quad Page Program	32h	32h	32h
Quad Page Program – Alternate instruction (3- or 4-byte address)	38h	38h **(1)**	— **(2)**
Quad Page Program (4-byte address)	34h	34h	—
Program Suspend	85h **(3)**	75h	75h
Program Resume	8Ah **(4)**	7Ah	7Ah

Note:

1. *Micron N25Q128A does not support 4-byte address commands.*
2. *If QPI is supported, Winbond uses command code 38h to Enter QPI Mode instead of as an alternate instruction for Quad Page Program.*
3. *Infienon uses different commands for Program Suspend 85h and Erase Suspend 75h while Micron and Winbond use the same command.*
4. *Infineon uses different commands for Program Resume 8Ah and Erase Resume 7Ah while Micron and Winbond use the same command.*

2.4 Erase Flash Array

The 4-kB Parameter Sector Erase 20h, Sector Erase D8h, Erase Suspend 75h, and Erase Resume 7Ah commands are common to all manufacturers for erase operations. The Bulk Erase C7h command is common to all manufacturer devices except the Micron N25Q00AA, which requires the Die Erase C4h command instead. While certain Micron N25Q512A part numbers support the Bulk Erase C7h, the Die Erase C4h command is always supported.

Also, since the Infineon S70FL01GS consists of two (2) S25FL512S die with independent chip selects, the Bulk Erase C7h command must be issued to each device.

Infineon and Micron also support the 4-byte address 4-kB Parameter Sector Erase 21h and Sector Erase DCh commands.

Unlike Micron and Winbond SPI flash devices having uniform 4-kB Parameter and uniform 64-kB sector architectures, Infineon FL-S family SPI flash devices have either hybrid 4-kB and uniform 64-kB sector architecture or uniform 256-kB sectors.

Core 3.0 Volt SPI Commands

Infineon S25FL127S, S25FL128S, and S25FL256S are available as hybrid sector architecture or uniform 256-kB sector devices depending on the ordering part number model. Infineon S25FL512S and S70FL01GS are only offered with uniform 256-kB sectors.

Table 5 Erase Flash Array Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
4-kB Parameter or 4-kB Uniform Sector Erase	20h	20h	20h
4-kB Parameter or 4-kB Uniform Sector Erase (4-byte address)	21h	21h	—
Sector / Block Erase 64 kB or 256 kB	D8h	D8h	D8h
Sector / Block Erase 64 kB or 256 kB (4-byte address)	DCh	DCh	—
Bulk or Chip Erase	C7h / 60h	C7h	C7h / 60h
Bulk Erase	60h	—	60h
Erase Suspend	75h	75h	75h
Erase Resume	7Ah	7Ah	7Ah

Note:

1. *Infineon S25FL512S and S70FL01GS do not support 4-kB sectors.*
2. *For Infineon, the Sector Erase D8h and DCh commands will erase a 64-kB or 256-kB uniform sector depending on the SPI flash device density and model.*
3. *Micron N25Q00AA does not support the Bulk Erase C7h command and only certain N25Q512A part numbers support the Bulk Erase C7h command.*
4. *Only Micron N25Q512A and N25Q00AA support the Die Erase C4h command.*
5. *Micron N25Q128A does not support 4-byte address commands.*
6. *Micron N25Q00AA does not support the 4-kB Erase command 21h with 4-byte address.*

2.5 Write and Register Access

All of the manufacturers support the following Write and Register Access commands: Write Enable 06h, Write Disable 04h, Read Status Register 05h, and Write Register 01h.

Status and configuration registers command operations require customization for each respective manufacturer because of register bit and operational differences. For example, Infineon, Micron, and Winbond have the same 8-bit Status Register 1 accessed with the Read Status Register 05h and Write Register 01h commands, but the definition of Status Register 1 bit 6 and bit 5 differ for each.

Table 6 Write and Register Access Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
Write Enable	06h	06h	06h
Write Disable	04h	04h	04h
Read Status Register-1	05h	05h	05h
Read Configuration Register 1	35h	—	35h **(1)**
Write Register (Status-1 and Configuration-1)	01h	01h	01h
Read Status Register-2	07h	—	—
Write Status Register-2	—	—	31h **(2)**
Read Status Register-3	—	—	15h **(2)**
Write Status Register-3	—	—	11h **(2)**
Clear Status Register 1	30h	50h	
Bank Register Access	B9h		— **(3)**
Bank Register Read	16h	C8h	C8h
Bank Register Write	17h	C5h	C5h
Enter 4-Byte Address Mode	—	B7h **(4)**	B7h **(5)**
Exit 4-Byte Address Mode	—	E9h **(4)**	E9h **(5)**

Note:

1. *Winbond refers to the 35h command as Read Status Register-2.*
2. *Winbond W25Q128BV does not support the Write Status Register-2 31h, Read Status Register-3 15h, Write Status Register-3 11h commands.*
3. *Winbond uses the B9h command code for Deep Power-Down.*
4. *Micron N25Q128A does not support 4-byte address commands.*
5. *Winbond W25Q128BV and W25Q128FV do not support 4-byte address commands.*

2.5.1 Bank / Extended Address Register

Infineon, Micron, and Winbond all provide a Bank or Extended Address Register option for augmenting 3-byte address commands with higher order address bits above A23 as shown in **Table 7**, **Table 8**, and **Table 9**. Micron and Winbond can support up to eight (8) register bits for the address while Infineon uses bit 7 EXTADD=0 to enable the Bank Address.

Infineon controls reading the Bank Address Register (BAR) and writing the entire or the address portion of the BAR using the following commands: Bank Register Access (BRAC) B9h, Write Register (WRR) 01h, Bank Register Read (BRRD) 16h, and Bank Register Write (BRWR) 17h.

Table 7 Infineon Bank Address Register (BAR)

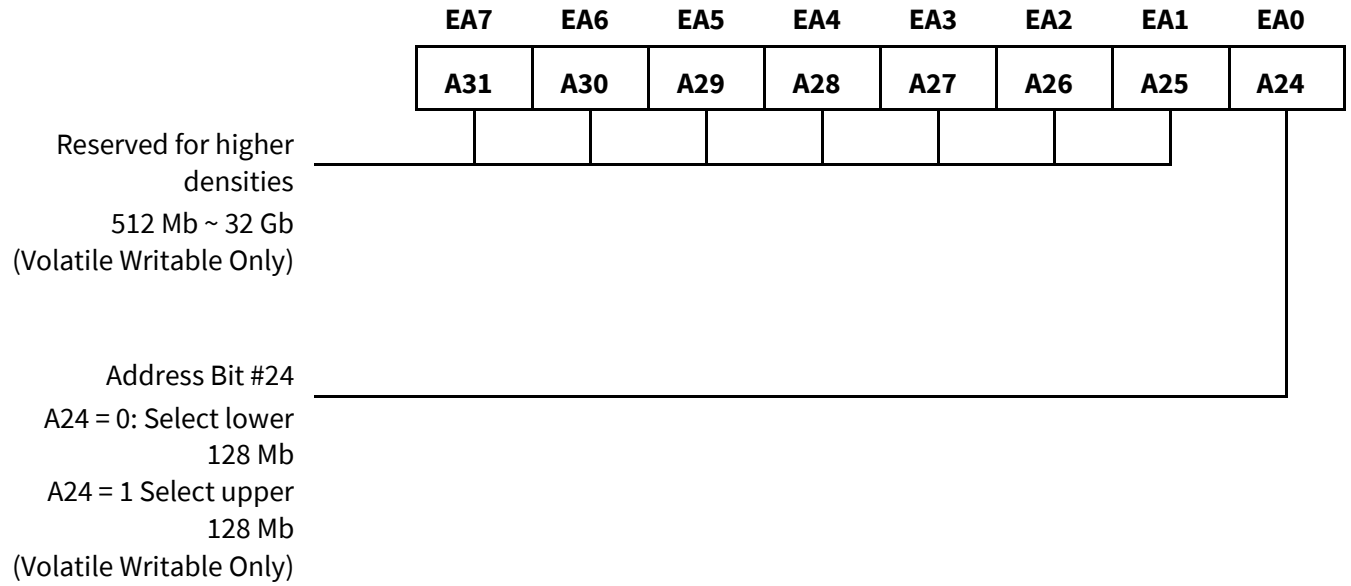
Bits	Field Name	Function	Type	Default State	Description
7	EXTADD	Extended Address Enable	Volatile	0b	1 = 4-byte (32 bits) addressing required from command 0 = 3-byte (24 bits) addressing from command + Bank Address
6 to 2	RFU	Reserved	Volatile	00000b	Reserved for Future Use
1	BA25	Bank Address	Volatile	0	A25 for 512 Mb device
0	BA24	Bank Address	Volatile	0	A24 for 512 Mb device

Micron and Winbond read and write their respective Extended Address Register using the Read Extended Address Register C8h and Write Extended Address Register C5h command codes.

Table 8 Micron Extended Address Register

Bit	Name	Settings	Description
7:3	A[31:25]	000000	Reserved
2:0	A[26:24]	111 = Highest 128 Mb segment 110 = Seventh 128 Mb segment 101 = Sixth 128 Mb segment 100 = Fifth 128 Mb segment 011 = Fourth128 Mb segment 010 = Third 128 Mb segment 001 = Second 128 Mb segment 000 = Lowest 128 Mb segment	Enables specified 128 Mb memory segment. The default setting (lowest) can be changed to the highest 128 Mb segment using bit 1 of the nonvolatile configuration register.

Table 9 Winbond Extended Address Register



2.5.2 Extended Address Mode

Infineon, Micron, and Winbond all provide a bit for controlling or enabling a 4-byte address mode for legacy SPI commands. Once the extended address mode is enabled, all legacy commands are expected to supply a 4-byte or 32-bit address instead of 3-byte address.

Infineon enables 4-byte legacy command addressing by setting Bank Address Register bit 7 EXTADD=1 also shown in **Table 7**. Once Bank Address Register bit 7 EXTADD=1, the Bank Address stored in the remaining bits is ignored for addressing.

Since 3-byte addressing is the default, Micron enables the 4-byte addressing mode by setting Nonvolatile Configuration Register bit 0 = 0. Micron's proprietary Read Nonvolatile Configuration Register B5h and Write Nonvolatile Configuration Register B1h commands are used to control the Nonvolatile Configuration Register setting.

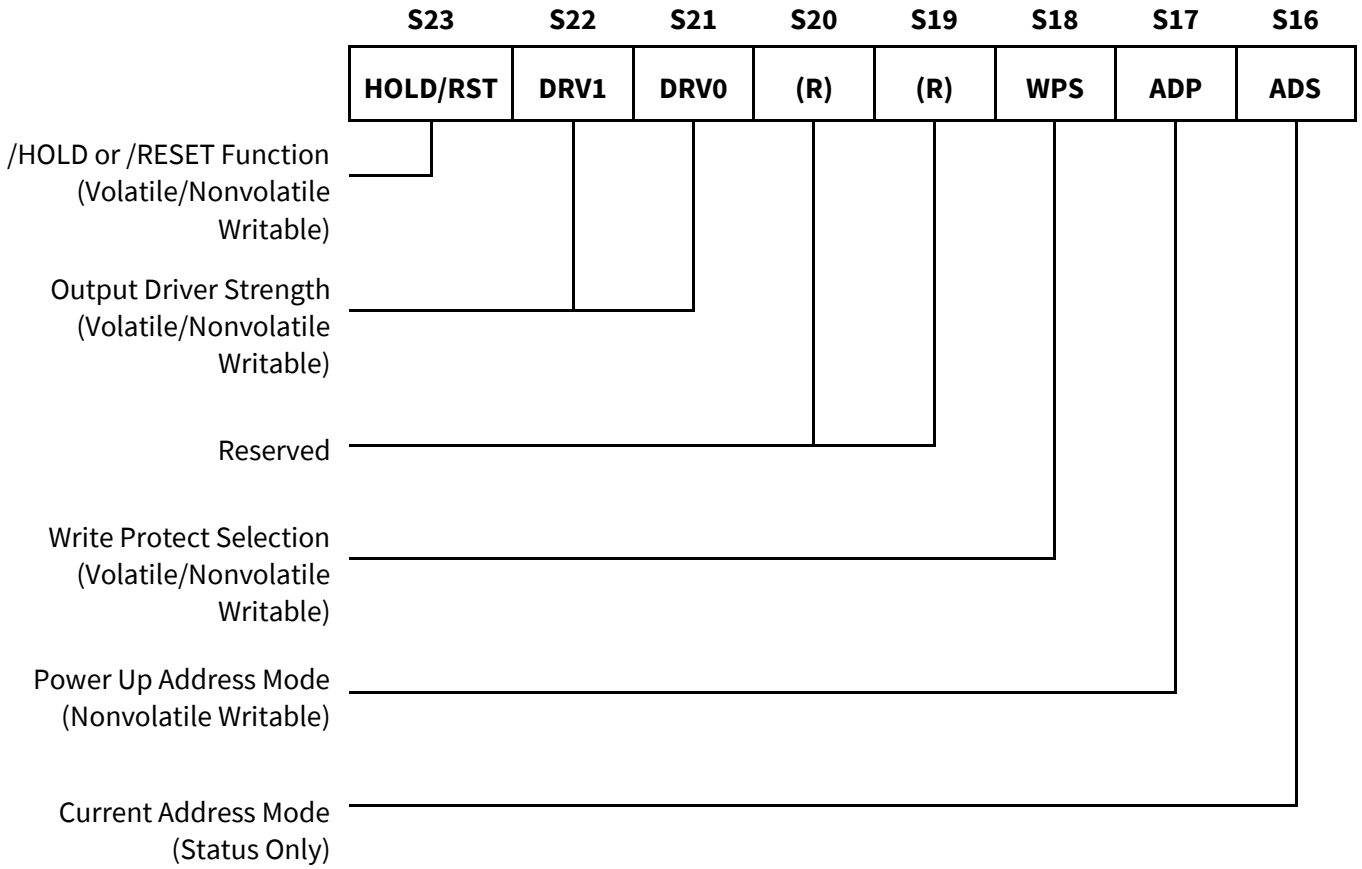
Table 10 Micron Nonvolatile Configuration Register Bit Definitions

Bit	Name	Settings	Description
715:12	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets the maximum allowed frequency and guarantees backward compatibility.
11:9	XIP mode at power-on-reset	000 = XIP; Fast Read 001 = XIP; Dual Output Fast Read 010 = XIP; Dual I/O Fast Read 000 = XIP; Quad Output Fast Read 000 = XIP; Quad I/O Fast Read 101 = Reserved	Enables the device to operate in the selected XIP mode immediately after power-on-reset.

Bit	Name	Settings	Description
		110 = Reserved 111 = Disabled (Default)	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 Ohms (Default)	Optimizes impedance at $V_{CC}/2$ output voltage.
5	Reserved	X	Don't Care
4	Reset/Hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)
3	Quad I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protocol)	Enables or disables quad I/O protocol.
2	Dual I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protocol)	Enables or disables dual I/O protocol.
1	128 Mb segment select	0 = Upper 128 Mb segment 1 = Lower 128 Mb segment (Default)	Selects a 128 Mb segment as default for 3B address operations. See also the extended address register.
0	Address bytes	0 = Enable 4B address 1 = Enable 3B address (Default)	Defines the number of address bytes for a command.

Winbond W25Q256FV and W25Q257FV power up in either 3-byte Address Mode or 4-byte Address Mode depending on the Non-Volatile Status Register Bit ADP (S17) setting as shown in **Table 11**. If ADP=0, the device will operate in the 3-byte Address Mode; if ADP=1 (factory default value), the device will operate in the 4-byte Address Mode. The non-volatile ADP power up state can be changed using the Winbond Write Status Register-3 11h command.

Table 11 Winbond Status Register 3



2.6 Reset

Infineon only supports the Software Reset F0h command unlike both the Micron and Winbond devices using the Reset command sequence of Reset Enable 66h followed by Reset Memory 99h.

Reset Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
Software Reset	F0h **(1)**	—	—
Reset Enable	—	66h	66h
Reset Memory	—	99h	99h
Mode Bit Reset	FFh	—	FFh **(2)**
Exit QPI Mode			FFh **(3)**

Note:

1. *Infineon only supports the Software Reset F0h command code.*
2. *Only supported by Winbond W25Q128BV.*
3. *Winbond W25Q128BV does not support QPI Mode.*

2.7 One Time Program (OTP) Array

Both Infineon and Micron support the same One Time Program Array (OTP) Program 42h and OTP Read 4Bh commands. Infineon has 1024 bytes of OTP array space whereas Micron only supports 64 bytes.

Table 12 OTP Commands

Command Description	Infineon S25FL-S Command Code	Micron N25Q Command Code	Winbond W25Q Command Code
OTP Program	42h	42h	42h
OTP Read	4Bh	4Bh	48h

3 Summary

Portable firmware or driver software implementations can leverage core SPI flash commands to minimize proprietary code or branches for each manufacturer. However, register commands and definitions for status, configuration, and extended addressing require some customization for each specific manufacturer.

References

[1] **Serial NOR Flash Memory**

[2] Infineon Datasheets:

- **S25FL128S and S25FL256S**
- **S25FL512S**
- **S70FL01GS**

[3] Micron Datasheets:

- N25Q128A 3V, Multiple I/O, 4KB Sector Erase Rev. L - 06/2012
- N25Q256A 3V, Multiple I/O, 4KB Sector Erase Rev. T - 03/14
- N25Q512A 3V, Multiple I/O, 4KB Sector Erase Rev. T - 08/14
- N25Q00AA 3V, Multiple I/O, 4KB Sector Erase Rev. I - 02/2013

[4] Winbond Datasheets:

- W25Q128BV October 03, 2013 Revision H
- W25Q128FV October 09, 2013 Revision I
- W25Q256FV October 16, 2013 Revision G
- W25Q257FV November 07, 2013 Revision A

Revision history

Document version	Date of release	Description of changes
**	2015-03-23	Initial version
*A	2015-09-22	Updated in template
*B	2017-07-12	Updated logo and Copyright
*C	2018-08-10	Updated template
*D	2021-03-25	Updated to Infineon template

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