AN98508

Cypress Serial Peripheral Interface (SPI) FL Flash Layout Guide

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Associated Part Families: S25FL, S70FL, S25FS, S70FS

AN98508 outlines PCB layout recommendations for Cypress SPI flash devices, including S25FL-P, S70FL-P, S25FL-S, S70FL-S, S25FS-S, and S70FS-S flash families.

Contents

1 Introduction

The Cypress serial peripheral interface (SPI) flash devices are high speed synchronous access non-volatile memory devices. Standard high speed layout practices should be followed when performing printed circuit board (PCB) design with SPI flash. This application note outlines PCB layout recommendations for Cypress SPI flash devices, including S25FL-P, S70FL-P, S25FL-S, S70FL-S, S25FS-S and S70FS-S flash families.

2 Basic SPI Flash Connectivity

All S25FL/S25FS devices feature one flash die per package and are enabled via a single chip select control input. All S70FL/S70FS devices feature two identical die per package which are individually enabled via two chip select control inputs and all other control inputs and I/O are shared between die. Figure 1 and Figure 2 illustrate basic Host to SPI Flash configuration options for S25FL flash and S70FL flash, respectively.

Figure 1. Simplified Connection Diagrams for S25FL Single and Multi I/O Configurations

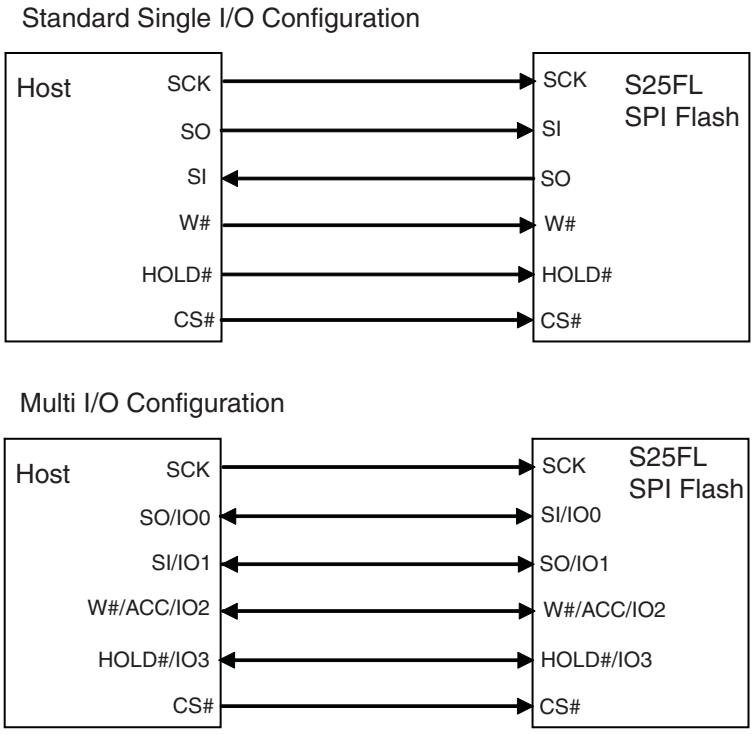
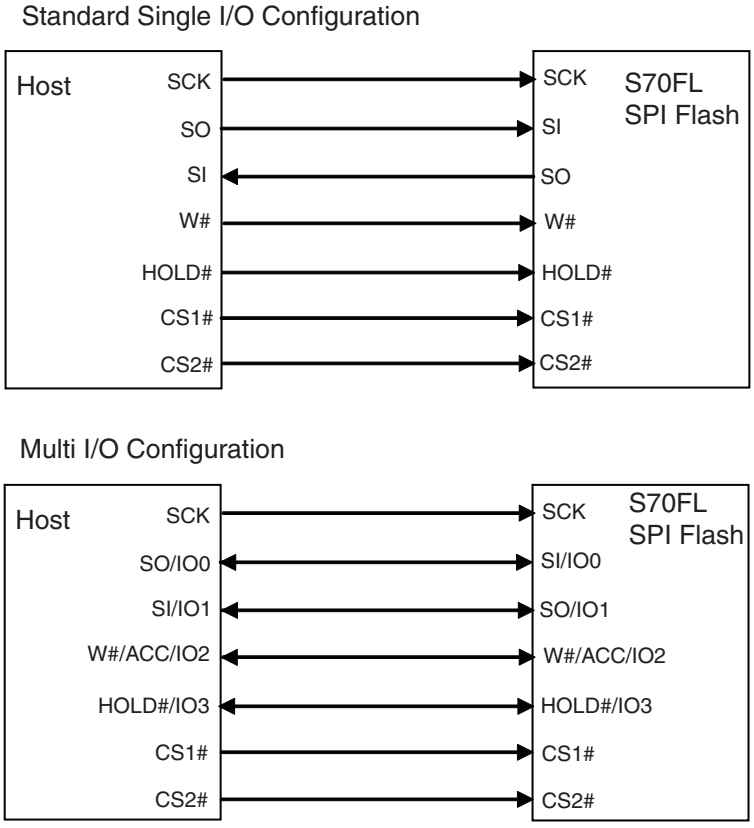
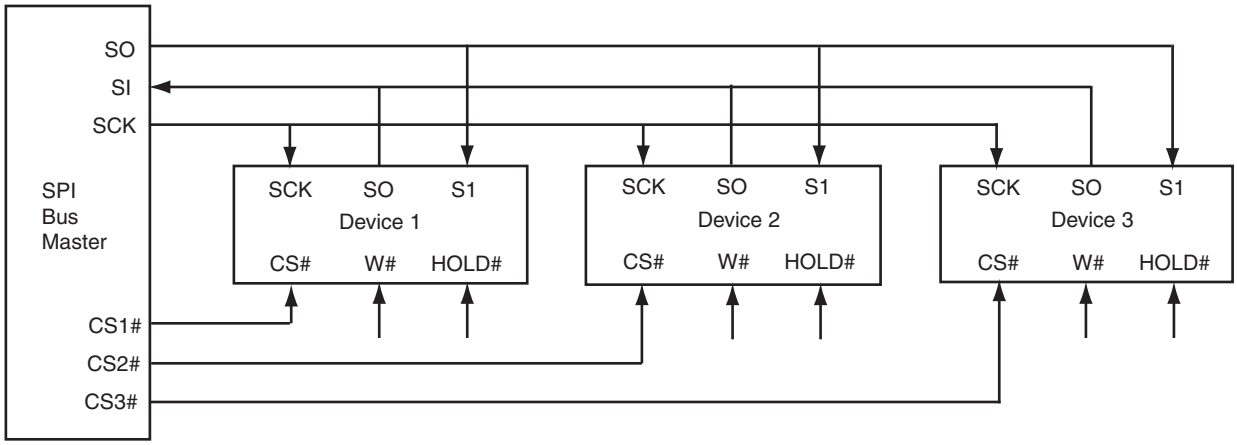


Figure 2. Simplified Connection Diagrams for S70FL Single and Multi I/O Configurations



Often multiple SPI devices are connected to a single host. Figure 3 illustrates such a configuration. Use of a dual die S70FL device can be viewed as use of Device 1 and Device 2 in Figure 3.

Figure 3. Simplified Multi- SPI Device Connection Diagram



Many SPI flash applications do not utilize the ACC, WP# or HOLD# functions. In those applications where an input is not utilized, the unused I/O should be pulled up to V_{CC}, or V_{IO} if present, via a suitable resistor, e.g., 4.7 kΩ to 10 kΩ.

3 SPI Flash Packaging

The FL-P and FL-S SPI Flash families provide a user configurable high speed single, dual or quad channel interface to the host controller. Cypress SPI flash are available in a variety of packages, including SOIC-8 and SOIC-16 leaded packages, USON-8 and WSON-8 leadless packages and FAB024 and FAC024 ball grid array (BGA) packages. Table 1 provides a matrix of package options for all FL-P and FL-S devices.

Table 1. Device Availability Matrix

Package \ Density	≤ 16Mbit	32 Mbit	64 Mbit	128 Mbit	256-1024 Mbit
SOIC 8L Narrow Body Pkg Code: SOA008	S25FL204K S25FL208K S25FL216K S25FL116K	S25FL132K	–	–	–
SOIC 8L Wide Body Pkg Code: SOC008	S25FL204K S25FL208K S25FL216K S25FL116K	S25FL032P S25FL132K	S25FL164K	S25FL127S S25FS128S	
SO3 016	–	S25FL032P	S25FL064P S25FL164K	S25FL128P S25FL129P S25FL128S S25FL127S S25FL128K	S25FL256S S25FL512S S25FS256S S25FS512S
SL3 016	–	–	–	–	S70FL256P S70FL01GS S70FS01GS
USON 8L	–	S25FL032P	–	–	–
WSON 8L Pkg Code: WND008	S25FL116K	S25FL132K	S25FL164k	S25FL127S S25FS128S	–
WSON 8L Pkg Code: WNF008	–	S25FL032P	S25FL064P	S25FL128P S25FL129P	–
WSON 8L Pkg Code: WNG008	–	–	–	S25FL128S	S25FL256S
WSON 8L Pkg Code: WNH008	–	–	–	–	S25FS256S S25FS512S S25FL256L
FAB024	S25FL116K	S25FL032P S25FL132K	S25FL064P S25FL164k	S25FL129P S25FL128S S25FL127S	S25FL256S S25FL512S
FAC024	S25FL116K	S25FL032P S25FL132K	S25FL064P S25FL164K	S25FL129P S25FL128S S25FL127S	S25FL256S S25FL512S
ZSA024	–	–	–	–	S70FL256P
other BGA (planned)	–	–	–	–	S25FL512S S70FL512S S70FL01GS

3.1 SPI Flash Package Connection Diagrams

Applicable package connection diagrams are provided in each SPI Flash data sheet. These diagrams are included here in Figure 4 through Figure 17 for reference.

Note: The packaging information is provided as typical examples and the reader should reference the most recent revision of the subject flash datasheet for latest packaging information and signal assignments.

Figure 4. SOIC 8L Narrow Body - S25FL204K/208K/216K/116K/132K

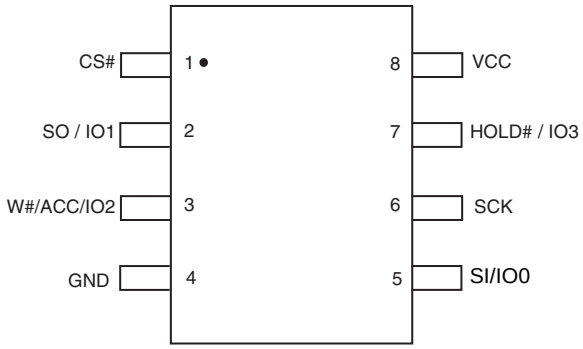


Figure 5. SOIC 8L Wide Body - S25FL204K/208K/216K/116K/032P/132K/164K/127S, S25FS128S

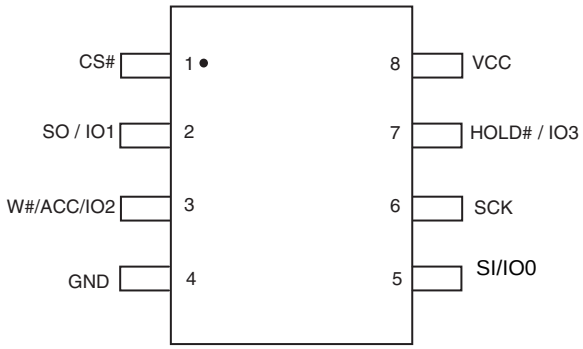


Figure 6. SO3 016 – S25FL128P

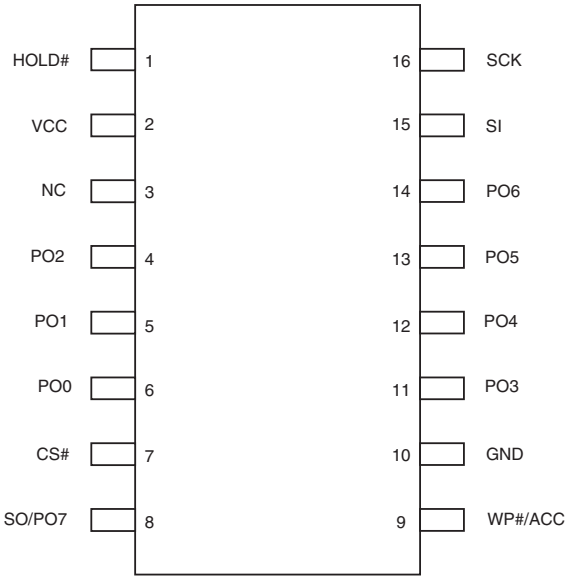


Figure 7. SO3 016 – S25FL032P/064P/164K/127S/129P

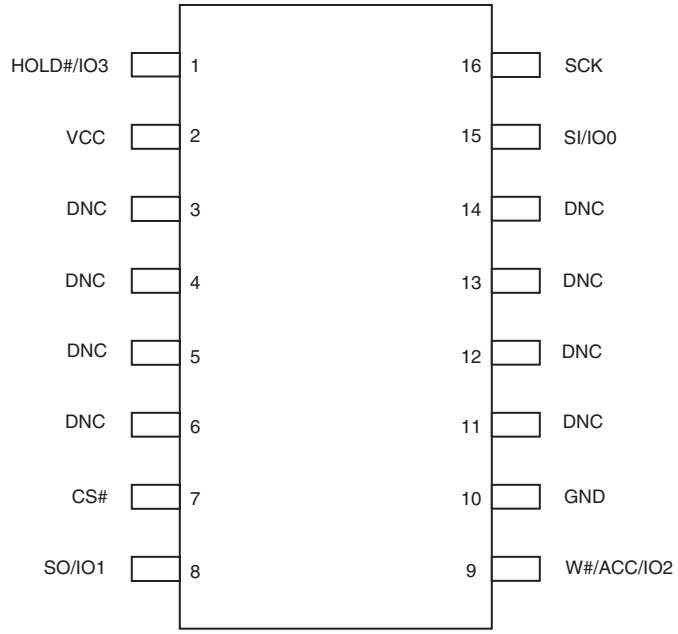


Figure 8. SO3 016 – S29FL128S/256S/512S

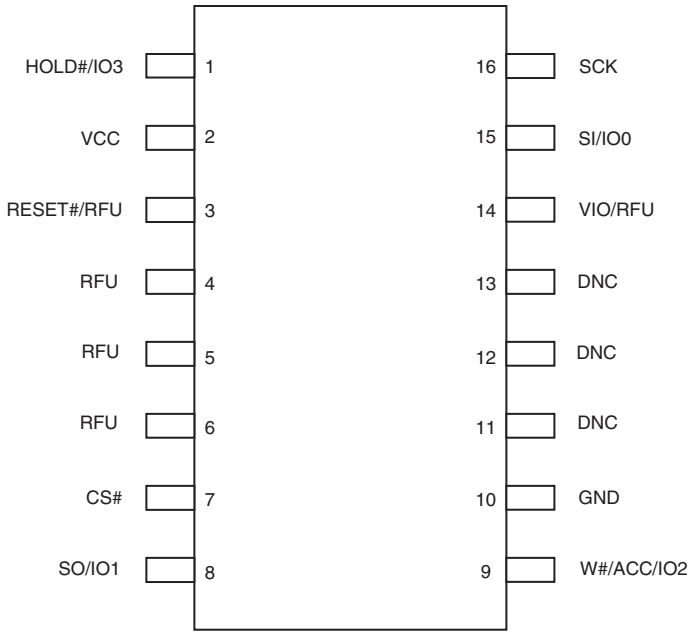


Figure 9. SO3 016 - S25FS256S/512S

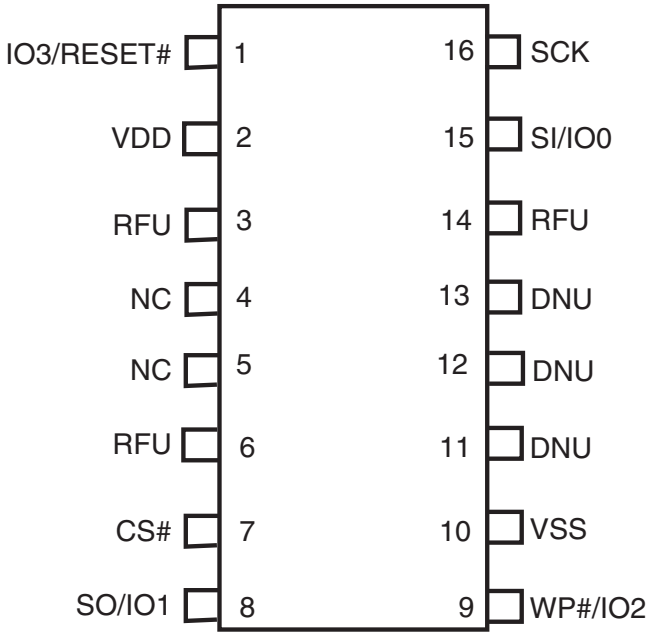


Figure 10. SL3 016 – S70FL256P/01GS

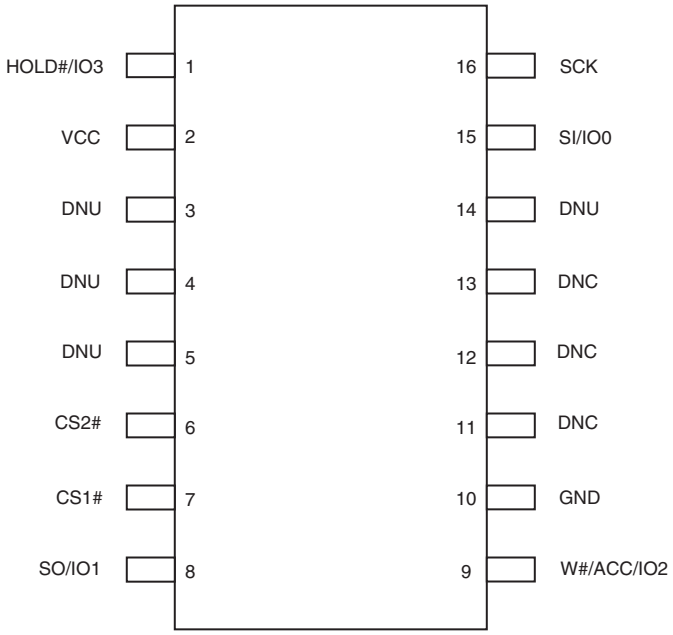


Figure 11. SL3 016 - S70FS01GS

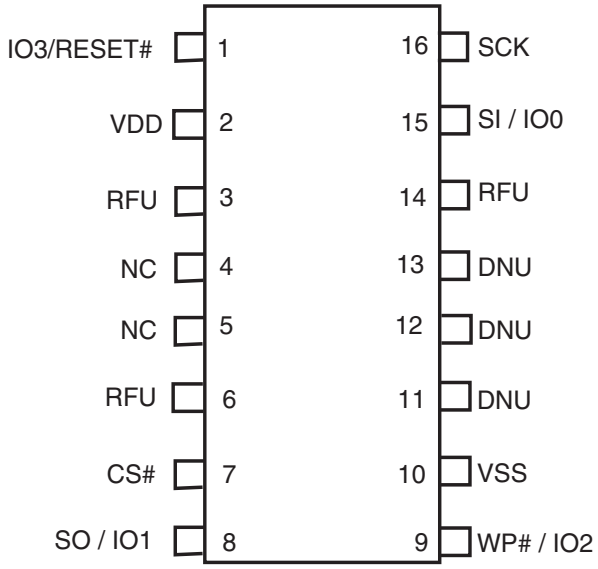


Figure 12. USON 8L – S25FL032P

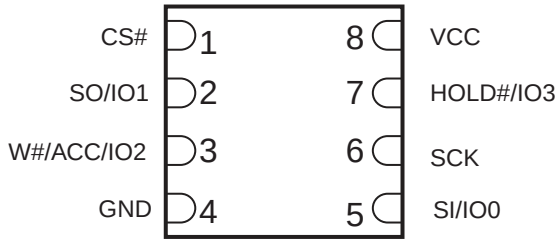


Figure 13. WSON 8L – S25FL128P

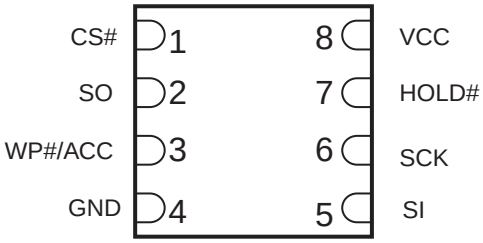


Figure 14. WSON 8L – S25FL032/064/129P, S25FL116K, S25FL128/256S

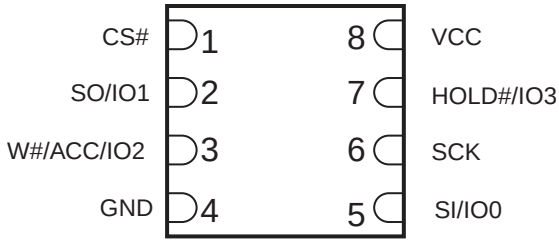
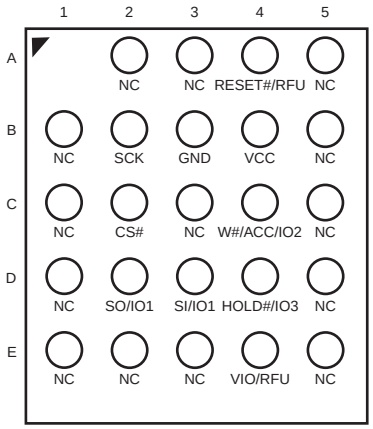
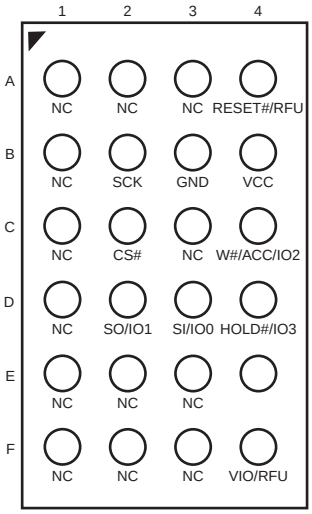


Figure 15. FAB024 – S25FL032/064/129P, S25FL116K, S25FL128/256S



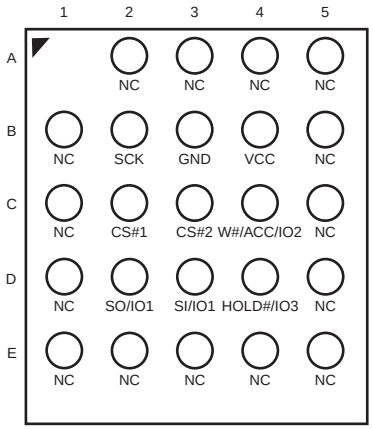
Note:
RESET# and V_{IO} inputs apply to S25FL-S models only.

Figure 16. FAC024 – S25FL032/064/129P, S25FL116K, S25FL128/256S



Note:
RESET# and V_{IO} inputs apply to S25FL-S models only.

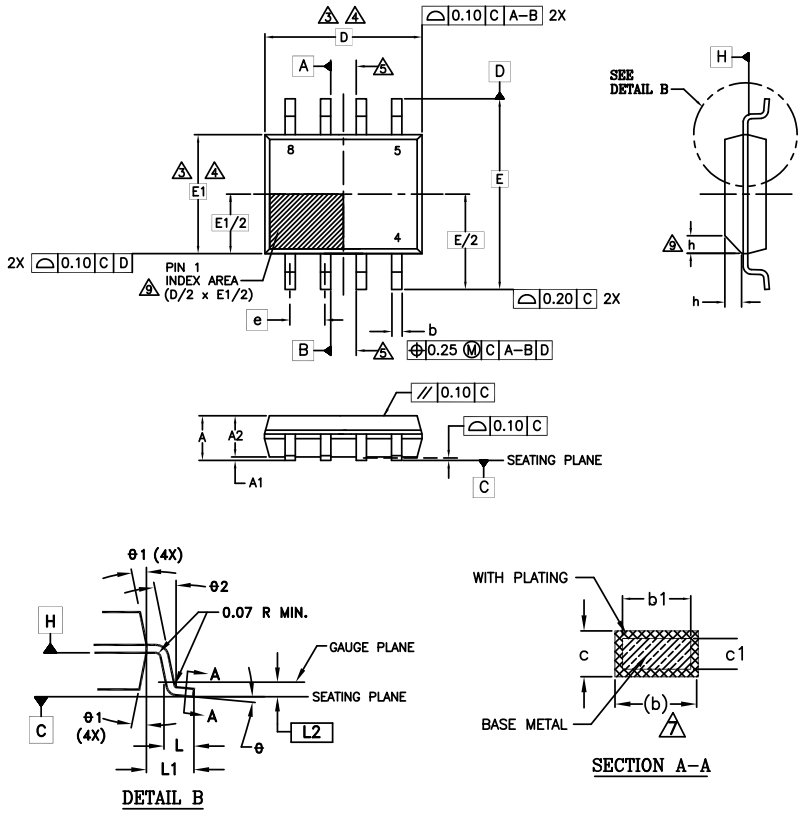
Figure 17. ZSA024 – S70FL256P



3.2 SPI Flash Package Drawings

Applicable package drawings are provided in each SPI Flash data sheet. These drawings are included here in Figure 18 through Figure 29 for reference.

Figure 18. SOIC 8L – Narrow 8-Pin Plastic Small Outline 150-mils Body Width Package (SOA008)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.32	-	-
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	0.89
L1	1.04 REF		
L2	0.25 BSC		
N	8		
h	0.25	-	0.50
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0° REF		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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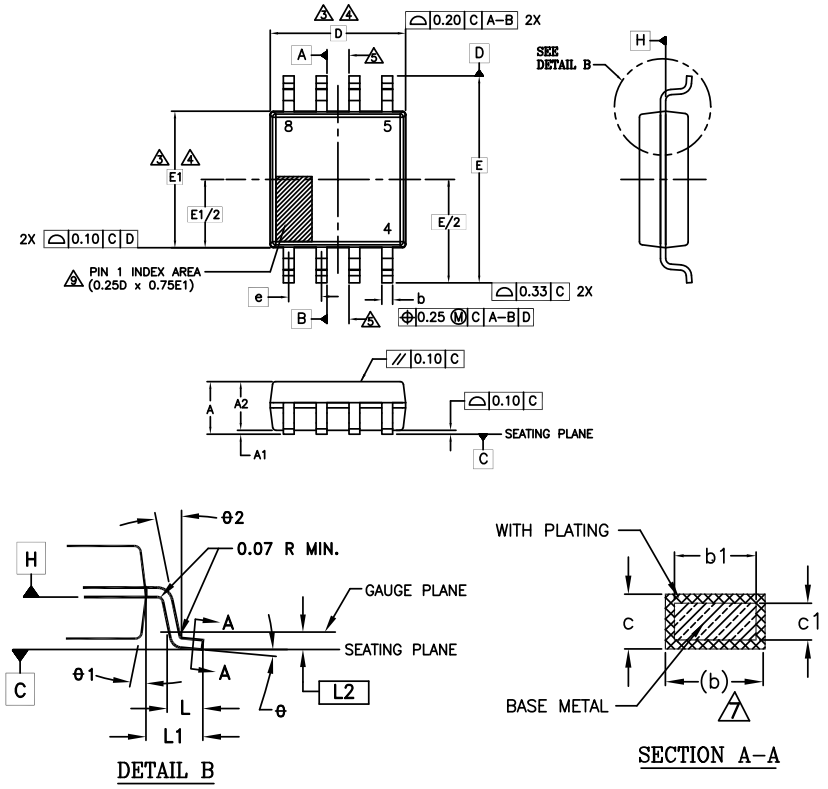
Figure 19. SOIC 8L – Wide 8-Pin Plastic Small Outline 208 mils Body Width Package (SOC008)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.75	-	2.16
A1	0.05	-	0.25
A2	1.70	-	1.90
b	0.36	-	0.48
b1	0.33	-	0.46
c	0.19	-	0.24
c1	0.15	-	0.20
D	5.28 BSC		
E	8.00 BSC		
E1	5.28 BSC		
e	1.27 BSC		
L	0.51	-	0.76
L1	1.36 REF		
L2	0.25 BSC		
N	8		
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0-8° REF		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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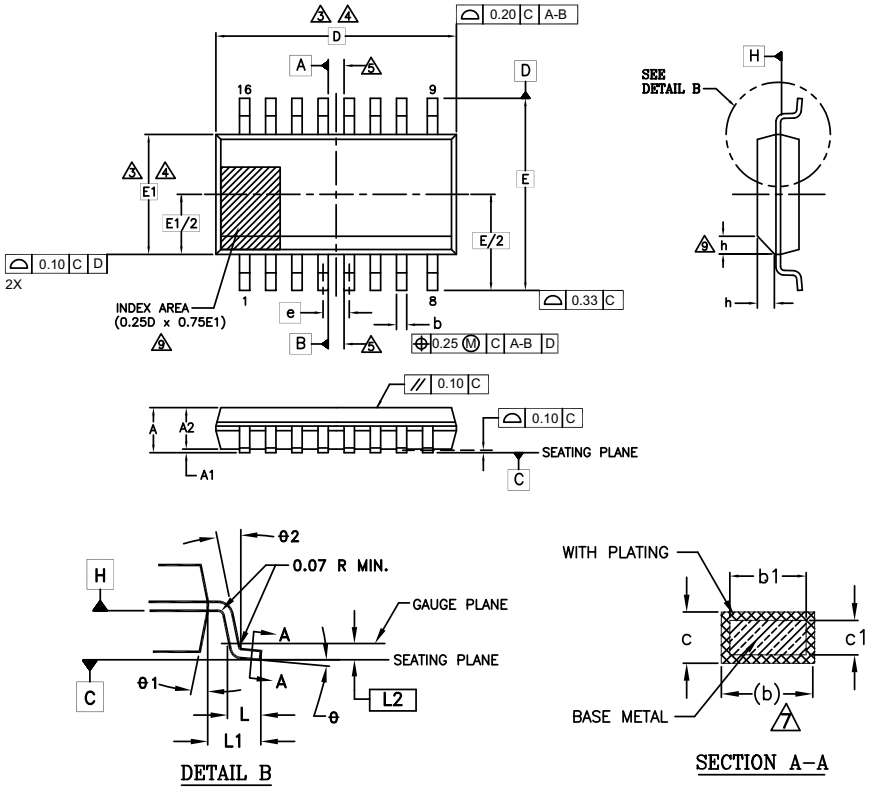
Figure 20. SO3 016 – 16-Pin Wide Plastic Small Outline Package (300 mil Body Width)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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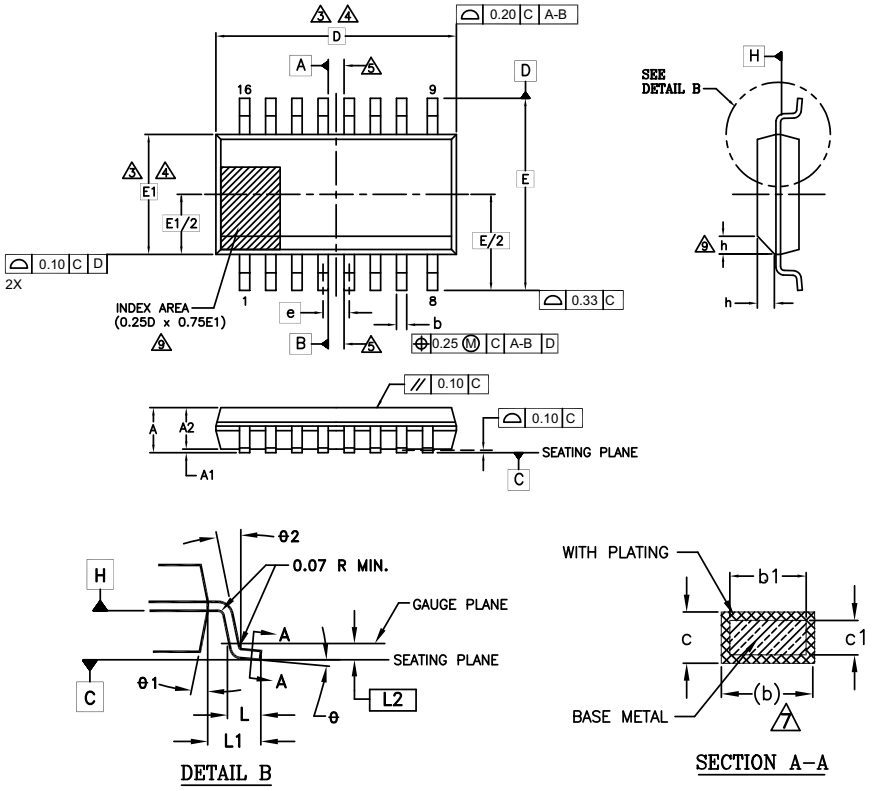
Figure 21. SL3 016 – 16-Pin Wide Plastic Small Outline Package (300 mil Body Width)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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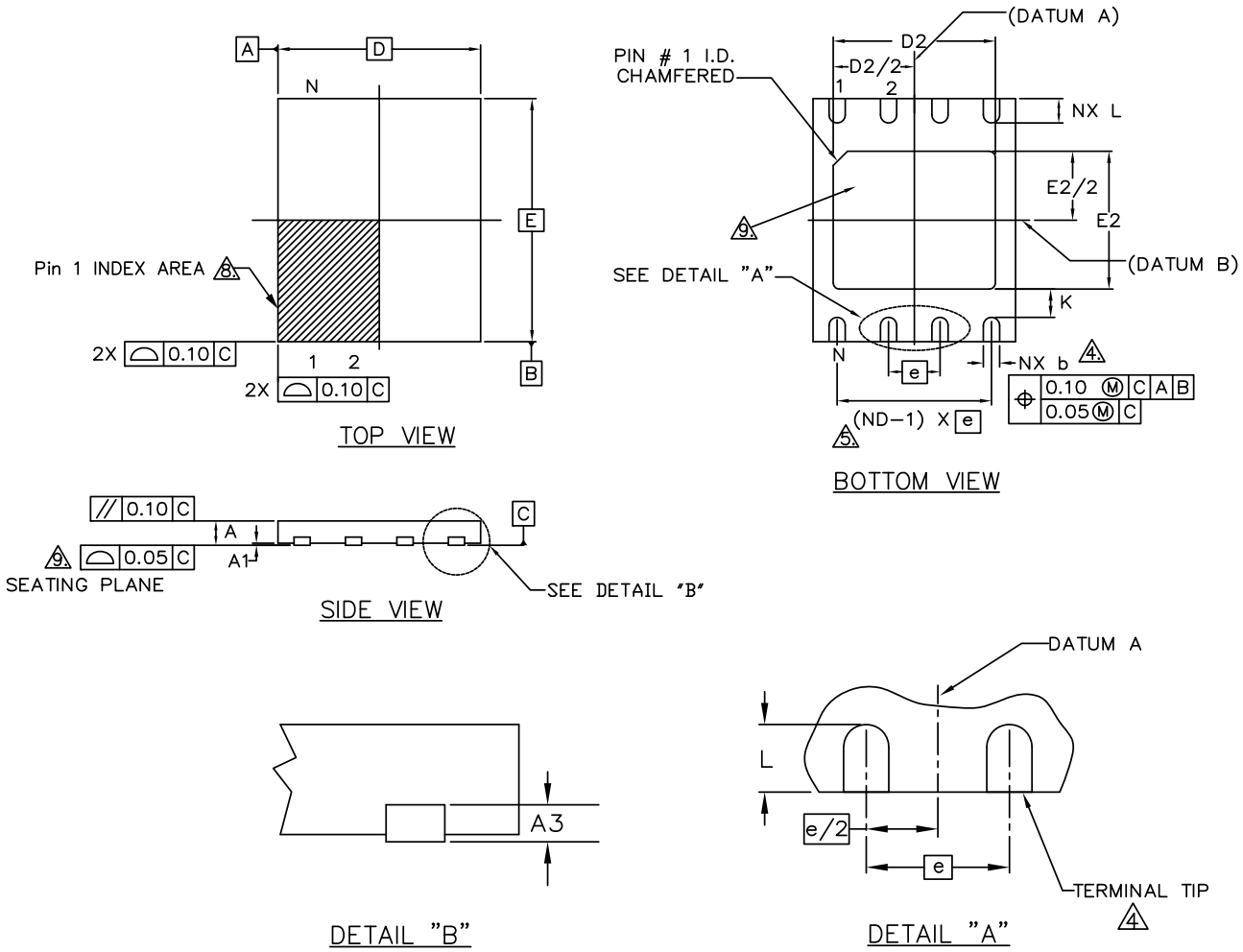
Figure 22. USON 8L - 8-contact (5 x 6 mm) No-Lead Package (UNE008)



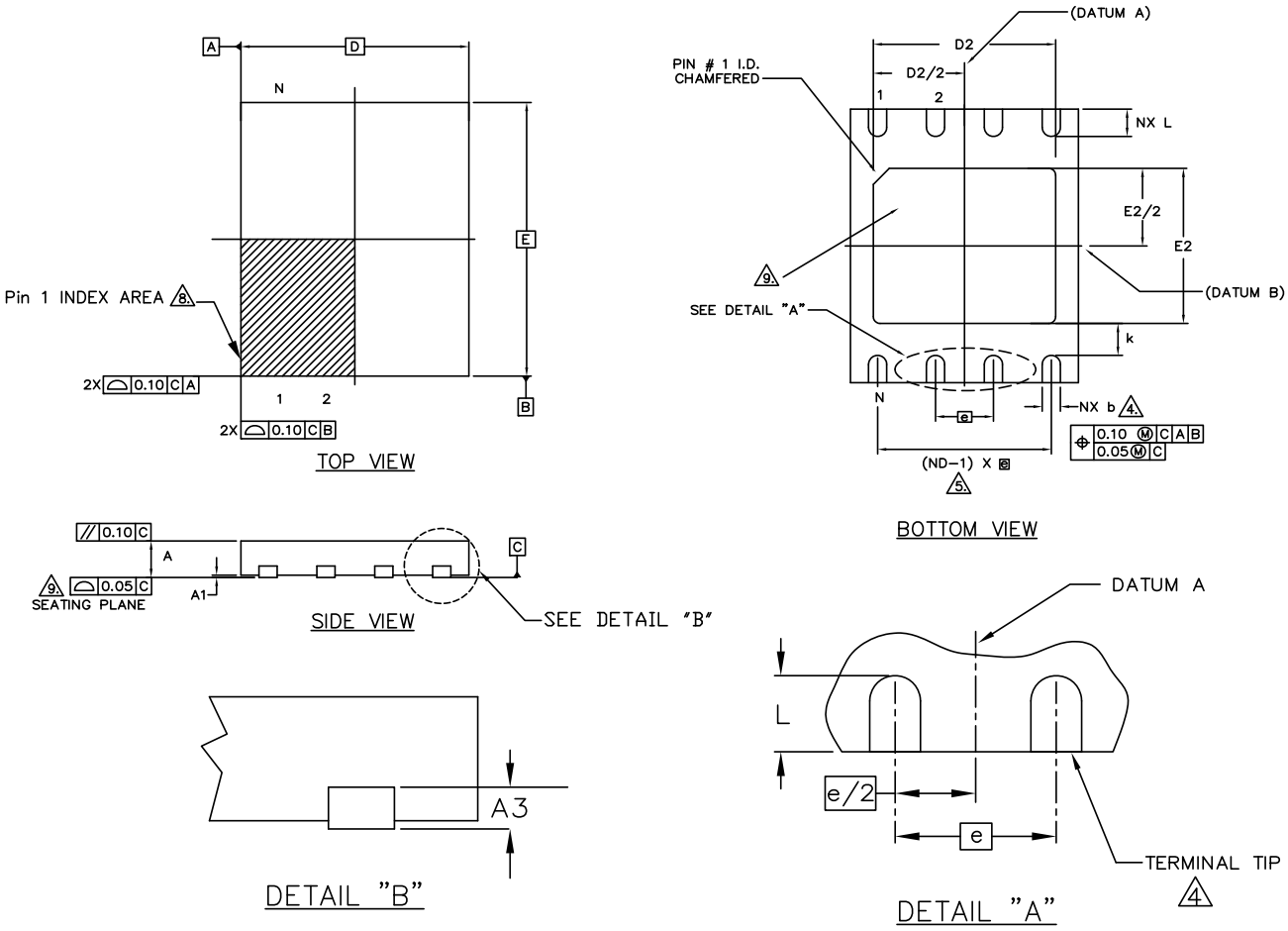
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.55	0.60	0.65
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		5.00 BSC	
E		6.00 BSC	
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

002-18903 Rev. **

Figure 23. WSON 8L - 8-Contact (5 x 6 mm) No-Lead Package (WND008)



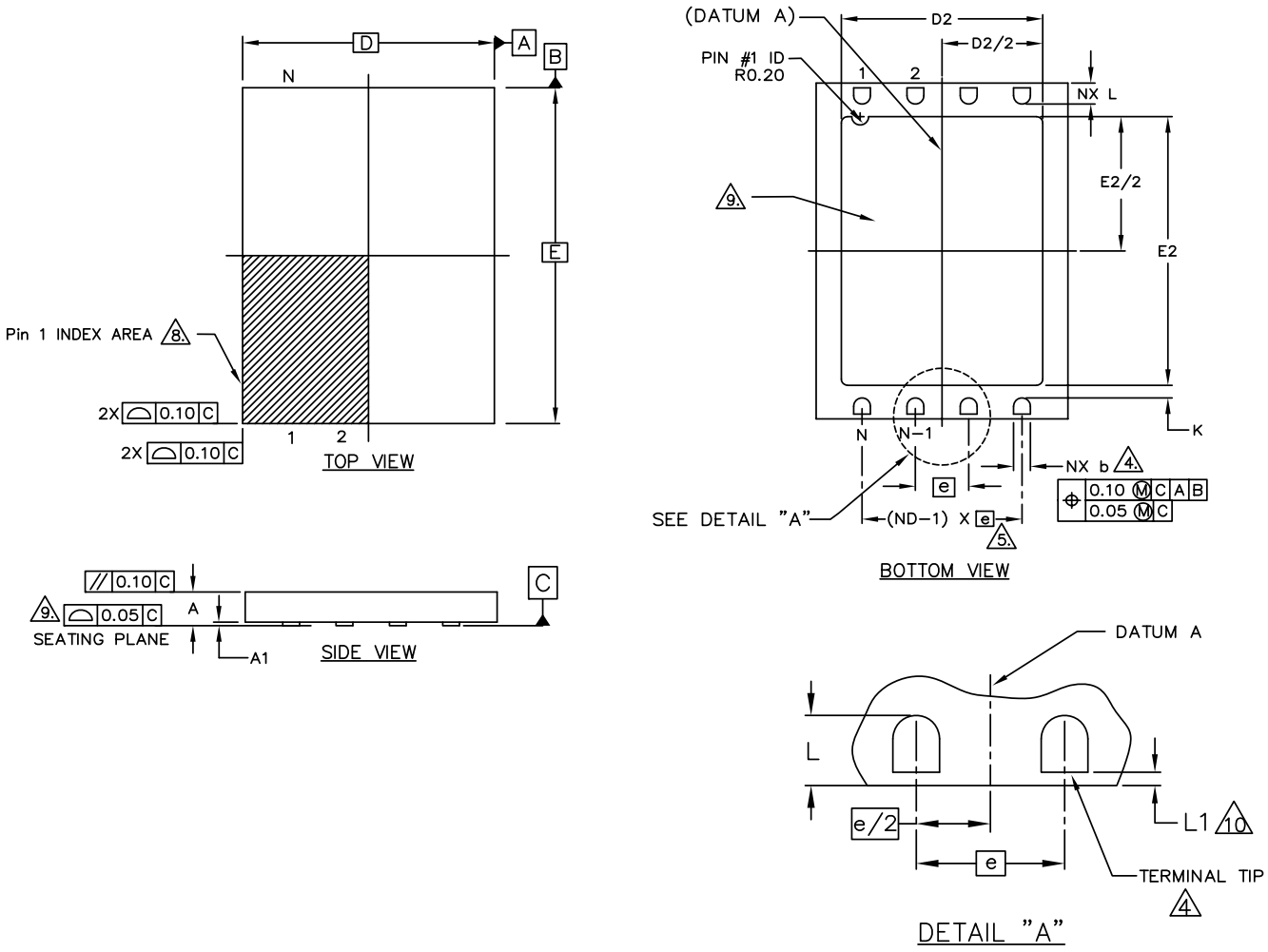
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.55	0.60	0.65
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		5.00 BSC	
E		6.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18755 Rev. **

Figure 24. WSON 8L - 8-Contact (6 x 8 mm) No-Lead Package (WNF008)



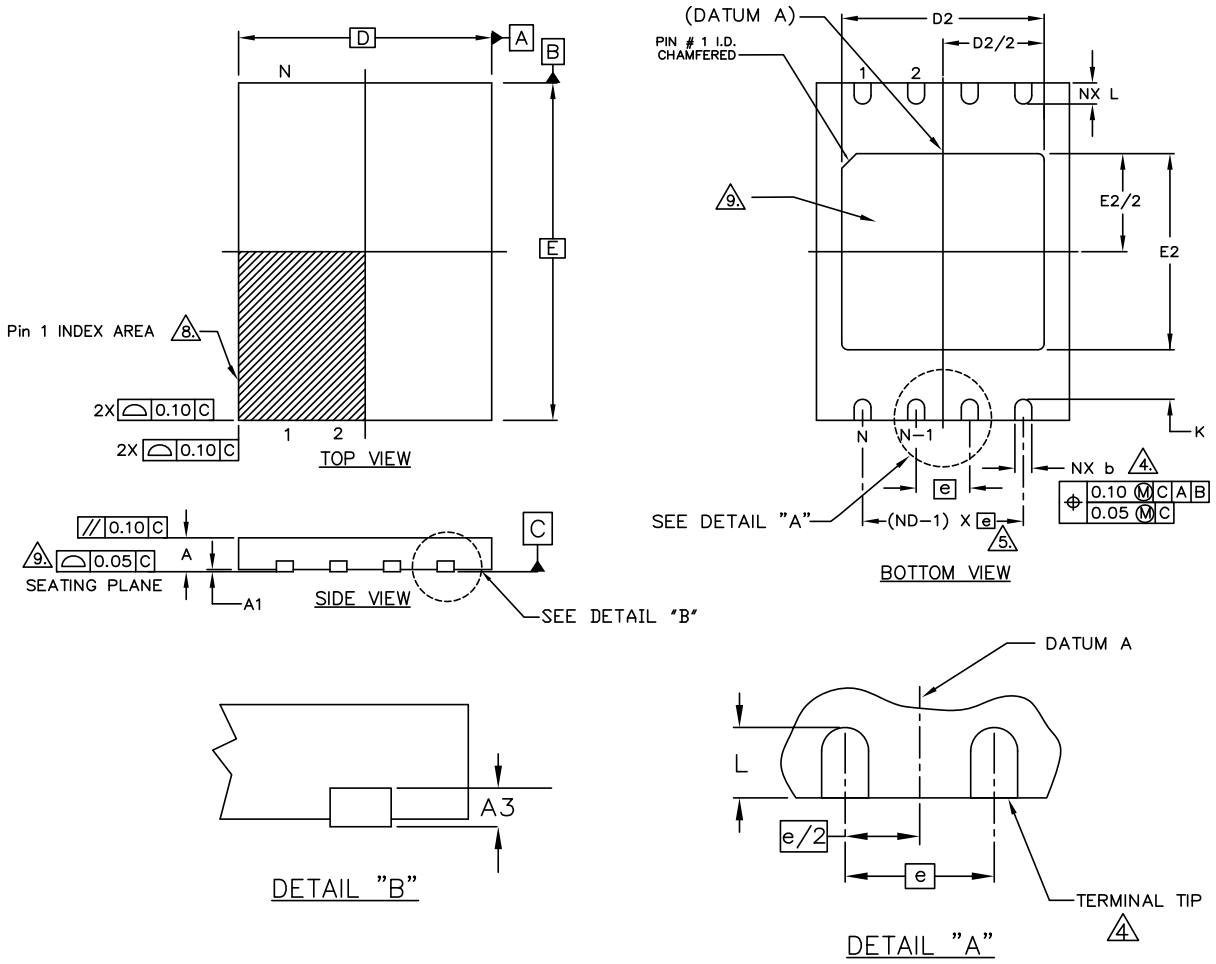
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	4.70	4.80	4.90
E2	5.70	5.80	5.90
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
K		0.20 MIN.	
L1	0.00	-	0.15

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18902 Rev. **

Figure 25. WSON 8L - 8-Contact (6 x 8 mm) No-Lead Package (WNG008)



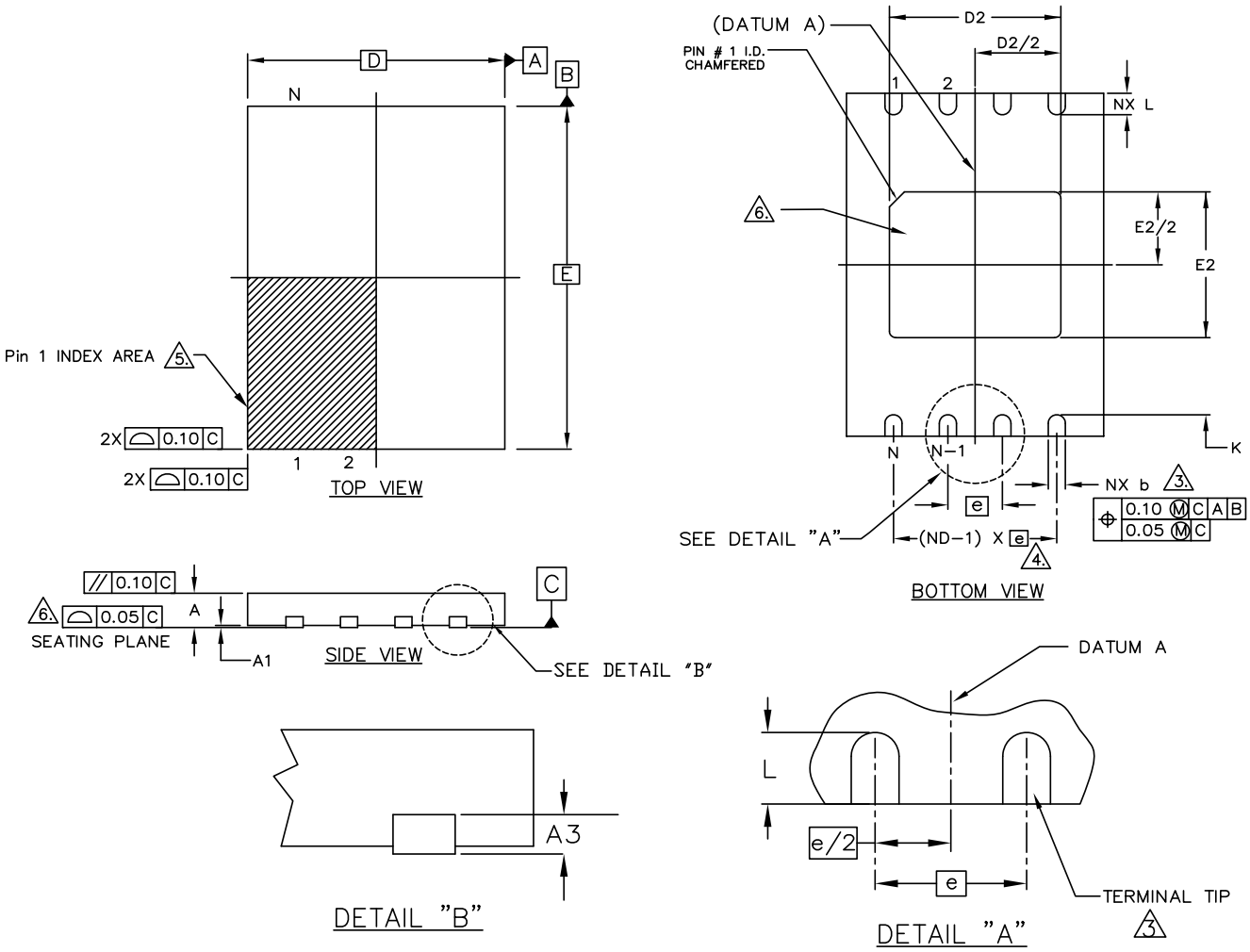
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	4.70	4.80	4.90
E2	4.55	4.65	4.75
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18827 Rev. **

Figure 26. WSON 8L - 8-Contact (6 x 8 mm) No-Lead Package (WNH008)



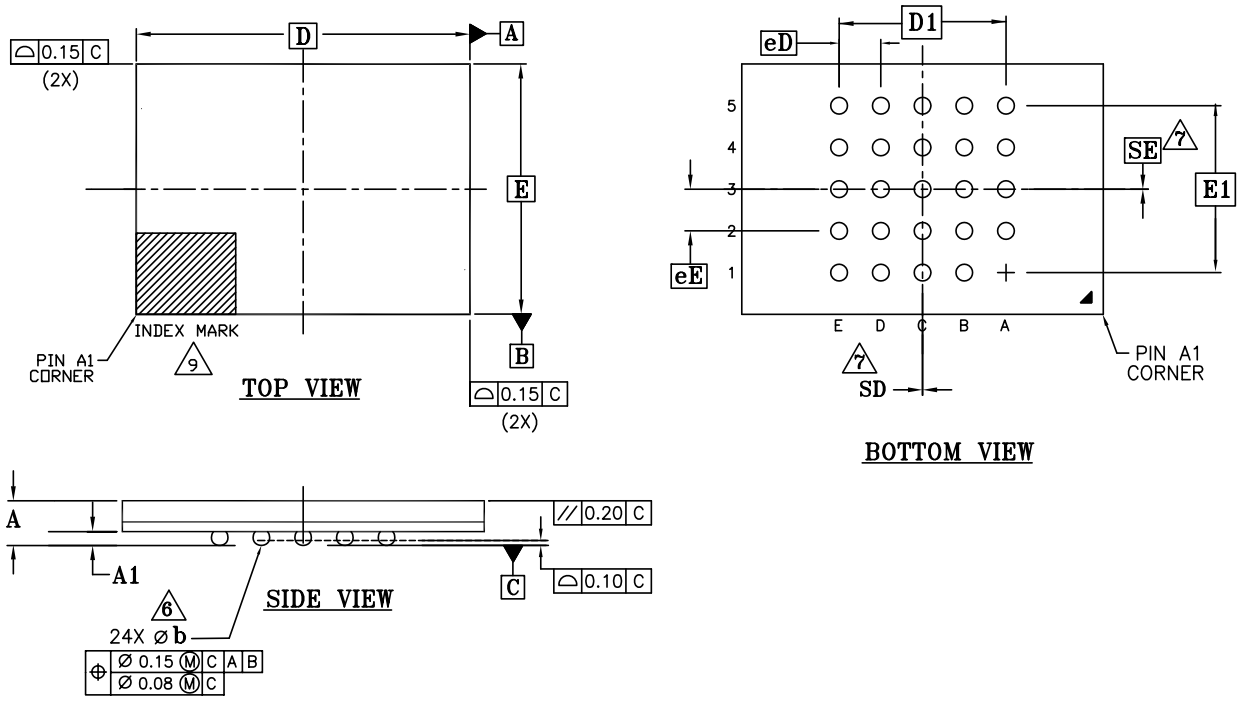
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
K	0.20	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A

002-15552 Rev. *A

Figure 27. FAB024 24-ball Ball Grid Array (6 x 8 mm) Package



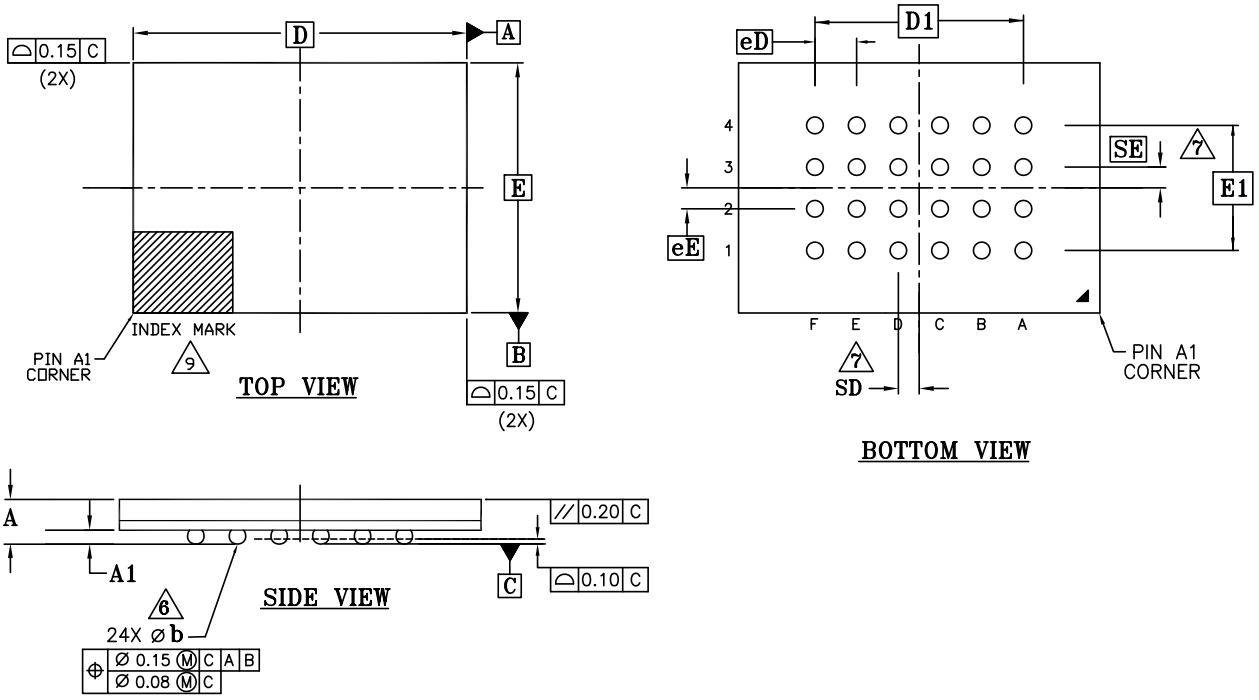
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
∅ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15534 Rev. **

Figure 28. FAC024 24-ball Ball Grid Array (6 x 8 mm) Package



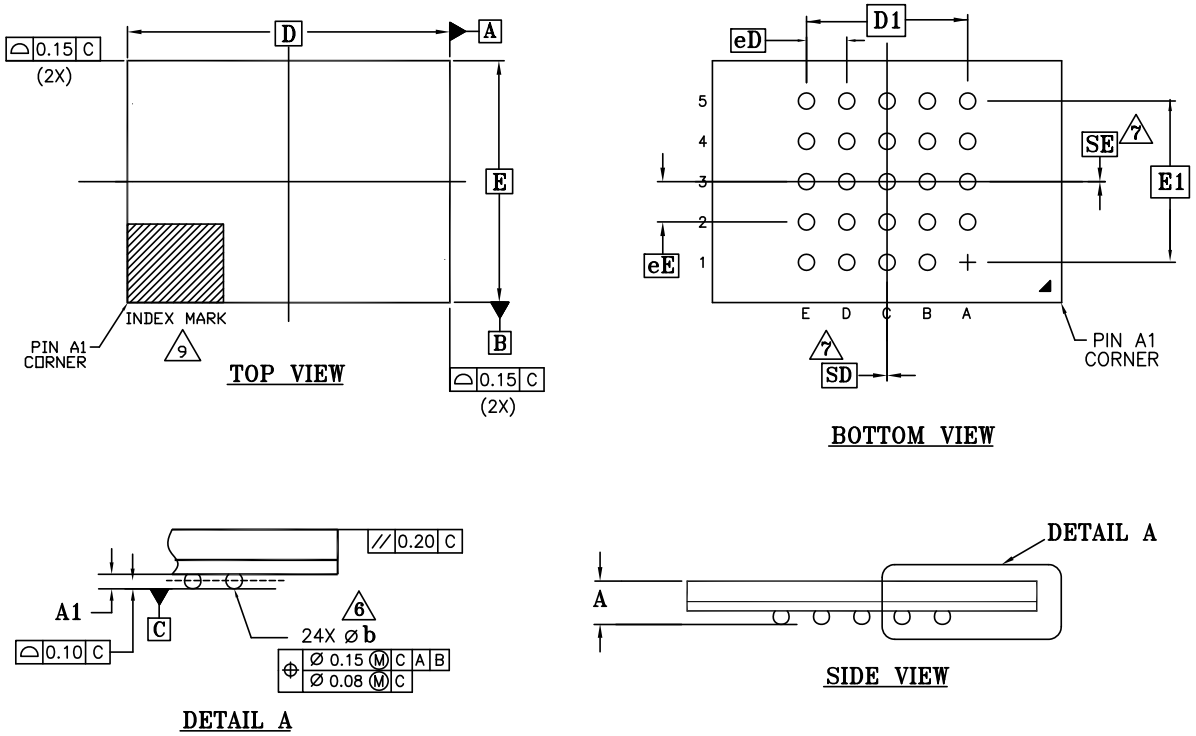
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		5.00 BSC	
E1		3.00 BSC	
MD		6	
ME		4	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.50 BSC	
SE		0.50 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15535 Rev. **

Figure 29. ZSA024 24-ball Ball Grid Array (6 x 8 mm) Packages



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	4.00 BSC		
E1	4.00 BSC		
MD	5		
ME	5		
n	24		
Ø b	0.35	0.40	0.45
eD	1.00 BSC		
eE	1.00 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15078 Rev. **

4 Land Patterns Recommendations

Applicable PCB land pattern recommendations for SOC 008, SO3 016, SL3 016, USON, WSON, FAB024, FAC024, and ZSA024 packages are provided here in Figure 31 through Figure 35.

Note: All dimensions are in mm.

Figure 30. SOA008 Proposed Land Pattern

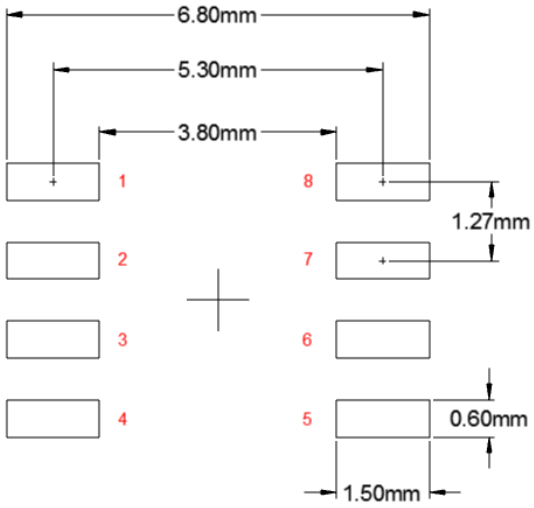


Figure 31. SOC008 Proposed Land Pattern

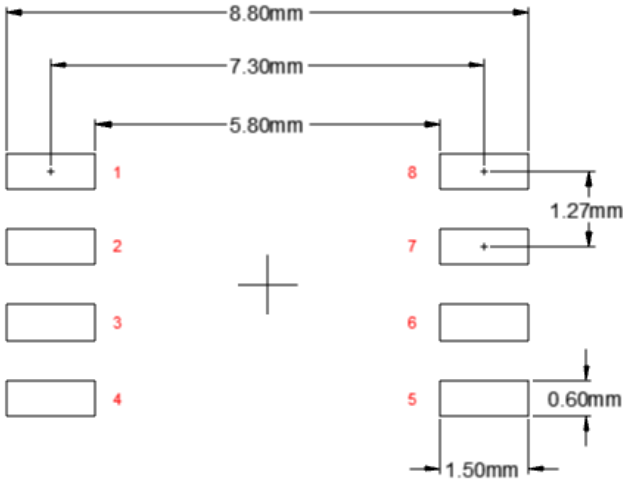


Figure 32. SO3 016 and SL3 016 Proposed Land Pattern

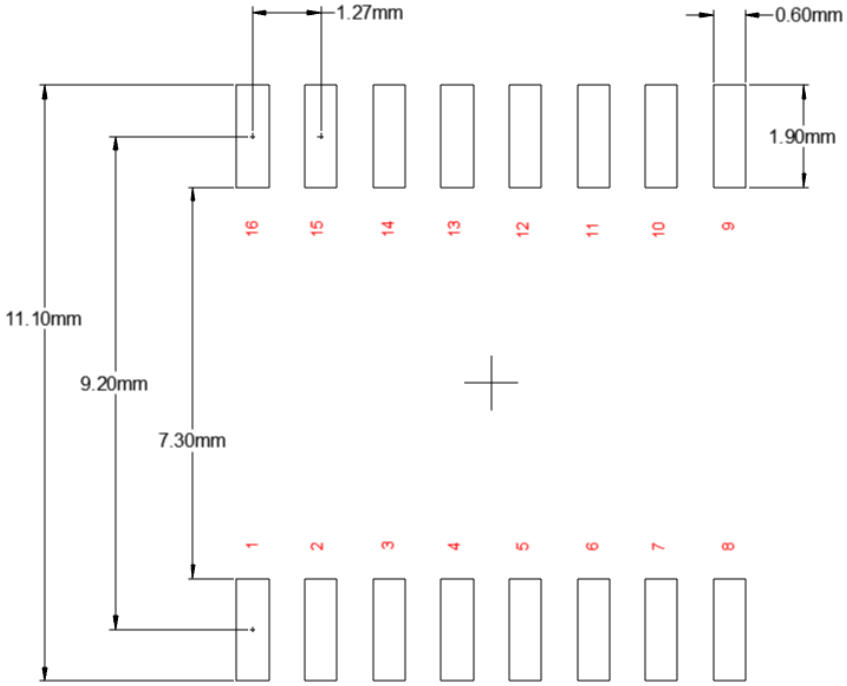
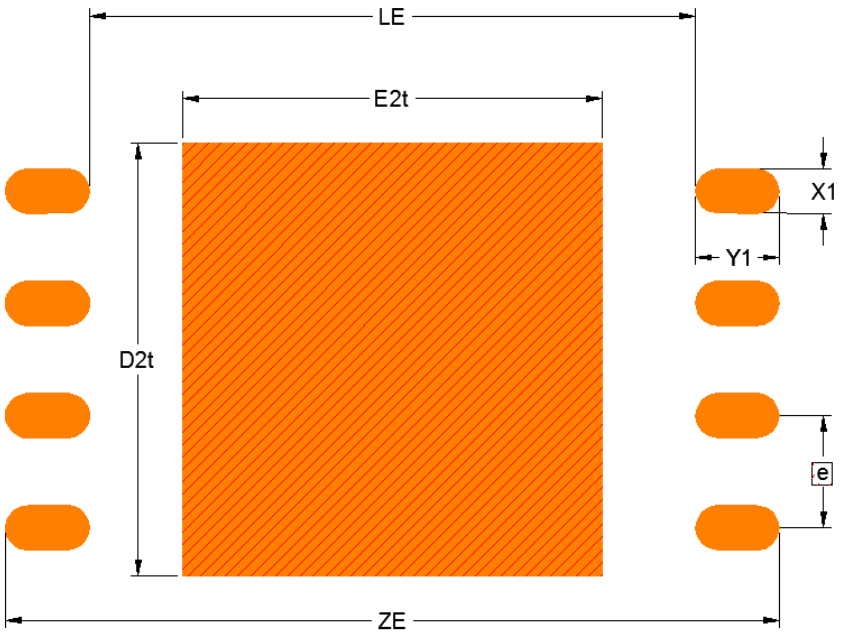


Figure 33. USON 8L and WSON 8L Proposed Land Pattern



Package	Package Code	Lead Pitch e	PCB Land Pattern Recommendation					
			LE (min)	ZE (max)	D2t (max)	E2t (max)	Y1	X1
USON 8L	UNE008	1.27	4.65	6.75	4.10	3.50	1.05	0.45
WSON 8L	WND008	1.27	4.65	6.75	4.10	3.50	1.05	0.45
	WNF008	1.27	6.75	8.05	4.90	5.90	0.65	0.5
	WNG008	1.27	6.85	8.75	4.90	4.75	0.95	0.45
	WNH008	1.27	6.85	8.75	4.10	3.50	0.95	0.45

The USON 8L and WSON 8L land patterns are shown above. It is recommended that the center slug should be solder mask define (SMD) to avoid bridging. The mask opening should be 0.05 – 0.1 mm smaller than the center pad on all four sides. At the pin, it should be NSMD with the mask opening 3 mil larger than the copper pad on all sides. At center slug, the stencil should also has small multiple openings with solder paste coverage about 40 – 70% of the exposed pad area to prevent bridging between the center slug and pins.

Figure 34. FAB024 and ZSA024 Proposed Land Pattern

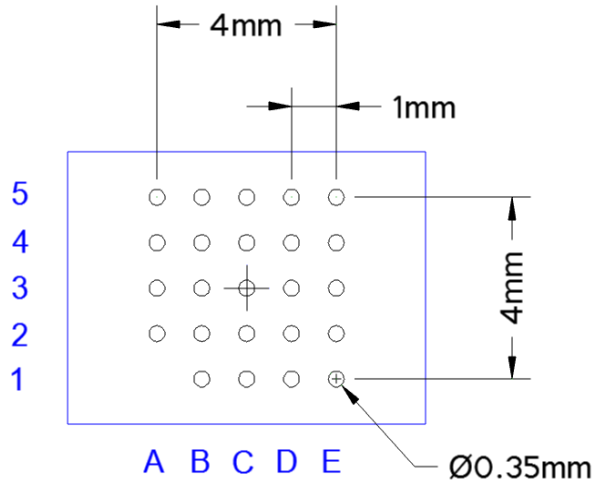
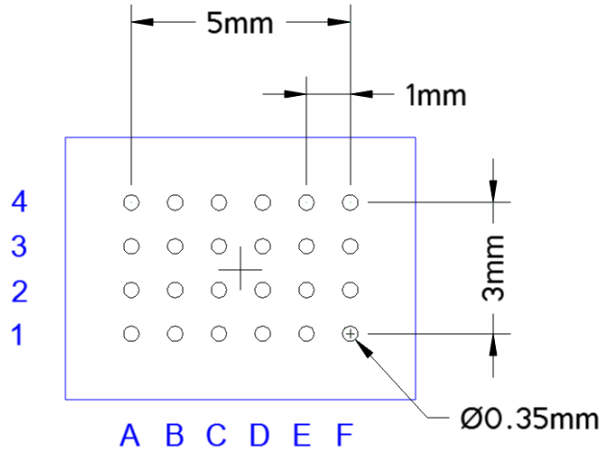


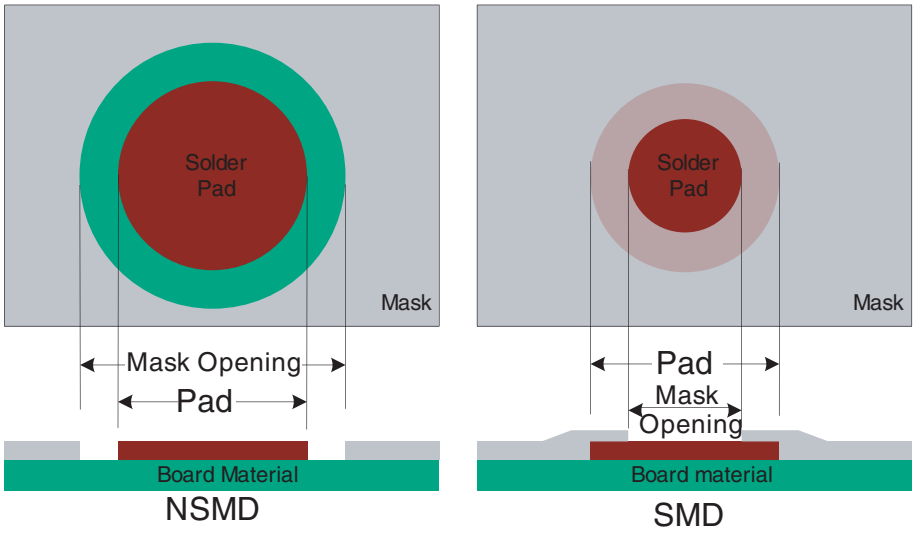
Figure 35. FAC024 Proposed Land Pattern



4.1 BGA Land Pad Recommendations

PCB solder-ball land pads can be either non-solder-mask defined (NSMD) or solder-mask-defined (SMD). For NSMD configurations, there is a small gap between the solder pad and the solder mask. Solder will flow into the gap between the pad and the solder mask (reference Figure 36). For SMD configurations, the solder mask covers the outer edge of the solder pad. Solder is prevented from flowing over the edges of the pad by the solder mask.

Figure 36. SMD vs. NSMD Landing Pad Definition



NSMD is generally the recommended land pad configuration because it enables a stronger bond between the solder pad and the solder ball with less stress concentration.

For SMD configurations, it is good practice to make the solder mask opening the same size as the diameter of the solder ball. On NSMD configurations, the solder pad should be between 80% and 100% of the solder ball diameter and the solder mask opening should be 0.15 mm larger than the solder pad to provide ample space for excess solder. Table 2 provides dimensional recommendations for SMD and NSMD configurations suitable for use with the FAB024, FAC024 and ZSC024 packages.

Table 2. NSMD and SMD Dimensional Recommendations for BGA Packages

Configuration	Opening	Recommended Dimension
SMD	Solder Pad	0.55 mm
	Solder Mask	0.45 mm
NSMD	Solder Pad	0.45 mm
	Solder Mask	0.60 mm

5 Printed Circuit Board Design Recommendations

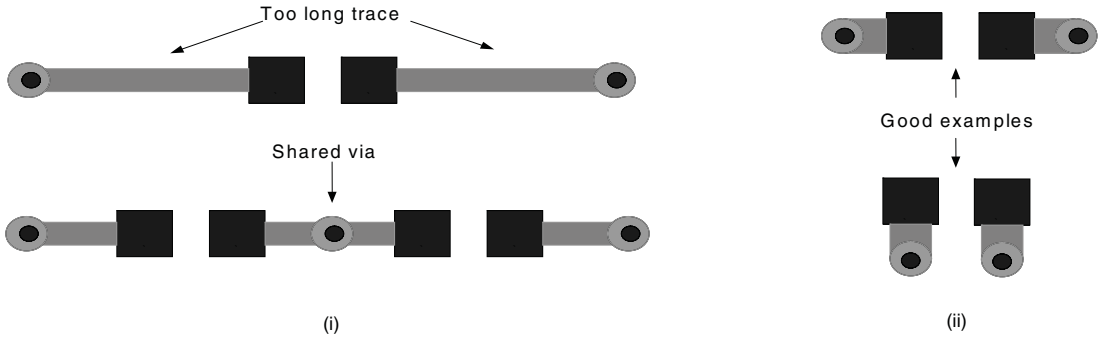
This section contains general layout recommendations.

5.1 Power Supply Decoupling

All S25FL and S70FL SPI Flash have one power supply input pin (V_{CC}) and one ground pin (GND). Additionally, certain models support a separate I/O supply input pin (V_{IO}) for applications that require I/O levels to be less than V_{CC}. Use of one 0.1 µF ceramic capacitor, normally in a 0603 or 0402 package, is recommended for decoupling each power supply input pin. A decoupling capacitor should be placed as close as possible to the V_{CC} supply input pin, as well as the V_{IO} supply input pin if present.

The routing of the decoupling capacitor should be optimized to achieve low inductance. Power supply trace lengths from the package pads to the vias should be as short as possible with a trace width of approximately 0.6 mm. It is recommended to avoid sharing the same via with 2 or more decoupling capacitors. Figure 37 shows examples of routing the decoupling capacitor.

Figure 37. Routing with Decoupling Capacitor



5.2 Clock Signal Routing

For reliable high speed synchronous data transfers, it is essential for the clock signal to have very good signal integrity. The following recommendations should be taken into consideration when routing the clock signal.

- Run the clock signal at least 3x of the trace width away from all other signal traces. This will help keep clock signal clean from noise, reference Figure 38.
- Use as few vias as possible for the entire path of the clock signal. Each via will create impedance changes and signal reflections.
- Run the clock trace as straight as possible and avoid using serpentine routing, reference Figure 39.
- Keep a continuous ground in the next layer as a reference plane.
- Route the clock trace with controlled impedance, typically a 50 ohm trace impedance with ± 5% tolerance.

Figure 38. Separate Clock from other Traces

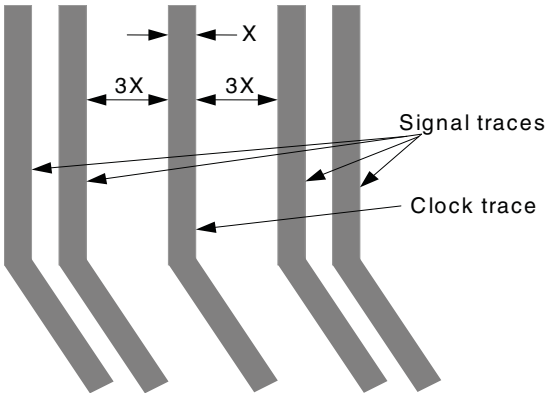
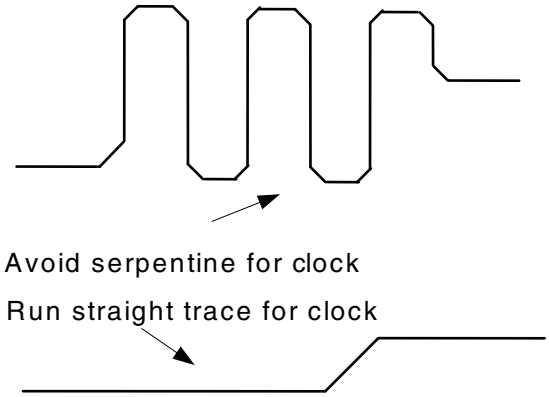


Figure 39. Straight Trace Runs for Clock

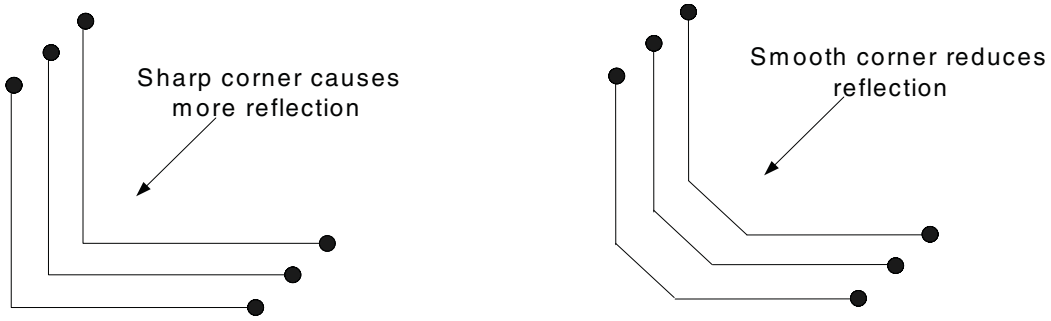


5.3 Data Signal Routing

The FL Flash support 1, 2 and 4-bit data bus configurations. In 2 and 4-bit multiple I/O configurations, it is important that the I/O traces are routed such that they have identical lengths, within ~ 3 mm, to assure equivalent propagation delays. To assure reliable data transfers for all configurations it is important that the propagation delays for the clock trace and all data traces are identical.

The data signals should be routed with traces of controlled impedance to reduce signal reflection. Data traces should have no 90° angle corners. The preferred method for implementing a 90° angle change is to cut the corner to smooth the trace, reference Figure 40. To maximize signal integrity, avoid using multiple signal layers for data signal routing and ensure all signal traces have a continuous reference plane.

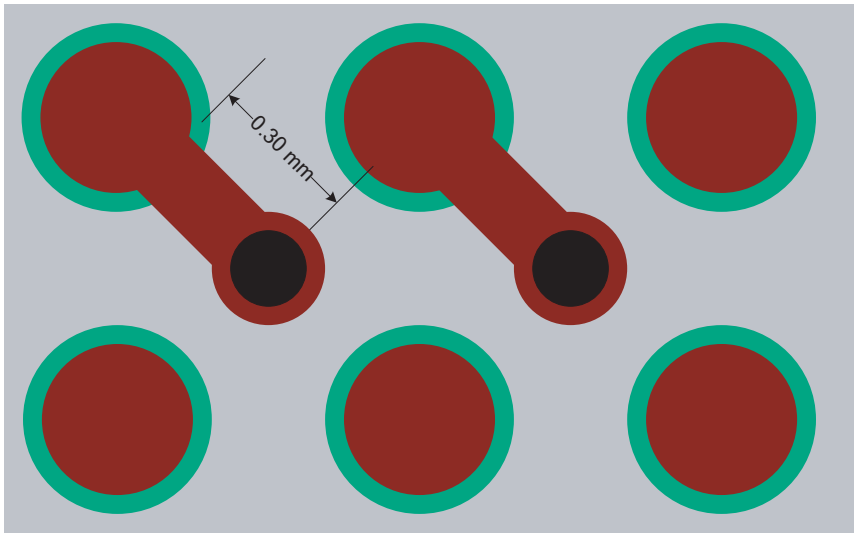
Figure 40. Signal Routing at the Corner



5.4 Via Routing

Vias should not be placed within a land pad as this can cause solder wicking inside the via hole, resulting in misshapen solder joints and electrical opens. Vias should be placed a minimum of 0.3 mm away from the solder pad as shown in Figure 41.

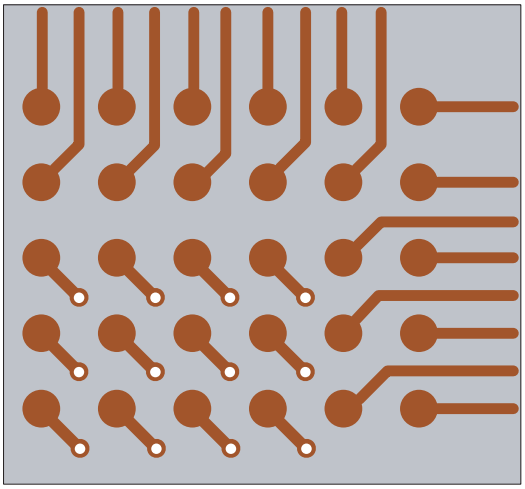
Figure 41. Recommended via Placement



5.5 Escape Path Routing

Maintaining good signal integrity must be a top priority when considering BGA escape path routing. Only one signal trace should be routed between any two adjacent land pads, reference Figure 42.

Figure 42. Escape Path Routing (example: FAB024)



6 Summary

The Cypress S25FL/S25FS serial peripheral flash devices utilize industry standard packages. PCB layout for Cypress SPI flash requires use of standard high speed board layout principals.

Document History Page

Document Title: AN98508 - Cypress Serial Peripheral Interface (SPI) FL Flash Layout Guide Document Number: 001-98508				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	07/02/2010	Initial version
*A	–	–	04/08/2011	SPI Flash Package Drawings: Updated figure: SO3 016 – 16-Pin Wide Plastic Small Outline Package (300 mil Body Width) Land Patterns Recommendations: Updated E2 dimension for WSON-8 package
*B	5050808	MSWI	12/1152015	Updated in Cypress template
*C	5725433	AESATMP9	06/13/2017	Updated logo and copyright.
*D	6130593	BWHA	04/19/2018	Updated diagrams Figure 18 through Figure 29 Updated template

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