AN98507

Connecting Cypress SPI Serial Flash to Configure Xilinx FPGAs

Author: Kuwano, Takahiro

Associated Part Family: Serial NOR Flash Memory

AN98507 describes compatibility information between Cypress SPI flash and Xilinx FPGAs, SPI flash basics, and considerations required in some cases.

1 Introduction

Xilinx FPGAs are programmable logic devices used for basic logic functions, chip-to-chip connectivity, signal processing, and embedded processing. These devices are programmed and configured using an array of SRAM cells that need to be re-programmed on every power-up. Several different methods of configuring FPGAs are normally used. They include programming by a microprocessor, JTAG port, or directly by a serial PROM or flash. Cypress' Serial Peripheral Interface (SPI) flash can be easily connected to Xilinx FPGAs to configure the FPGA at power up. The readers of this application note are expected to understand the basics of Xilinx FPGA configuration using SPI flash, by reading user guides and application notes from Xilinx listed in Related Documents. This document intends to be a supplement for the Xilinx documents by covering specific topics for Cypress SPI flash.

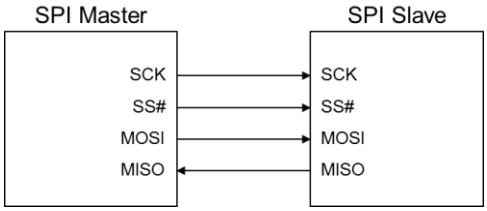
2 SPI Basics

Serial Peripheral Interface (SPI) is a simple 4-wire synchronous interface protocol that enables a master device and one or more slave devices to communicate. The SPI bus consists of four signal wires:

- Master Out Slave In (MOSI) signal generated by the master (data to slave)
- Master In Slave Out (MISO) signal generated by the slave (data to master)
- Serial Clock (SCK) signal generated by the master to synchronize data transfers
- Slave Select (SS#) signal generated by master to select individual slave devices, also known as Chip Select (CS#) or Chip Enable (CE#)

Figure 1 shows the connection between a SPI Master and a SPI Slave.

Figure 1. SPI Master and SPI Slave Connection



In addition to the basic x1 data width mode above, Cypress SPI flash and the Xilinx FPGAs support x2 and x4 data width mode. In the x2 data width mode, the MOSI signal becomes bidirectional. In the x4 data width mode the additional two pins are used for data transfer. Furthermore, the Xilinx UltraScale and UltraScale+ FPGAs supports the Dual x4 mode, which (=x8) uses two SPI flash devices in parallel.

3 SPI Flash Connections to FPGAs

Figure 2 and Figure 3 show the FPGA-to-SPI-Flash connection in x4 and Dual x4 data width mode. The pin names and functions are explained in Table 1.

Figure 2. FPGA and SPI Flash Connection in x4 Data Width Mode

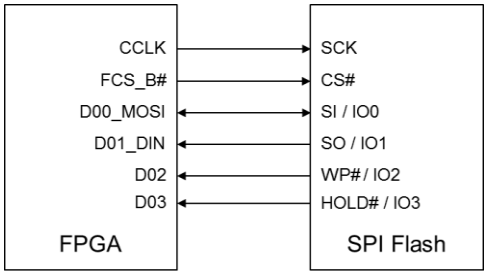


Figure 3. FPGA and SPI Flash Connection in Dual x4 Data Width Mode

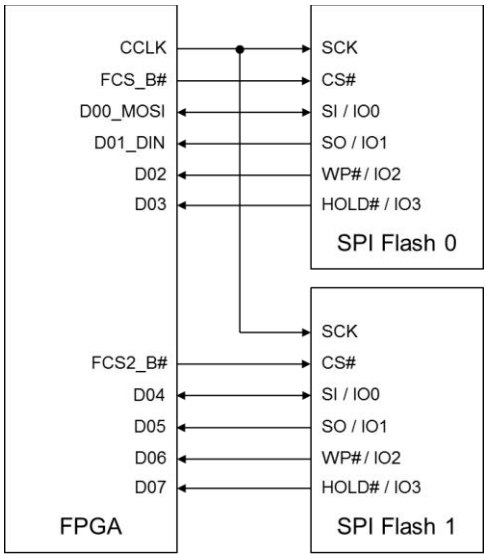


Table 1. FPGA and SPI Flash Pins

FPGA Pin Name	SPI Flash Pin Name	Description
CCLK	SCK	Serial Clock
FCS_B# FCS2_B#	CS#	Chip Select
D00_MODI D04	SI / IO0	Serial Input in x1 mode IO0 in x2 and x4 mode
D01_DIN D05	SO / IO1	Serial Output in x1 mode IO1 in x2 and x4 mode
D02 D06	WP# / IO2	Write Protect in x1 and x2 mode IO2 in x4 mode
D03 D07	HOLD# / IO3	Hold (pause) serial transfer in x1 and x2 mode IO3 in x4 mode

During FPGA configuration process, the FPGA reads the configuration bitstream from SPI flash by issuing read commands. There are some variations of read command depending on the data width and addressing. Table 2 shows the read commands used by the Xilinx FPGAs. Cypress S25FL-L and S25FL-S 3.0V SPI flash families (listed in Table 3) support all commands. The Cypress S25FS-S 1.8V SPI flash family does not support DOR(3Bh), 4DOR(3Ch), QOR(6Bh), and 4QOR(6Ch).

Table 2. Read Commands Used for FPGA Configuration

SPI Command Name (in Xilinx Documents)	SPI Command Name (in Cypress Datasheets)	Opcode
Fast read	FAST_READ	0Bh
Fast read, 32-bit address	4FAST_READ	0Ch
Dual output fast read	DOR	3Bh
Dual output fast read, 32-bit address	4DOR	3Ch
Quad output fast read	QOR	6Bh
Quad output fast read, 32-bit address	4QOR	6Ch

4 Considerations for Selecting Cypress SPI Flash

4.1 Supported Cypress SPI Flash for Xilinx FPGAs

Table 3 shows the supported Cypress SPI flash for Xilinx FPGA families. The table is based on supported devices listed in the Vivado Design Suite User Guide: Programming and Debugging (UG908) and ISE Help, excluding the SPI flash families not recommended for new designs (i.e., S25FL1-K and S25FL-P). The following sections describes the considerations for selecting one of Cypress SPI flash.

Table 3. Supported Cypress SPI Flash for Xilinx FPGAs

Xilinx FPGAs			Cypress SPI Flash				
FPGA Family	IO Voltages	SPI Modes	S25FL064L[1]	S25FL128L[1] S25FL256L[1]	S25FL127S[1] S25FL128S	S25FL256S S25FL512S	S70FL01GS
Artix-7	3.3V, 2.5V, 1.8V, 1.5V	x1, x2, x4	✓	✓	✓	✓	
Kintex-7	3.3V, 2.5V, 1.8V, 1.5V	x1, x2, x4	✓	✓	✓	✓	
Spartan-7	3.3V, 2.5V, 1.8V, 1.5V	x1, x2, x4	✓	✓	✓	✓	
Virtex-7	1.8V, 1.5V	x1, x2, x4			✓	✓	
Kintex UltraScale	3.3V, 2.5V, 1.8V, 1.5V	x1, x2, x4, x8	✓	✓	✓	✓	
Kintex UltraScale+	1.8V, 1.5V	x1, x2, x4, x8	✓	✓	✓	✓	
Virtex UltraScale	3.3V, 2.5V, 1.8V, 1.5V	x1, x2, x4, x8	✓	✓	✓	✓	
Virtex UltraScale+	1.8V, 1.5V	x1, x2, x4, x8	✓	✓	✓	✓	
Zynq-7000	3.3V, 1.8V	x1, x2, x4, x8	✓		✓	✓	✓
Zynq UltraScale+ MPSoC	3.3V, 1.8V	x1, x2, x4, x8			✓	✓	✓
Zynq UltraScale+ RFSoC	3.3V, 1.8V	x1, x2, x4, x8			✓	✓	✓
Spartan-6	3.3V	x1, x2, x4	✓[2]	✓[2]	✓[2]		

Note: 1. S25FL064L, S25FL128L, and S25FL127S do not have the V_{IO} option. A level shifter is needed if the I/O voltage of the FPGA is not 3.3 V.

Note: 2. S25FLxxP is listed in the table at Xilinx ISE Help; however, the S25FLxxP is not recommended for new designs. S25FL-L and S25FL-S families are compatible with the S25FL-P family and known to work. See KBA219147 and AN98577 for details.

4.2 I/O Voltage of Configuration Interface

The I/O voltage compatibility needs to be considered to select Cypress SPI flash for Xilinx FPGA configuration. As shown in Table 3, some of Xilinx FPGA families support only 1.8 V or 1.5 V for the configuration I/O voltage. All SPI flash families listed in Table 3 require 3.3 V for the core voltage (V_{CC}). For some Cypress SPI flash families, there is an ordering option that can accept 1.8 V at the I/O voltage (V_{IO}) pin, which is separated from the core voltage (V_{CC}). S25FL128S, S25FL256S, S25FL152S, and S70FL01GS have the V_{IO} option. Note that the SPI flash with the V_{IO} option requires a higher t_V (Clock Low to Output Valid) value that impacts the configuration performance (see Table 4). If the application requires higher configuration speed, it is recommended to use a part without the V_{IO} option, and with a level shifter. Cypress offers the S25FS-S SPI flash family which operates at 1.8-V core voltage (V_{CC}); however, the S25FS-S family does not support read commands used for x2 and x4 data width mode.

4.3 Quad Output Read Support

In the master SPI configuration mode, Xilinx FPGAs can read from the SPI flash with x4 data width. It is called Quad Output Read in Cypress SPI flash. All Cypress SPI flash families listed in Table 3 support Quad Output Read; however, the option is not enabled by default. To enable it, the Quad Enable Bit in the Flash internal configuration register must be set (see Cypress SPI flash datasheets for details).

Xilinx's in-system Flash programming tools (Vivado or iMPACT) set the Quad Enable Bit when programming the FPGA configuration bitstream to Cypress SPI flash. If third-party Flash programmers are used for programming the FPGA configuration bitstream to the SPI flash before mounting it to PCB, the programmers must set the Quad Enable Bit.

4.4 Maximum Configuration Clock Frequency

XAPP586 and XAPP1233 use Equation 1 to determine the maximum configuration clock frequency and provide calculation examples.

$$F_{CCLK,MAX} \leq \frac{1}{(T_{SPITCO} + T_{SPIDCC} + T_{TPD})} \quad \text{Equation 1}$$

In the calculation, a timing parameter, T_{SPITCO} is defined as the flash clock to out or SPI clock Low to Output Valid, which is represented by a symbol, t_V (Clock Low to Output Valid) in Cypress SPI flash datasheets. Table 4 shows the maximum t_V values of Cypress SPI flash families in several conditions. A lower t_V value results in a higher clock frequency. The other two parameters, T_{SPIDCC} and T_{TPD}, rely on the FPGA and PCB characteristics. Note that the t_V value increases if the SPI flash has the V_{IO} option and the V_{IO} range is lower than V_{CC}.

Table 4. Maximum t_V (Clock Low to Output Valid)

Symbol	Conditions			S25FL064L S25FL128L	S25FL127S	S25FL128S S25FL256S S25FL512S
	V_{CC} Range	V_{IO} Range	CL			
t_V	2.7 – 3.6 V	= V_{CC}	30 pF	8.00 ns	8.00 ns	8.00 ns
	2.7 – 3.6 V	= V_{CC}	15 pF	6.00 ns	-	-
	3.0 – 3.6 V	= V_{CC}	30 pF	-	7.65 ns	7.65 ns
	3.0 – 3.6 V	= V_{CC}	15 pF	-	6.50 ns	6.50 ns
	2.7 – 3.6 V	1.65 – 2.7 V	30 pF	-	-	14.5 ns
	2.7 – 3.6 V	1.65 – 2.7 V	15 pF	-	-	12.0 ns

The $F_{CCLK.MAX}$ value when T_{SPITCO} = 6.0 ns (S25FL064L with 15-pF load), T_{SPIDCC} = 3.0 ns, and T_{TPD} = 2.0 ns is 90.9 MHz, for example. This value is within the maximum clock frequency (104 MHz) for read operation in S25FL064L.

4.5 Power-On Sequence Precautions

At power on, the FPGA automatically starts its configuration procedure by reading the configuration Bitstream from the SPI flash; therefore, the SPI flash used for FPGA configuration must be ready to respond to the read command. The time between power ramp to configuration start is defined as T_{POR} in Xilinx FPGA datasheets, which is 10 ms (7 series FPGA) and 5 ms (UltraScale FPGA) at minimum. In Cypress SPI flash, a timing parameter t_{PU} is defined as shown in Table 5 and Figure 4. Because t_{PU} is an order of magnitude less than T_{POR}, the SPI flash becomes ready before the FPGA issues the read command if the same power rail supplies both FPGA and SPI flash. If not, a countermeasure may be needed. In addition, if the selected Cypress SPI flash has the RESET# signal and RESET# remains LOW at t_{PU} end, you must ensure that CS# remain HIGH for a period of t_{RH} after RESET# returns HIGH (Figure 5)

Table 5. Power On Timing

Symbol	Conditions	S25FLxxxL	S25FLxxxS
$V_{CC(min)}$	Minimum operation voltage	2.7 V	2.7 V
t_{PU}	$V_{CC(min)}$ to Full Device Access	300 µs	300 µs
t_{RH}	Reset Hold (RESET# HIGH to CS# LOW)	150 ns	50 ns

Figure 4. t_{PU} – $V_{CC(min)}$ to Full Device Access

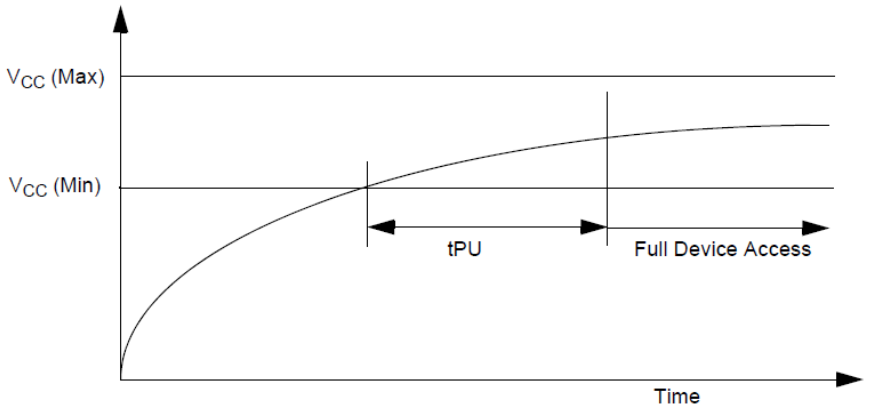
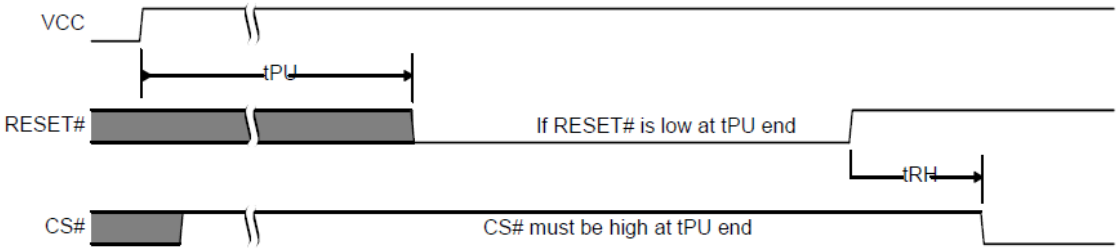


Figure 5. t_{RH} – Reset Hold (RESET# high to CS# low)



5 Related Documents

Cypress Datasheets
S25FL064L, 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory Datasheet
S25FL256L/S25FL128L, 256-MB (32-MB)/128-MB (16-MB), 3.0 V Flash Memory Datasheet
S25FL127S, 128 Mbit (16 Mbyte) 3.0V SPI Flash Memory Datasheet
S25FL128S/S25FL256S, 128 Mbit (16 Mbyte)/256 Mbit (32 Mbyte) 3.0V SPI Flash Memory Datasheet
S25FL512S, 512 Mbit (64 Mbyte) 3.0V SPI Flash Memory Datasheet
S70FL01GS, 1 Gbit (128 Mbyte) 3.0V SPI Flash Memory Datasheet
Cypress Application Notes
AN98577 – Migration from FL-P to FL-S Family SPI Interface Flash Memories
AN217010 – Migrating from S25FL1-K Serial NOR Flash to S25FL064L Serial NOR Flash
Cypress Knowledge Base Articles
Using Cypress S25FL-L SPI Flash with Xilinx Spartan-6 FPGA - KBA219147
Xilinx User Guides / Application Notes
7 Series FPGAs Configuration User Guide (UG470)
UltraScale Architecture Configuration User Guide (UG570)
Vivado Design Suite User Guide: Programming and Debugging (UG908)
Using SPI Flash with 7 Series FPGAs Application Note (XAPP586)
SPI Configuration and Flash Programming in UltraScale FPGAs Application Note (XAPP1233)

Document History

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Revision	ECN	Submission Date	Description of Change
**	–	10/25/2007	New Application Note.
*A	–	03/03/2008	Updated Figures 3.1 and 3.2 Added section 4.3
*B	–	03/31/2011	Introduction: Added Spartan-6, Virtex-6 Updated section SPI Flash Connections to FPGAs: Added DOUT to table: Pin Descriptions for FPGA Configuration from SPI Flash Updated table: SPI Flash Selection for Spartan Family FPGA Devices Updated table: SPI Flash Selection for Virtex-5 Family FPGA Devices Added table: SPI Flash Selection for Spartan-6 Family FPGA Devices Added table: SPI Flash Selection for Virtex-6 Family FPGA Devices Added figure: Spartan-6 serial (x1, x2, x4) Configuration from Cypress S25FL-P and S25FL-K SPI Quad I/O Serial Flash Connection Diagram Direct Programming SPI Flash: Updated section Using Cypress S25FL 3V SPI Flash with Virtex-6: Added section References: Added references
*C	4909568	09/05/2015	Added Table 1, Table 2, Table 3 Updated Table 1 Replaced detailed descriptions of Xilinx products with links to relevant Xilinx application notes Updated 4 Applying Voltages at Power-On Updated Figure 4 Removed sections Direct Programming SPI Flash and Fastest Configuration Time Updated links in 5 References Updated in Cypress template
*D	5790701	07/05/2017	Updated logo and copyright.
*E	6158274	04/27/2018	Updated the content to align the latest Flash/FPGA. Updated template
*F	6891182	06/02/2020	Updated Table 3 Updated links in Related Documents

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