AN98503

Signal Integrity and Reliable Flash Operations

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Associated Part Family: Parallel NOR Flash

AN98503 discusses the design considerations for signal integrity (SI) and power delivery network (PDN) that affect the robustness and performance of a system.

1 Introduction

Today's embedded systems continue to push many boundaries, operating at higher speeds and lower voltages. Advanced architecture Flash devices support higher speed XIP operations and operating voltages, while offering higher performance.

In the realm of high-speed digital design, there are many system-level factors that can significantly impact Flash performance. Two such factors are Signal Integrity (SI) and the Power Delivery Network (PDN). SI relates to how the design of the overall packaging affects general signal characteristics and propagation while PDN relates to how well power can be delivered to the Flash IC.

The goal of this document is to highlight how SI and PDN design trade-offs can affect the robustness of a system, which in turn can directly impact the performance of an embedded Flash operation.

Note that SI and PDN are very complex issues, and thus, it is not the intent of this document to discuss these topics at length or in great detail. The reader may access the references noted in this document as well as other sources which may provide more in depth discussion and analysis on these subjects.

2 Signal Integrity Overview

In today's high-speed digital designs, the smaller parasitic inductances and capacitances in the module and associated IC's reduce signal transition times. This can result in signal and V_{CC} noise which can degrade operational reliability. Although every design is different, problems often begin showing up in the range of nanoseconds and faster. Typically faster rise times are associated with higher operating frequencies. SI and PDN issues on boards have been typically associated with higher frequency signals on the board, but it is important to recognize that SI and PDN issues are not necessarily related to just operating frequencies — in many cases signal rise times are the real source of the problem. With the ever increasing rise times SI and PDN implementation have become significant factors that affect the level of reliability of an Embedded System and its associated ICs.

The following sections highlight a few SI and PDN principles and issues of interest; again it is noted that SI and PDN are complex subjects and there is substantial amount of in-depth materials the reader can find on these subjects.

2.1 What is Signal Integrity?

Signal Integrity describes how well the signal maintains its desired shape and how the signal effects the receiving device's ability to perform the desired operation.

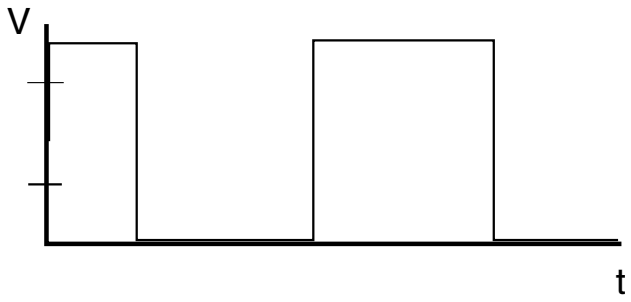
A signal looses its fidelity or integrity when the signal becomes distorted or when the signal-to-noise ratio (S/N) degrades. Signal distortion means that the waveform begins to change shape and S/N degrades as the signal or ground noise increases. The degree that this can happen before it becomes a problem depends very much on the application.

Looking at an example using inductance shows how additional noise is generated via high speed signal switching. All signal traces have inductance and the voltage generated across an inductor can be approximated by $V = L*di/ t_{rise}$, where L is the trace inductance, di/t_{rise} is the change in the switching current over the rise time. V increases proportionally as t_{rise} decreases. The voltage across the trace inductance adds on the original signal

and is seen as noise. Thus, the noise coupled to the original signal gets worse as V increases. The S/N ratio gets worse and the related potential for system problems increases.

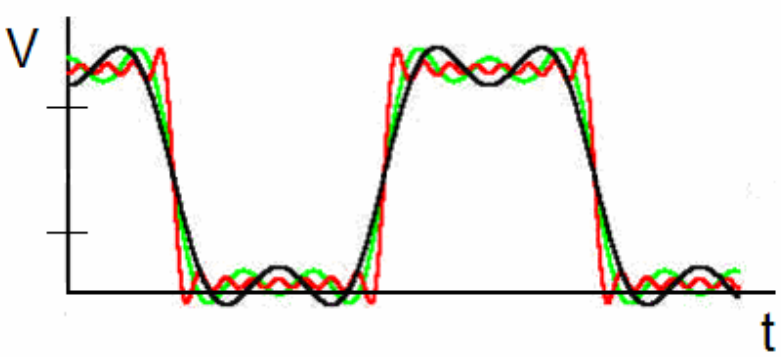
Digital signals are typically square waves or rectangular pulses and can be associated with one or multiple bits of information per clock cycle. Figure 1 shows an ideal square wave with no signal noise or distortion.

Figure 1. Ideal Square Wave



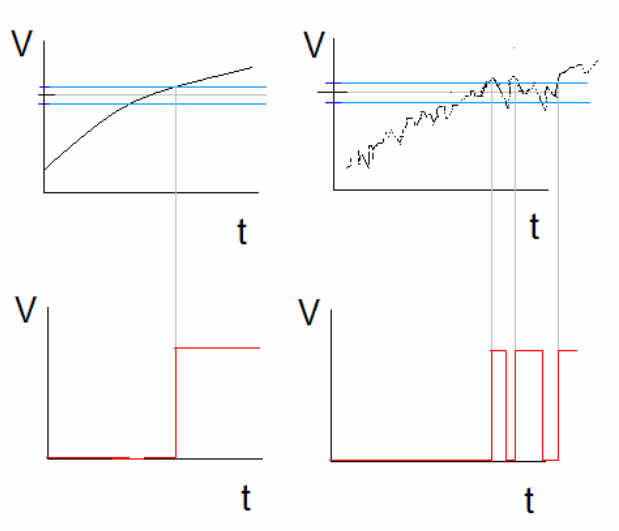
A nice thing about digital signals is, the system only needs to detect whether the voltage is in the “1” range or the “0” range. Depending on the system, a logic range can be fairly large and the signal can have a fair amount of distortion without obscuring the intended logic level or bit-state as shown in Figure 2. Note such signal overshoot may directly or indirectly couple to power and ground planes thus affecting the fidelity of a subject ICs power system.

Figure 2. Typical Square Wave with some Distortion



Analog signals are susceptible to distortion or noise from multiples sources. Figure 3 shows an example analog signal in real world applications where a comparator is used to convert analog signals to a digital CMOS level. The signal on the left is noise and distortion free resulting in a reliable conversion process where the signal on the right has both distortion and noise which induces errors during the conversion process.

Figure 3. Analog Signal: Left: Ideal Signal & Right: Noise Induced On the Signal



To some degree SI is affected by how the design of the electronic packaging affects signal propagation and characteristics. Signal lines are designed to behave very much like ideal transmission lines and under such conditions good signal fidelity is maintained and timing skews are minimized.

2.2 Power Delivery Network (PDN)

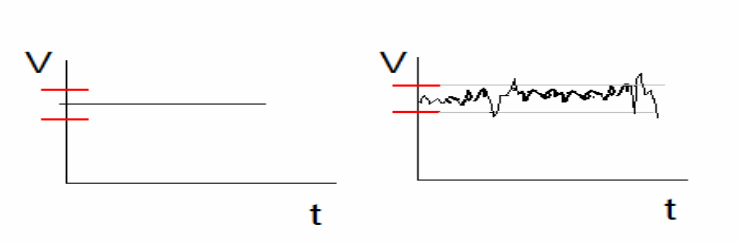
A well designed Power Delivery Network (PDN) ensures that the system V_{CC} and ground voltage fluctuations are within allowed margins. V_{CC}/Ground Noise is typically the result of circuits switching inside the semiconductor devices and at the device interface. Noise from the transitions are coupled to V_{CC} and ground by parasitic inductance.

The design of a noise-free PDN to supply a large amount of power at low voltages to microprocessor based systems operating with very fast slew rates, large dynamic loads and high clock frequency is a non-trivial task.

The earlier discussions referenced how inductance can be a critical parameter in noise generation during signal switching. The electrical performance of a power and ground system is sometimes characterized by its impedance across the switching current frequency spectrum. CMOS devices have faster signal slew rates that make the implementation of power and ground with sound fidelity a significant challenge. Power and ground impedance increases with faster edge rates. They can become significant where board and package level resonances are realized during design implementation. The faster the device's edge or slew rates the more difficult it is to maintain low impedance across the power and ground supply system.

Figure 4 shows two examples of V_{CC} supplying Flash ICs. The V_{CC} on the left is the ideal case where the voltage is stable and within the upper and lower limits over time. The V_{CC} on the right exhibits significant voltage fluctuation verses time and there are excursions where the voltage level is outside the desired limits. Power/ Ground Noise is created in many cases from the PDN parasitic impedances during drivers Simultaneous Switching Output (SSO).

Figure 4Illustration of V_{CC} Signals (Left: Ideal; Right: Noise on V_{CC})



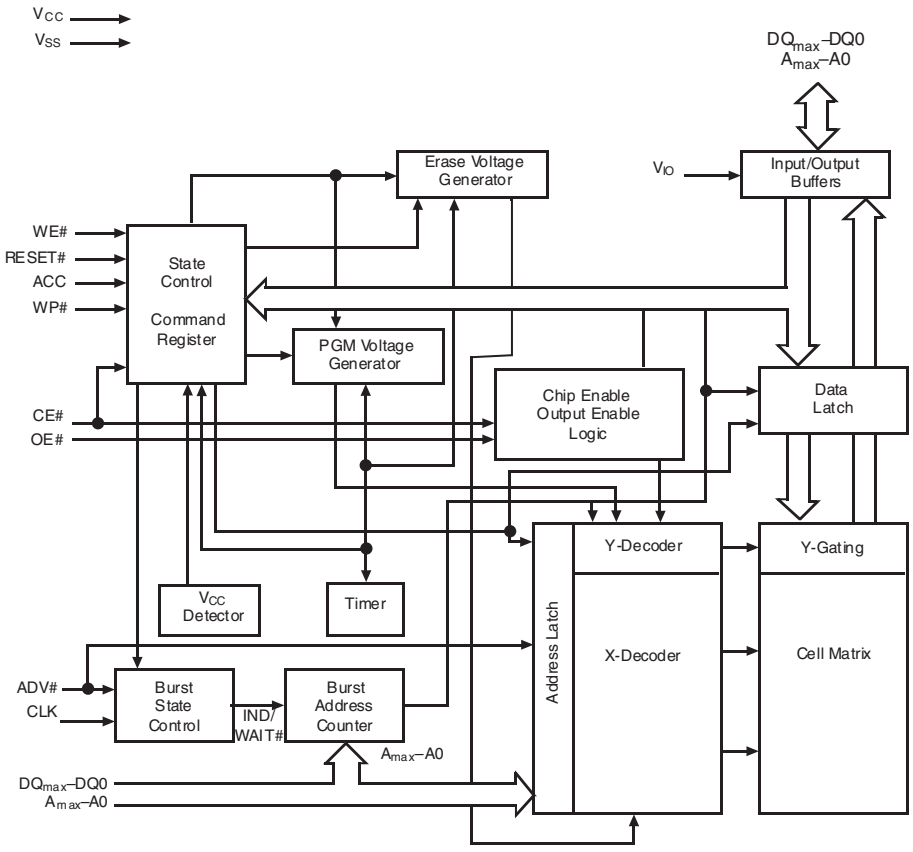
2.3 Flash Subsystem Overview

The following sections highlight some major Flash operational blocks and how the reliability of Flash operations can best be maintained by proper SI and PDN implementations.

2.3.1 Flash Block Diagram

In a typical embedded system, a microprocessor accesses a Flash device to perform three primary operations: Reading, Programming, and Erasing data in the Flash Cell matrix. The Flash Block diagram in Figure 5 shows the major components in a Flash device.

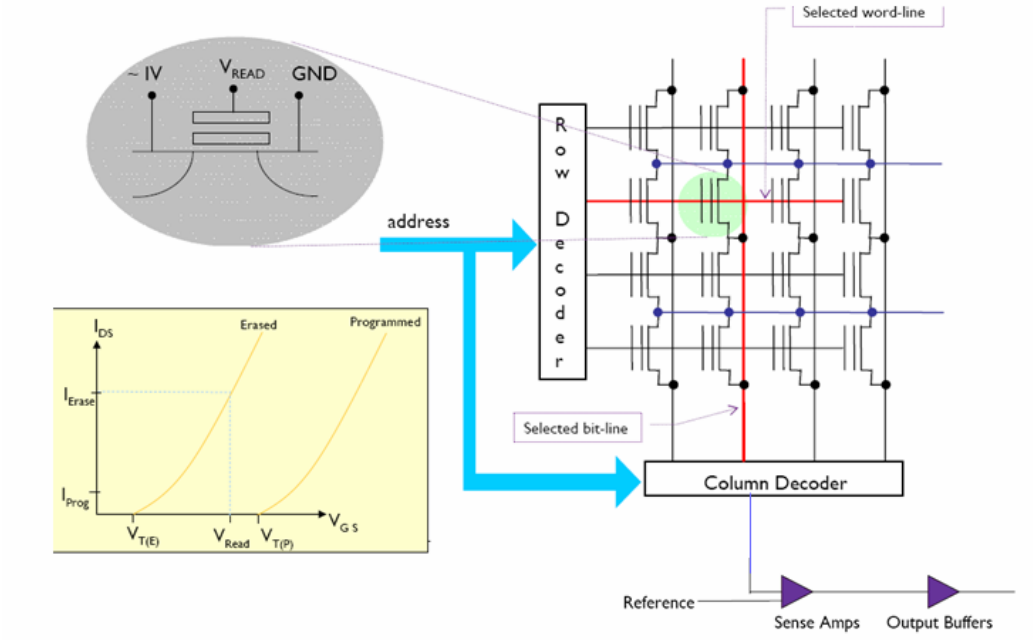
Figure 5. High Level NOR Flash Block Diagram



2.3.2 Flash Read Operation: Address Decode and Data Conversion

During a Flash Read operation Row and Column Decoding is used to select subject cells in the Flash array. The subject cell's IDS current will be an I_{Erase} or $I_{Program}$ based on the charge stored in the cell. The subject IDS current is output to Sense Amplifiers where it is converted from an analog signal to a digital signal and captured in the Output Buffers. The major Flash blocks used to complete this process is depicted in Figure 6 below:

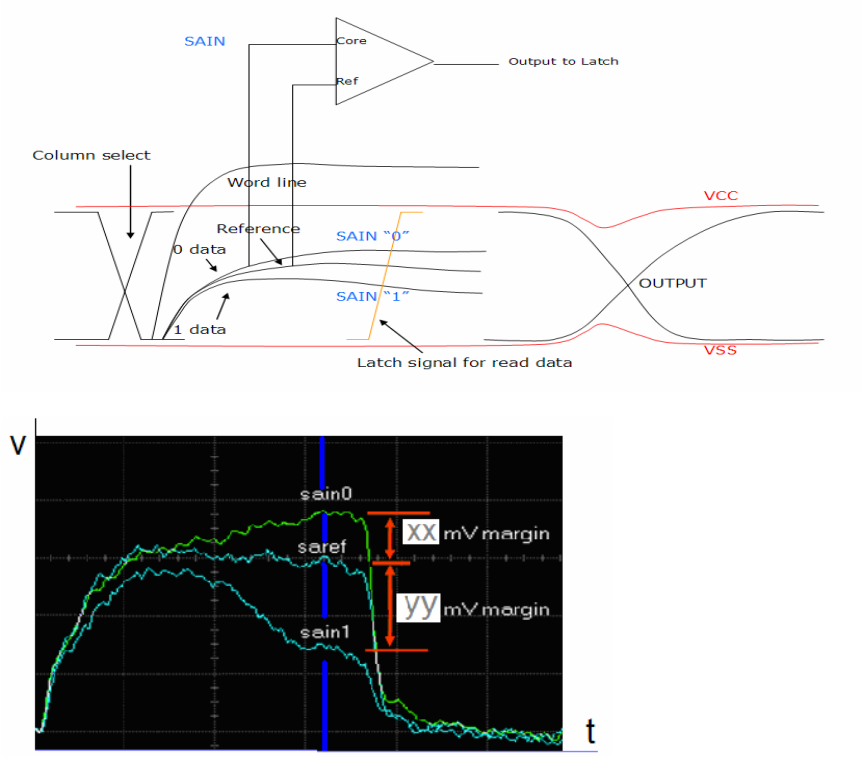
Figure 6. Flash Cell Array, Address Decode and Sense Amplifier



2.3.3 How Signal integrity and PDN Can Effect Flash Read Operation

Figure 7 shows additional details of the typical analog signals in the Sense Amplifier section where the signals are captured and converted to digital logic level. These subsections in Cypress Flash have been designed and characterized to operate reliably within the data sheet specifications.

Figure 7. Pre-Amplifier Signal and Reference



When a module design maintains a valid Flash V_{CC} while minimizing ground bounce, the analog signals and reference voltage(s) in the Pre-Amplifier section are operating in an environment that enables reliable read operation. Note these same signals and references are susceptible to signal distortion from V_{CC} noise, Simultaneous Switching Noise (SSN), and ground bounce. During a Read Operation, ground bounce couples noise to the Flash V_{CC} and reduces read margin. If the noise is large enough, it can result in a read error. Providing a proper design of a power and ground distribution system is a key factor to realize robust and reliable read operations.

The same SI and PDN criteria apply during Program and Erase operations. The Program and Erase operations will not be described in detail; note these operations also utilize the same subsections when verifying the subject cell charge level.

3 Conclusion: SI / PDN Trade-Offs Can Effect Critical Embedded Operations

Today's high-speed Embedded Systems are complex designs. Many times these designs realize signal rise and fall times that have decreased to where the parasitic impedances can result in signal/V_{CC} noise and ground bounce that becomes troublesome and can affect the design's reliable operation. As previously described, fast signal rise times can be the source of SI and PDN issues.

Section 2.3 differentiates how optimizing or the lack of optimizing SI and PDN can affect the reliability of a Flash Read, Program, or Erase operations. SI and PDN is one design aspect that should be part of the design planning and validation to ensure the power and ground voltage fluctuations are within an IC's V_{CC} margins.

Dennis Herrell a Co-Author of “Modeling of the Electrical Performance of the Power and Ground Supply for a PC Microprocessor on a Card” states:

> “There numerous PDN design trade-offs that can be made at various levels, including on-chip, on-package, on-card and onboard. The proper design of a power and ground distribution system includes issues such as the stack-up of power, ground, signal and dielectric layers, the placement of decoupling capacitors of right types at right locations, and the placement of vias connecting metal planes. Many of these design decisions

first come from previous design experiences and from insights on what physically happens inside an IC package, followed by what-if analyses and optimizations through software simulations, and by verifications through hardware measurements."

Johnson and Graham co-authors of High Speed Signal Propagation state that when lacking a good global 0V reference ground, a simple low pass filter can be employed to reduce the differential noise between V_{CC} and GND in the vicinity of the filter.

Cypress does recommend:

- A Flash V_{CC} is maintained within the Flash data sheet specification and ground bounce is minimized across all of the modules operating conditions.
- Minimization of overshoot of the Flash I/O.

4 References

1. "High Speed Signal Propagation Advanced Black Magic", Howard Johnson & Martin Graham, 2003
2. "Modeling of the Electrical Performance of the Power and Ground Supply for a PC Microprocessor on a Card", Jiayuan Fanga, Dennis Herrellb, Jin Zhaoa, Jingping Zhanga and Raymond Chenc
3. Cypress S29CD016J Data Sheet

Document History Page

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**	–	–	02/22/2008	Initial version
*A	4941311	MSWI	09/30/2015	Updated to Cypress template
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