S29VS064R/S29XS064R (64 Mb) PCB Routing Recommendation

AN98501 provides general routing guidelines for PCBs (printed circuit boards) designed with Cypress S29VS064R or S29XS064R products.

1 Introduction

This document provides general routing guidelines for PCBs (printed circuit boards) designed with Cypress S29VS064R or S29XS064R products.

This document does not eliminate the need for customer signal integrity/power delivery simulations and should be used as an initial reference towards PCB design with Cypress part. Cypress provided IBIS models should be used for signal timing/crosstalk simulations.

2 Signal Descriptions

The following table describes various pins and their function used in the S29VS064R and S29XS064R.

Table 1. Signal Descriptions

Signal	Description
A21-A16	Address Inputs (A21 is for 64 Mb only).
A/DQ15–A/DQ0	Multiplexed Address/Data input/output.
CE#	Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE#	Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE#	Write Enable Input.
V_{CC}	Device Power Supply (1.70V–1.95V).
V_{CCQ}	Input/Output Power Supply (1.70V–1.95V).
V_{SS}	Ground.
V_{SSQ}	Input/Output Ground.
NC	No Connect; not connected internally.
RDY	Ready output; indicates the status of the Burst read. V_{OL}= data invalid. V_{OH} = data valid.
CLK	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits Amax–A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
RESET#	Hardware reset input. V_{IL}= device resets and returns to reading array data.
V_{PP}	At 9V, accelerates programming. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

3 Package Breakout Routing Recommendations

Figure 1. S29VS/XS-64R — 44-Ball Very Thin FBGA Top View, Balls Facing Down

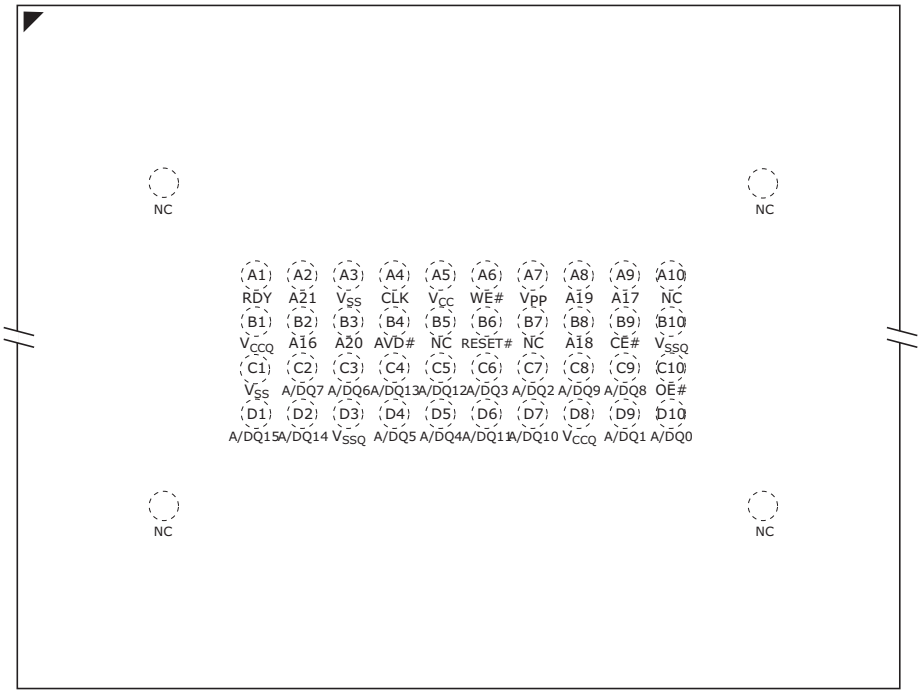


Figure 2. PCB Top Layer Escape Routing

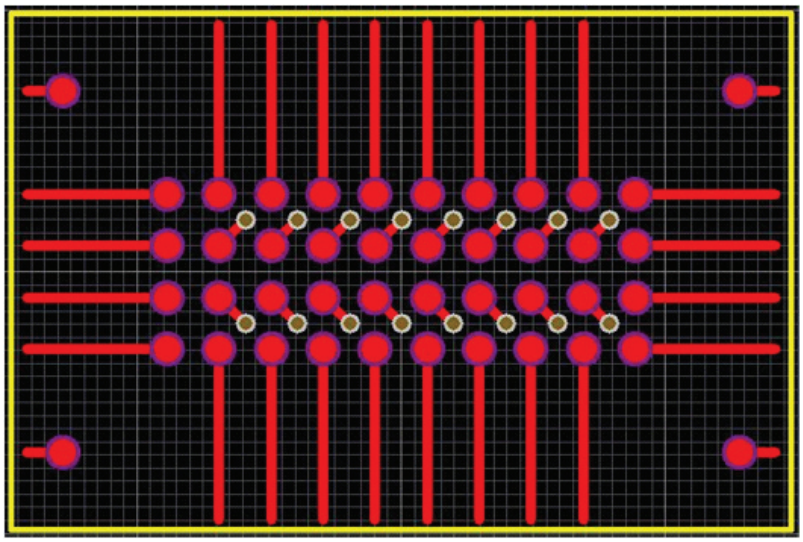
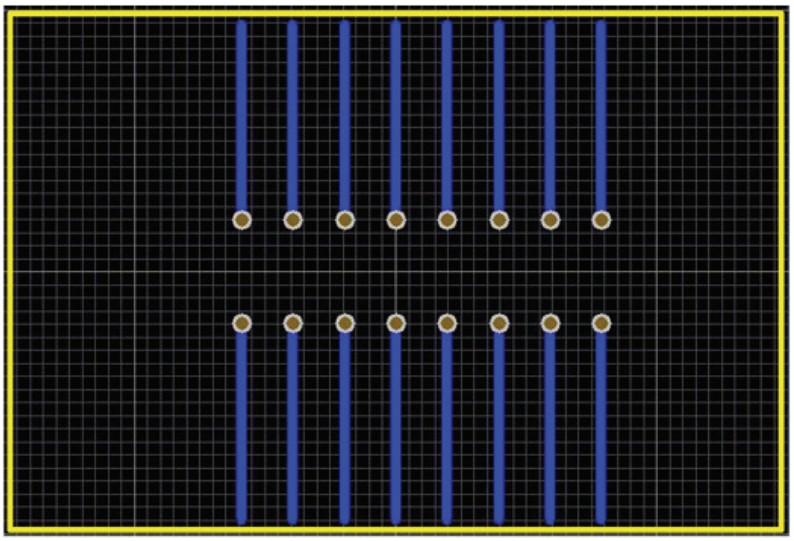


Figure 3. PCB Bottom Layer Escape Routing



For an example 2-layer escape routing shown in Figure 2 and Figure 3, you should use;

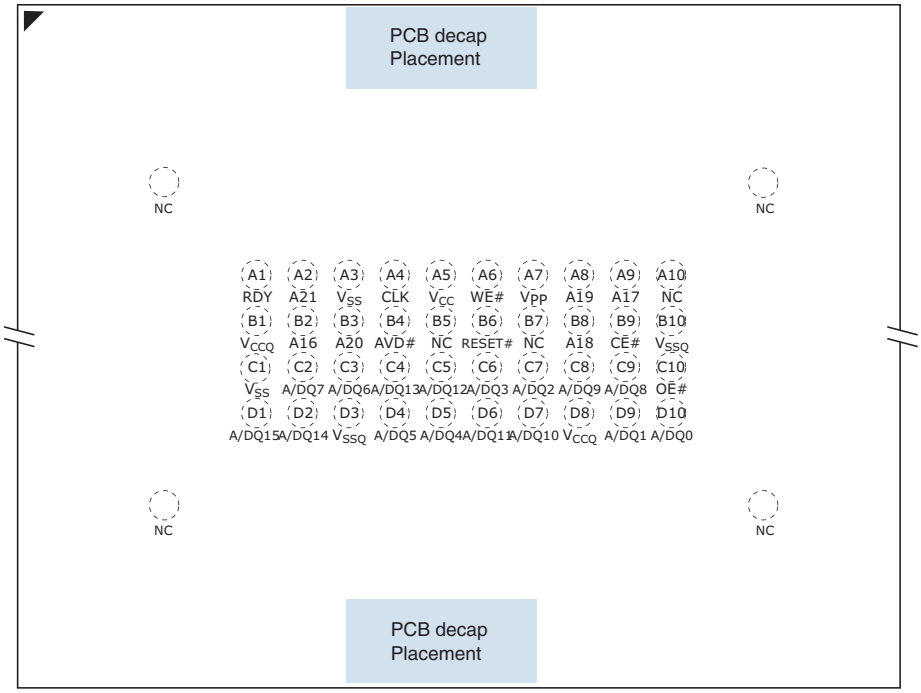
- Ball Pad Size: 0.25 mm (9.84 mils)
- Solder Mask Opening: 0.35 mm (13.78 mils)
- Ball Pitch: 0.5mm (19.685 mils)
- Minimum trace width and trace spacing: 0.1 mm (4 mils)

Once the ball field is cleared, you can redirect the traces in the direction of the SPI controller package while maintaining minimum (4 mils) or better spacing being traces.

4 Supply Routing Guidelines

It is recommended that you meet or beat the supply routing recommendations below.

- V_{SS} and V_{SSQ} balls can be connected to a single ground plane.
- V_{CC} and V_{CCQ} balls can be connected to a single supply plane.
- Maintain low impedance routing (traces > 20 mils) from voltage regulator to flash supply pins.
- Except the package breakout area, maintain a minimum trace width of 20 mils for all supply traces. Both supply and ground traces (or planes) must be closely coupled to each other (i.e. route them close to each other to avoid large inductive loops).
- In case of a 2-layer PCB where both layers can be treated as mixed (signals and supply/ GND routed), ensure GND routing underneath all signal traces for a continuous return path.
- You should place PCB decoupling capacitors as close to the package as possible.
- Minimum 1 µF 0402 ceramic capacitor near each side of the package should be placed, as shown below. The selected capacitor should have low ESL and ESR. V_{CC} and GND trace routing from the capacitor should be as wide as possible to avoid inductive/resistive effects.



- Since V_{PP} is a high voltage signal, route it as close to GND as possible and as far away from V_{CC} and other signals (> 12 mils). Also maintain a wide trace on V_{PP} to provide low inductance path on PCB.

5 Signal Routing Guidelines

It is recommended that you meet or beat the signal routing recommendations below.

Notes

- All length/mismatch guidelines are provided in picoseconds (ps). This is because based on customer topology, the transmission line delay will change (normally 1 inch ~ 166 ps). You should use signal integrity tools to estimate the actual trace velocity and subsequent path delays.
- You should perform signal integrity simulations using Cypress provided IBIS models to determine actual guidelines suitable for their application. The guidelines below and simulation methodology should be used as a starting reference.
- Normally delay is measured between T_{VM} (timing reference voltage which is usually $V_{CC}/2$) of source to T_{VM} of destination. However, please pay attention to signal polarity in the data sheet to ensure that the destination timing is to the rising edge of the destination signal, or falling edge, or both.
- The recommendations below assume (for simplicity) synchronous (burst read) operation and point-to-point routing between controller and Cypress flash. If that is not the case, then you need to first select which topology type to follow (star/T or daisy chain). Star or T topology is recommended (with appropriate termination resistors determined based on IBIS simulations).

5.1 Guidelines

1. Maintain a continuous GND return path for all signals. If A/DQ bus switches layers through a set of vias, it is recommended to add stitching capacitors (connected between V_{CC} and GND) near the transition point. Capacitor value can be equal to or greater than 1 µF.
2. PCB should target impedance of 50 ohms ±15%. However, the actual impedance tolerance needs to be simulated to verify that your topology can accommodate a 15% tolerance around nominal impedance.
3. A/DQ0-15 and clock topology min/max lengths should be determined as below:
   a. First obtain the memory controller and flash port IBIS model.

b. Generate Clock and A/DQ0-15 topologies based on target PCB stackup and topology min/max restrictions. If multiple devices are present on the flash bus, a termination resistor on clock is recommended. Determine value based on simulations.

c. Transmission line coupling (between A/DQ and other nets as well as CLK and other nets) should be included. It is also beneficial to include via models (in case of signal layer changes) as well as transmission line loss for long lines (e.g. > 10 inches).

d. CLK trace should be spaced from any other signal > 3 times Clock trace width (to avoid crosstalk).

e. Simulate both clock delay (TCLK_PCB) and A/DQ delay (TDQ_PCB). Simulations need to be performed across minimum/typical/maximum corners of the IBIS model as well as PCB impedance tolerance. Also odd/even data patterns need to be included in A/DQ switching to incorporate cross-talk effects.

f. Meet the following equation:

TCLK - (TCLK_PCB + TCLK_JITmax + TBACCmax + TDQ_PCBmax + TMSCUmin) ≥ 0

Where;

TCLK = Clock period (since burst reads are single cycle transfer).

TCLK_PCB = Delay on clock line from controller to flash.

TDQ_PCBmax = Worst case delay on A/DQ0-15 line from flash to controller.

TCLK_JITmax = Maximum cycle to cycle jitter on clock at flash pin.

TBACCmax = Maximum Burst access time valid clock to output delay (refer to the S29V/XS-R MirrorBit Flash Family data sheet).

TMCSUmin = Minimum memory controller data set-up time.

This equation ensures that clock travel from the memory controller to (memory clock jitter + memory burst data output + data travel) back to the (memory controller + data set-up at the controller) all fits within a single clock cycle.

4. The Address net length should be calculated (including crosstalk) as follows.

Take the clock length (and topology) determined in Step 3. Meet the following equation for all address signals:

TCLK - TCLK_JITmax - TCNTR_ADD_TCOmax – (TADD_PCBmax - TCLK_PCB) – TACS ≥ 0

Where;

TCNTR_ADD_TCOmax = Max. CLK to address launch delay at the controller.

TCLK_PCB = Flight delay for CLK net.

TADD_PCBmax = Max flight delay for A16-A21 or A/DQ0-15.

TACS = Minimum Address to CLK setup time required at flash.

TCLK_JITmax = Maximum cycle to cycle jitter on clock at flash pin.

This equation assumes that controller switches address on the clock edge previous to the one used by flash to sample the incoming address signals.

5. AVD# length should be calculated as below.

Taking the clock length from Step 3., meet the following equation:

T CLK - TCLK_JITmax - TCNTR_AVD_TCOmax – (TAVD_PCB - TCLK_PCB) – TAVDS ≥ 0

Where;

TCNTR_AVD_TCOmax = Max. CLK to AVD# launch delay at the controller.

TCLK_PCB = Flight delay for CLK net.

TAVD_PCB = Flight delay for AVD#.

TAVDS = Minimum AVD# to CLK setup time required at flash.

TCLK_JITmax = Maximum cycle to cycle jitter on clock at flash pin.

This equation assumes that controller switches AVD# on clock edge previous to the one used by flash to sample the incoming AVD# signal.

6. CE# topology should be determined as below.

   Taking the clock length from Step 3., meet the following equation:

   TCLK - TCLK_JITmax - TCNTR_CE_TCOmax – (TCE_PCB - TCLK_PCB) – TCES ≥ 0

   Where;

   TCNTR_CE_TCOmax = Max. CLK to CE# launch delay at the controller.

   TCLK_PCB = Flight delay for CLK net.

   TCE_PCB = Flight delay for CE#.

   TCES = Minimum CE# to CLK setup time required at flash.

   TCLK_JITmax = Maximum cycle to cycle jitter on clock at flash pin.

   This equation assumes that controller switches CE# on clock edge previous to the one used by flash to sample the incoming CE# signal.

7. OE# topology should be determined as below.

   Taking the clock length from Step 3., meet the following equation:

   TCNTR_ADD_TCOmax + TACCmax - TCNTR_OE_TCOmax - TOE_PCB –TOEmax ≥ 0

   Where;

   TCNTR_ADD_TCOmax = Maximum Address launch delay at the controller.

   TCNTR_OE_TCOmax = Maximum OE# launch delay at the controller.

   TOE_PCB = Flight delay for CE#.

   TOEmax = Maximum OE# set-up time requirement at flash.

8. RDY length should be targeted to be ≤ A/DQ0-15 lengths.
9. Since RESET# is asynchronous, no specific length requirement is placed on this signal.
10. Since writes are asynchronous, no specific length requirement is placed on the WE# signal.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	10/08/2012	Initial version
*A	4960661	MSWI	10/13/2015	Updated in Cypress template
*B	5866638	AESATMP8	08/29/2017	Updated logo and Copyright.

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