

Recommended Mode of Operation for 110-nm S29CD032J/S29CL032J Flash Memory

About this document

Scope and purpose

AN98497 outlines best practices when programming the 110-nm S29CD032J/S29CL032J device. It is recommended that these best practices be observed to achieve error-free operation of the device.

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Background

1 Background

In many system implementations, the S29CD032J/S29CL032J flash device shares an External Bus Interface with other peripherals which can support Burst Read capabilities (see [Figure 1](#)). The System Controller can access the S29CD032J/S29CL032J and perform basic read, erase and program operations. System noise, along with extensive Burst Read activity on the External Bus Interface during embedded programming may create conditions where errors in programming the S29CD032J/S29CL032J can occur.

This behavior has been observed in applications where the System Controller executes code from external SRAM while programming the S29CD032J/S29CL032J flash device. This issue has never been observed in other applications where the System Controller executes code from its internal SRAM while programming the S29CD032J/S29CL032J flash.

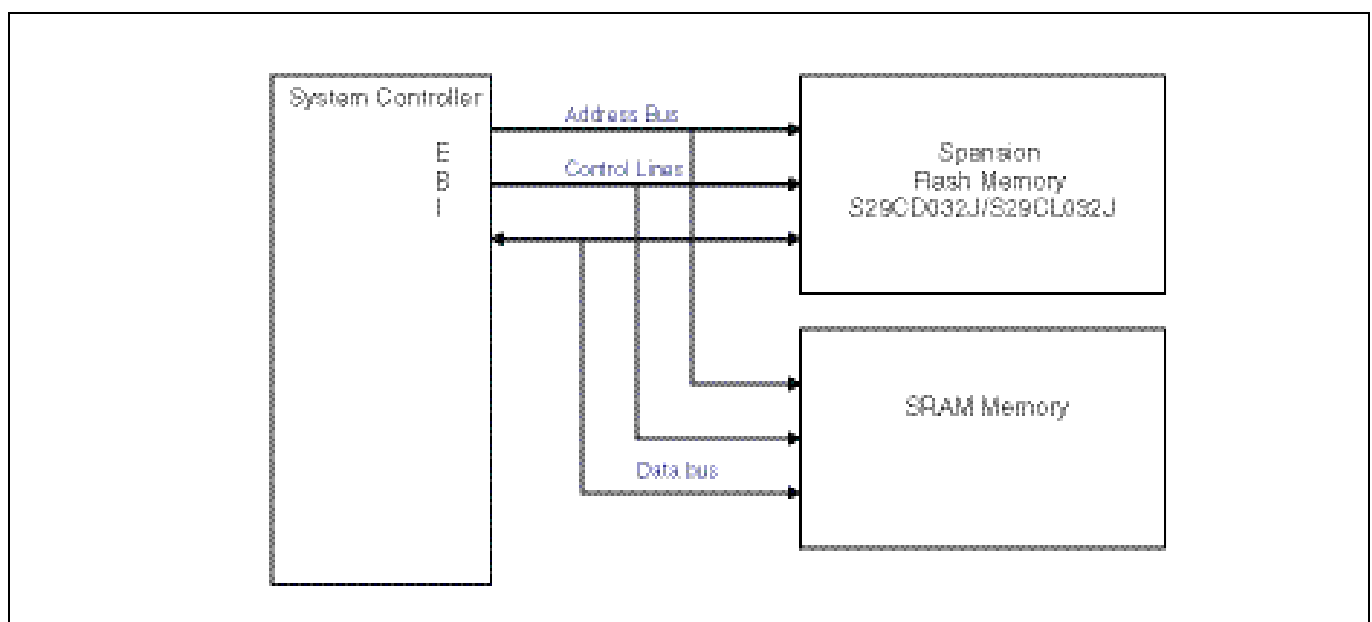


Figure 1 External bus interface

The timing diagram below highlights the start and stop of the “quiet bus time” (t_{WHWH1}). During time t_{WHWH1} it is recommended to minimize burst read activity on the External Bus Interface.

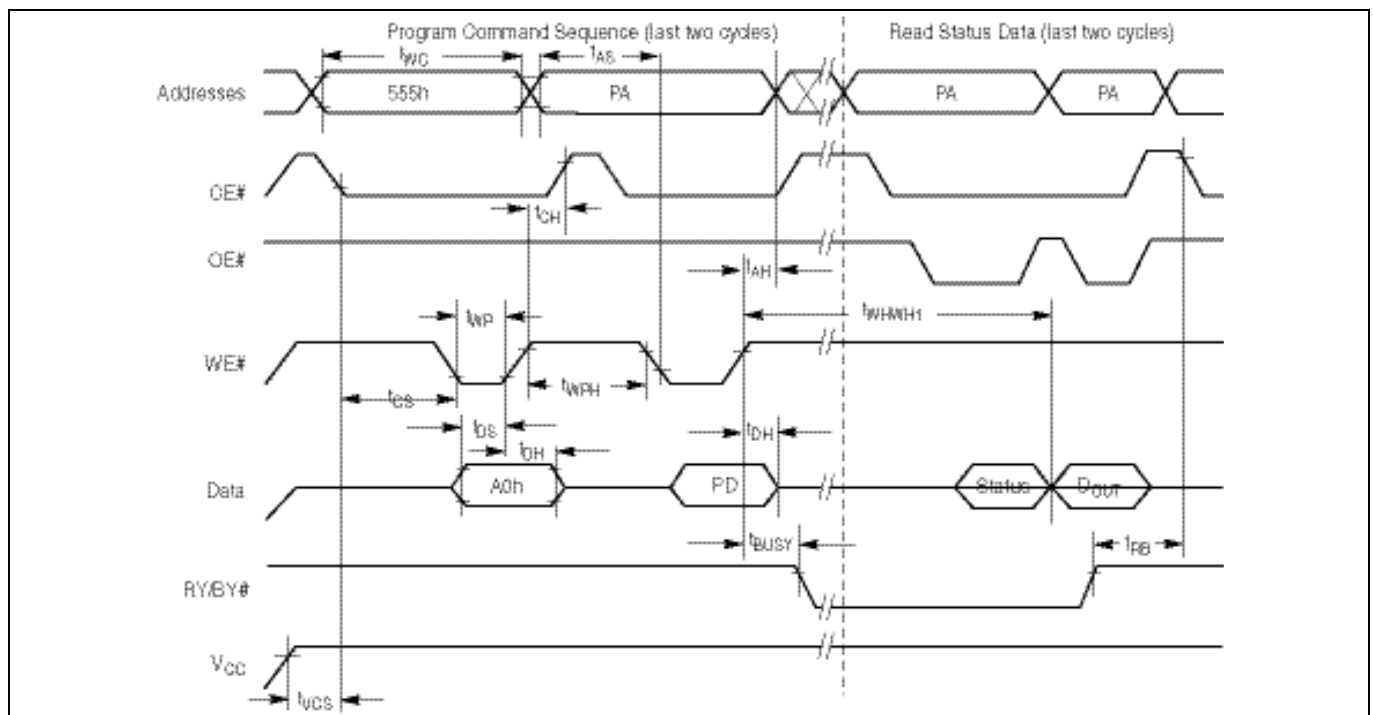


Figure 2 **Program operation timings**

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Revision history

Revision history

Document version	Date of release	Description of changes
**	2009-03-27	New application note.
*A	2015-10-22	Updated to Cypress template.
*B	2017-08-04	Updated Cypress Logo and Copyright.
*C	2021-07-05	Updated Document Title to read as "AN98497 - Recommended Mode of Operation for 110-nm S29CD032J/S29CL032J Flash Memory". Replaced "Cypress" with "Infineon" in required instances across the document. Removed "Cypress" in required instances across the document. Updated to Infineon template.

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