AN98480

S29NS-N to S29NS-P Migration: From the NS-N (110 nm) to the NS-P (90 nm)

AN98480 discusses the design considerations when migrating from the S29NS-N to the S29NS-P.

1 Introduction

Every effort was made to ensure seamless migration from the S29NS-N to the S29NS-P.

1.1 Software Migration Considerations

There are very few changes required in SW when migrating from the S29NS-N to S29NS-P

- Device ID has changed.
- There are no array size driven software changes required when migrating from the same density for the S29NS-N to the S29NS-P due to the sector size, and block size being the same from the S29NS-N to the S29NS-P for the same density. If the customer is changing the density from the S29NS-N to the S29NS-P, then the appropriate density software changes need to be made.
- When migrating from the S29NS064N to the S29NS-P, software changes may be needed to account for the lack of 8 Kword sectors in the S29NS-P devices.

1.2 Hardware Migration Considerations

- The S29NS-N and S29NS-P are offered in the same 44-ball VDE044 package (6.2 mm x 7.7 mm), but the S29NS-P is not offered in the 44-ball VDD044 (9.2 mm x 8 mm) or 48-ball VDC048 (11 mm x 10 mm) packages.

1.3 Improvements from S29NS-N to S29NS-P

- Programmable output slew rate, see Table 1.
- New VDD064-64-Ball Very Thin Fine-Pitch Ball Grid Array, 8.0mm x 9.2mm package (not backward compatible with 44 or 48 ball packages)
- Higher operating frequencies available, 83 MHz and 108 MHz

2 Performance Characteristics

Read Access Time						
Speed Option (MHz)	108		80		66	
Flash Device	NS-N	NS-P	NS-N	NS-P	NS-N	NS-P
Max. Synch. Latency, ns (t_{IACC})	NA	80	80	80	80	80
Max. Synch. Burst Access, ns (t_{BACC})	NA	7.6	9	9	11	11.2
Max. Asynch. Access Time, ns (t_{ACC})	NA	83	80	83	80	83
Max OE# Access Time, ns (t_{OE})	NA	9	9	9	11	9

Typical Program and Erase Times		
Flash Device	NS-N	NS-P
Single Word Programming	40 µs	40 µs
Effective Write Buffer Programming (V_{CC}) Per Word	9.4 µs	9.4 µs
Effective Write Buffer Programming (V_{PP}) Per Word	6 µs	6 µs

Typical Program and Erase Times		
Sector Erase (16 Kword Sector)	150 ms	150 ms
Sector Erase (64 Kword Sector)	800 ms	800 ms

Table 1. Comparisons of Key Features

	S29NS-N	**S29NS-P**
Technology	MirrorBit®	MirrorBit®
Process rule	110 nm	90 nm
V_{CC}	1.70 V to 1.95 V	1.70 V to 1.95 V
Max Density (monolithic)	256 Mbit	512 Mbit
Bank Number for 64 M/128 M/256 M/512 M	8/16/16/NA	NA/16/16/16
Large Sector size 64 M/128 M/256 M/512 M	64 K/128 K/128 K/NA Bytes	NA/128 K/128 K/128 K Bytes
Small Sector Size 64 M/128 M/256 M/512 M	16 K/32 K/32 K/NA Bytes	NA/32 K/32 K/NA Bytes
Top Boot Sector Configurable	Yes	NS128P/NS256P only
Bottom Boot Sector Configurable	**No**	**No**
Simultaneous Read/Write Operation	Yes	Yes
Full/Half drive output slew rate control	No	Yes
32 Word Write Buffer	Yes	Yes
Programmable linear (8/16/32) with or without wrap around and continuous burst read	Yes	Yes
Secure Silicon Sector of 128 words each for Factory and Customer	Yes	Yes
20 year data retention (typical)	Yes	Yes
Operating Temperature Range	-25°C to +85°C	-25°C to +85°C
Hardware (WP#) protection of top and bottom sectors	Yes	Yes
100 K Cycles Per Sector (typical)	Yes	Yes
Command Set Compatible with JEDEC (42.4)	Yes	Yes
Low V_{CC} Write Inhibit	Yes	Yes
Persistent and Password methods of Advanced Sector Protection	Yes	Yes
Write Operation Status Bits for Program or Erase status	Yes	Yes
Program Suspend/Resume Commands	Yes	Yes
Erase Suspend/Resume Commands	Yes	Yes
Unlock Bypass mode to reduce programming time	Yes	Yes
Synchronous or Asynchronous program operation	Yes	Yes
ACC input to reduce factory programming time	Yes	Yes
Support for Common Flash Interface (CFI)	Yes	Yes

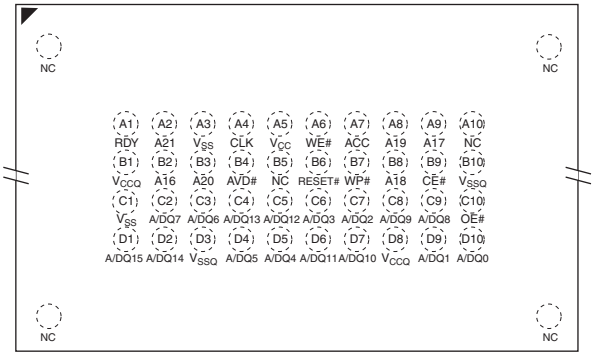
3 Package Migration

Figure 1. S29NS064N and S29NS064P Package Comparison

S29NS064N (64 M)

S29NS064P (64 M)

S29NS064N—44-Ball Very Thin FBGA Connection



Not available on 90 nm

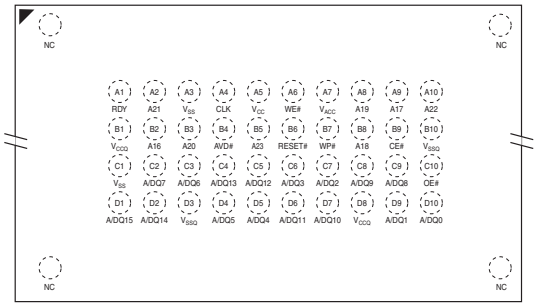
The VDE044 package type and pinout for the S29NS128N and S29NS128P are identical; therefore, the S29NS128P is a drop-in replacement for the S29NS128N (see Figure 2).

Figure 2. S29NS128N and S29NS128P Package Comparison

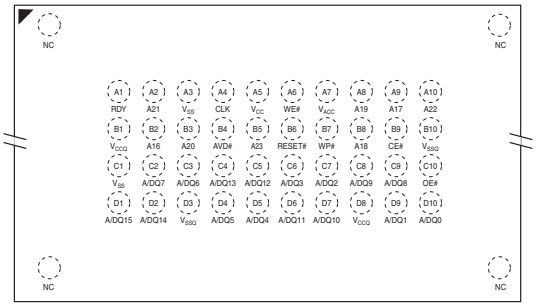
S29NS128N (128

S29NS128P (128 M)

S29NS128N—48-Ball Very Thin FBGA Connection



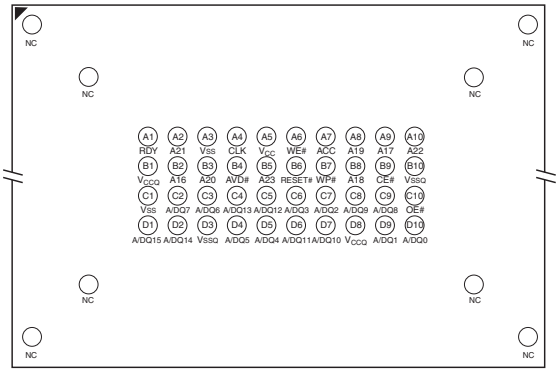
S29NS128P—44-Ball Very Thin FBGA Connection



The S29NS256N package has four additional NC (No Connection) balls as compared to the S29NS256P (see Figure 3), but should not have a negative impact on the migration.

Figure 3. S29NS256N and S29NS256P Package Comparison

S29NS256N—48-Ball Very Thin FBGA Connection



S29NS256P—44-Ball Very Thin FBGA Connection

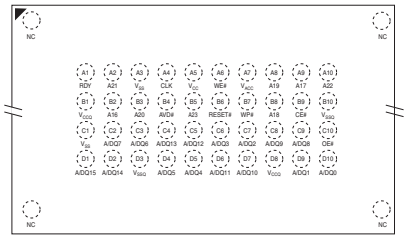
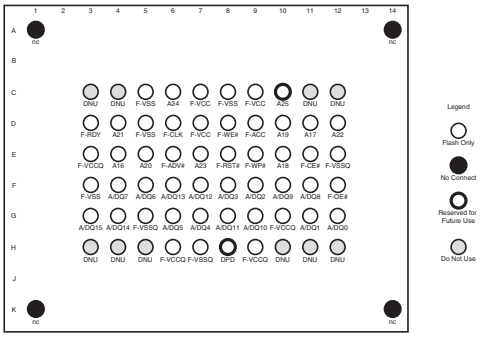


Figure 4. S29NS512N and S29NS512P Package Comparison

S29NS512N

Not available on 110 nm

S29NS512P—VDD064 64-Ball Very Thin FBGA Connection Diagram



4 Synchronous (Burst) Read Mode

Both the S29NS-N and S29NS-P have the same burst modes:

- Continuous Burst
- 8-, 16-, 32- word Burst with wrap around
- 8-, 16-, 32- word Burst without wrap around

Important: The wait states between the two products are different; therefore, the configuration register needs to be updated to reflect the new wait states for the migration.

Please reference the S29NS-N and S29NS-P data sheets for the respective wait state differences.

5 Configuration Register

The S29NS-P adds an additional 16 configuration register bits. See Table 2.

Table 2. Configuration Register Comparison

S29NS-N		S29NS-P			
CR 0		CR 0		CR 1	
CR 0.15	Reserved (0 = default)	CR 0.15	Asynch/Synchronous Read	CR1.15	Reserved
CR 0.14	Reserved (0 = default)	CR 0.14	Boundary Crossing (w & w/o latency)	CR1.14	Reserved
CR 0.13	Programmable Wait States	CR 0.13	Programmable Wait States	CR1.13	Reserved
CR 0.12		CR 0.12		CR1.12	Reserved
CR 0.11		CR 0.11		CR1.11	Reserved
CR 0.10	RDY Polarity	CR 0.10	RDY Polarity	CR1.10	Reserved
CR 0.9	Reserved (1 = default)	CR 0.9	Reserved (1 = default)	CR1.9	Reserved
CR 0.8	RDY active prior or with data	CR 0.8	RDY active prior or with data	CR1.8	Reserved
CR 0.7	Reserved (1 = default)	CR 0.7	Reserved (1 = default)	CR1.7	Reserved
CR 0.6	Reserved (1 = default)	CR 0.6	Reserved (1 = default)	CR1.6	Reserved
CR 0.5	Reserved (0 = default)	CR 0.5	Reserved (0 = default)	CR1.5	Reserved
CR 0.4	Reserved (0 = default)	CR 0.4	RDY Function (0 = default)	CR1.4	**Output Drive strength**
CR 0.3	Burst read w/wo Wrap around	CR 0.3	Burst read w/wo Wrap around	CR1.3	Reserved
CR 0.2	Burst length and Mode (8/16/ 32/ Continuous Word)	CR 0.2	Burst length and Mode (8/16/ 32/ Continuous Word)	CR1.2	Reserved
CR 0.1		CR 0.1		CR1.1	Reserved
CR 0.0		CR 0.0		CR1.0	**Additional Programmable Wait State**

6 Autoselect

The Autoselect information is very similar between the S29NS-N and S29NS-P, and are due to differences in the device IDs (see **bold** text in Table 3). See Table 3 for details.

Table 3. Autoselect Comparison

Description	Address	Read Data	
		S29NS-N	S29NS-P
Manufacturer ID	(BA) + 00h	0001h	0001h
Device ID	(BA) + 01h	**2D7E (NS256N)** **2C7E (NS128N)** **2B7E (NS064N)**	**307E (NS512P)** **317E (NS256P)** **327E (NS128P)**
Device ID	(BA) + 0Eh	**2D2F (NS256N)** **2C35 (NS128N)** **2B33 (NS064N)**	**303F (NS512P)** **3141 (NS256P)** **3243 (NS128P)**
Device ID	(BA) + 0Fh	**2D00 (NS256N)** **2C00 (NS128N)** **2B00 (NS064N)**	**3000 (NS512P)** **3100 (NS256P)** **3200 (NS128P)**

Table 3. Autoselect Comparison

Description	Address	Read Data	
		S29NS-N	S29NS-P
Indicator Bits	(BA) + 07h	DQ15-DQ8 = Reserved DQ7 (Factory Lock Bit): 1=Locked, 0=Not Locked DQ6 (Customer Lock Bit): 1=Locked, 0=Not Locked DQ5 (Handshake Bit): 1=Reserved, 0=Standard Handshake DQ4, DQ3 (WP# Protection Boot Code): 01=WP# Protects Top Boot sectors DQ2 - DQ0 = Reserved	DQ15-DQ8 = Reserved DQ7 (Factory Lock Bit): 1=Locked, 0=Not Locked DQ6 (Customer Lock Bit): 1=Locked, 0=Not Locked DQ5 (Handshake Bit): 1=Reserved, 0=Standard Handshake DQ4, DQ3 (WP# Protection Boot Code): 01=WP# Protects Top Boot sectors DQ2 - DQ0 = Reserved
Sector Block Lock/Unlock	(SA) + 02h	0001h=Locked, 0000h = Unlocked	0001h=Locked, 0000h = Unlocked

7 Programmable Output Slew Rate Control

This feature allows the user to change the output slew rate (or drive strength) during a read operation by setting the configuration register bit CR1.14. This feature allows the user to tune the drive strength to match their system requirements.

Table 4. Programmable Output Slew Rate

Mode	Description	I_{OL} & I_{OH}
1	Full Drive (Default)	100 µA
2	Half Drive	50 µA

8 DC Characteristics

There are minor differences between the S29NS-N and S29NS-P DC Characteristics. These differences are not detailed in the migration guide due to the numerous parameters. Please refer to the respective data sheets for reference.

9 AC Characteristics

There are minor differences between the S29NS-N and S29NS-P AC Characteristics. These differences are not detailed in the migration guide due to the numerous parameters. Please refer to the respective data sheets for reference.

10 Lock Register

The Lock Register bit DQ3 assignment is different between the S29NS-N and S29NS-P. Please see Table 5 for the differences between the S29NS-N and S29NS-P

Table 5. Lock Register Comparison

Device	DQ15-05	DQ4	DQ3	DQ2	DQ1	DQ0
S29NS-N	Undefined	Undefined	Undefined	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Customer Secure Silicon Sector Protection Bit
S29NS-P	1's	DYB Lock Boot Bit 0 = sectors power up protected (Default) 1= sectors power up unprotected	PPB One-Time Programmable Bit 0=All PPB erase command disabled 1=All PPB Erase command enabled	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Customer Secure Silicon Sector Protection Bit

11 Memory Array Commands

There are some minor differences between the S29NS-N and S29NS-P for the Memory Array Commands. These differences are shown in Table 6.

Table 6. S29NS-N and S29NS-P Command Definitions (Sheet 1 of 2)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
S29NS-N Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20								
	Program (7)	2	XXX	A0	PA	PD										
	Reset (8)	2	BA	90	XXX	00										
S29NS-P Unlock Bypass (13)	Unlock Bypass Entry (10)	3	555	AA	2AA	55	555	20								
	Unlock Bypass Program (7), (8)	2	XX	A0	PA	PD										
	Unlock Bypass Sector Erase (7), (8)	2	XX	80	SA	30										
	Unlock Bypass Erase (7), (8)	2	XX	80	XXX	10										
	Unlock Bypass CFI (7), (8)	1	XX	98												
	Unlock Bypass Reset	2	XX	90	XXX	00										
S29NS-N Set Configurfation Register (9)		4	555	AA	2AA	55	555	D0	X00	CR						
S29NS-P Set Configuration Register (14, 15, 16)		5	555	AA	2AA	55	555	D0	X00	CR0	X01	CR1				
S29NS-N Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR						
S29NS-P Read Configuration Register		4	555	AA	2AA	55	555	C6	X0 (0 or 1)	CR (0 or 1)						

Table 6. S29NS-N and S29NS-P Command Definitions (Sheet 2 of 2)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
S29NS-N Secured Silicon Sector Command Definitions	Secured Silicon Sector Entry (11)	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Program	2	XX	A0	00	data										
	Secured Silicon Sector Read	1	00	data												
	Secured Silicon Sector Exit (12)	4	555	AA	2AA	55	555	90	XX	00						
S29NS-P Secured Silicon Sector Command Definitions	Secured Silicon Sector Entry (17)	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Secured Silicon Sector Read	1	00	data												
	Secured Silicon Sector Exit (7)	4	555	AA	2AA	55	555	90	XX	00						

Legend

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

SA = Address of the sector to be verified (in autoselect mode) or erased. SA includes BA. Address bits A_{max}–A14 uniquely select any sector (NS256N and NS128N), and address bits A_{max} - A13 uniquely select any sector (NS064N).

BA = Address of the bank (A23–A20 for S29NS256N, A22–A19 for S29NS128N), and A21-A19 for S29NS064N, that is being switched to autoselect mode, is in bypass mode, or is being erased.

CR = Configuration Register set by data bits D15-D0.

PWD3–PWD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.

RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 0, if unprotected, DQ1 = 1.

RD(2) = DQ2 protection indicator bit. If protected, DQ2 = 0, if unprotected, DQ2 = 1.

RD(4) = DQ4 protection indicator bit. If protected, DQ4 = 0, if unprotected, DQ4 = 1.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes

1.See description of bus operations.

2.All values are in hexadecimal.

3.Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.

4.Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.

5. Unless otherwise noted, address bits A_{max}–A12 are don't cares.

6. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.

7. The Unlock Bypass command sequence is required prior to this command sequence.

8. The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.

9. Requires the RESET# command to configure the configuration register.

10. Write Buffer Programming can be initiated after Unlock Bypass Entry

11. Entry commands are needed to enter a specific mode to enable instructions only available within that mode.

12. The Exit command must be issued to reset the device into read mode. Otherwise the device will hang.

13. When device is in Unlock Bypass mode, do not enter another command before Unlock Bypass reset command is issued).

14. Do not use 0x30 for CR data (otherwise in the erase suspend --> CR read or set sequence, the device will go into erase resume instead of CR read or set).

15. Software reset is needed after CR read (otherwise the device is still in CR read mode).

16. Configuration Registers can not be programmed out of order. CR0 must be programmed prior to CR01 otherwise the configuration registers retain their previous settings.

17. Unless otherwise noted, address bits Amax – A14 are don't cares.

12 Common Flash Memory Interface (CFI)

The CFI information differences between the NS-N and the NS-P are due to the addition of the 512 Mb density for the NS-P and performance differences between the NS-N and NS-P. Please consult the CFI tables for the differences between the NS-N and NS-P.

Document History Page

Document Title: AN98480 - S29NS-N to S29NS-P Migration: From the NS-N (110 nm) to the NS-P (90 nm) Document Number: 001-98480				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/11/2007	Initial version
*A	–	–	01/21/2008	Updated Process rule values in Comparisons of Key Features Table
*B	4955494	MSWI	10/09/2015	Updated in Cypress template

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